Polyphase Modulation Using a FPGA for High-Speed Applications

February 2008, version 1.0 Application Note 511

Introduction

This application note reviews and analyzes a polyphase modulation scheme that generates high-frequency intermediate frequency (IF) carrier signals in digital IF modems using an Altera® FPGA. Modulating IF signals to higher carrier frequencies takes full advantage of the high sampling rate of modern digital-to-analog converters and eases the requirement for analog voltage-controlled oscillators (VCO) and mixers. This application note presents a mathematical model of the polyphase system which provides insights into system parameter selections. In particular, this application note discusses the polyphase filter design.

Polyphase Modulation

In modern digital communication systems, IF modulation is often implemented in the digital domain to ease the requirement for analog devices. For instance, in digital transmission, baseband signals are up-converted to IF frequency, then modulated by IF sinusoidal carriers. The digital IF carriers and information signals are converted to analog signals by a high-speed, digital-to-analog converter (DAC), and finally modulated onto carrier signals by an analog voltage-controlled oscillator.

An IF modem usually uses a numerically controlled oscillator (NCO) to generate digital IF carriers. As a result, the IF Carrier frequency is limited by the Nyquist theorem to half the sampling rate of the NCO. This often leaves the high-speed DAC underutilized, because many modern DACs can support up to GHz sampling frequencies.

To solve this issue, an over-sampling polyphase modulation scheme was proposed [1] that utilizes the high-speed, low-voltage differential serializer (LVDS) embedded in the Altera FPGA to achieve higher-than-Nyquist frequency IF carriers. The key is to exploit the periodicity of sinusoidal signals and the high sampling frequency of the LVDS serializer.

This application note reviews the theory used in *Implementing an FPGA-Based Broadband Modem Using Model-Based Design*, and provides a detailed discussion about design considerations when implementing the proposed scheme.

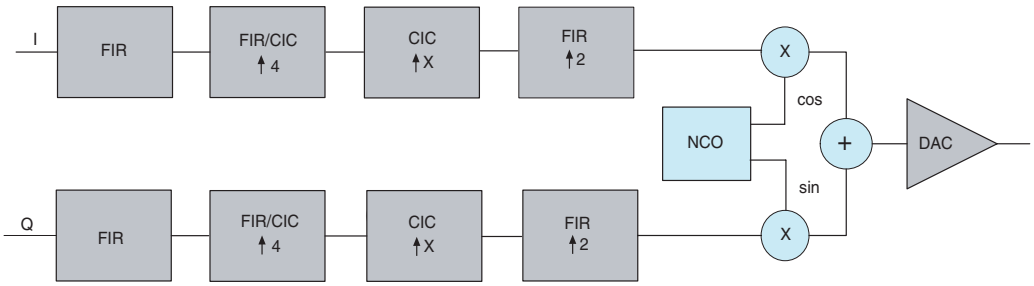
System Model

Conventional IF Modulation

A conventional variable-rate, digital-up converter for communications systems is shown in Figure 1. "I" denotes the inphase signal; "Q" denotes the quadrature signal. After pulse shaping, the baseband signal is often up-converted by a cascade of two half-band filters.

For more information, refer to *Multirate Signal Processing for Communication Systems*.

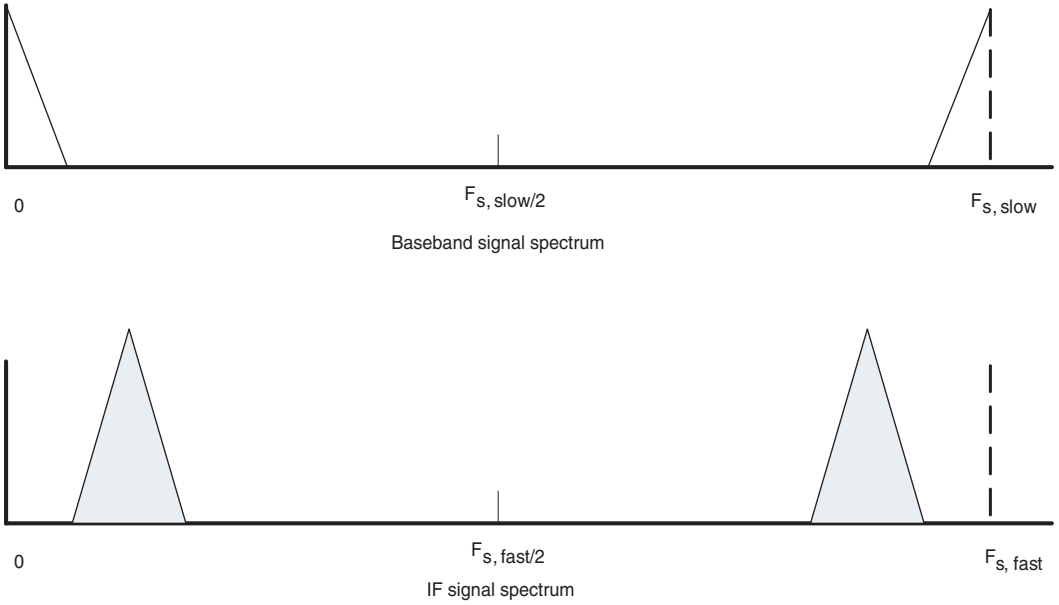
Figure 1. Conventional Digital-Up Conversion System



A variable rate, cascaded integrator-comb (CIC) filter can further provide a large range of rate change. It is often accompanied by a compensating finite impulse response (FIR) filter. The interpolated digital signal is then modulated by IF sinusoidal carriers.

The baseband and IF band signal spectrums are shown in Figure 2. In this system, the baseband signal is modulated to a carrier that is less than half of the frequency of the NCO clock frequency.

Figure 2. Baseband and IF Band Signal Spectrum of the Conversional System Shown in Figure 1



Architecture of the Polyphase Modem

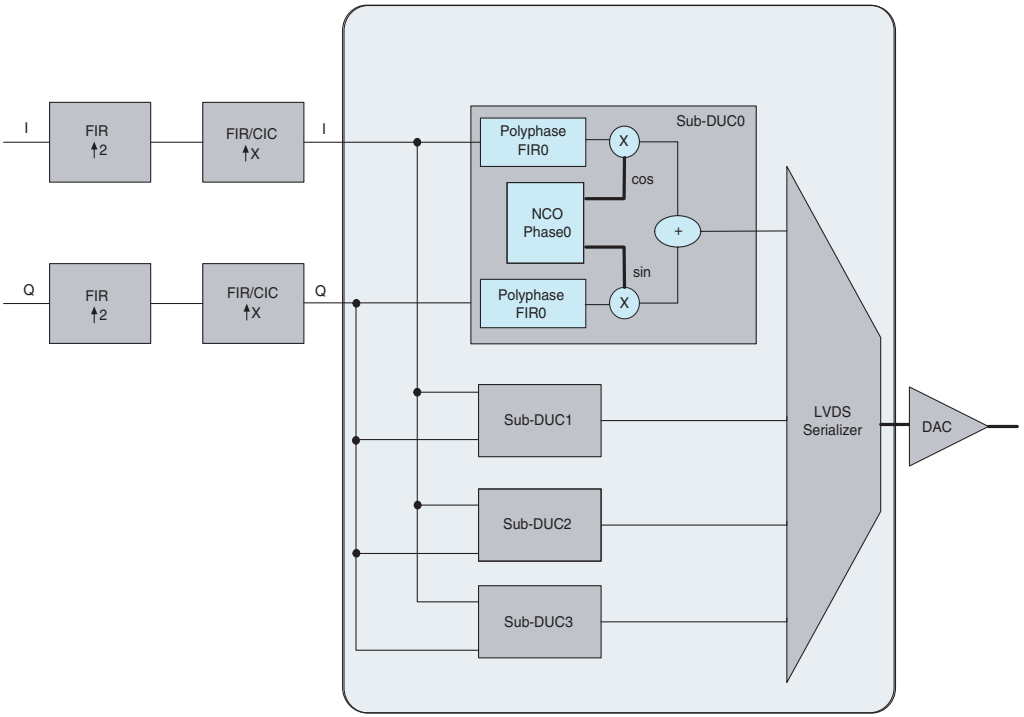
The configuration shown in Figure 1 usually generates carrier signals that do not exceed 150 MHz. To take full advantage of the high sampling rate of the DAC, which can operate at 1 GHz, a polyphase up-converter is proposed, as shown in Figure 3.

For more information, refer to *Implementing an FPGA-Based Broadband Modem Using Model-Based Design*.

In the new polyphase system, the I and Q signals are processed by N-parallel sub-up converters (sub-DUC). Each sub converter is essentially a polyphase component. A high-speed LVDS serializer acts as a multiplexer to sample outputs from the N-polyphase components.

The following section explains how the modules highlighted in Figure 3 modulate the interpolated input signals to carriers that can exceed the Nyquist frequency of a NCO.

Figure 3. Polyphase-Up Conversion System with Aliasing



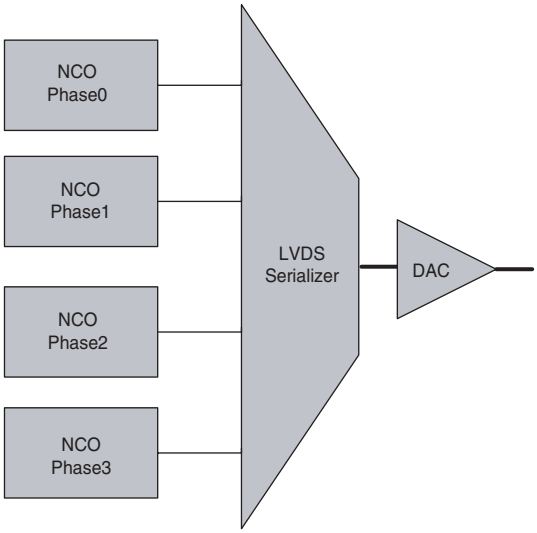
Polyphase Modulation Algorithm

High-Frequency Carrier Generation

To understand the polyphase modem, it is best to first investigate how to generate a high-frequency carrier using a moderate-speed FPGA.

Suppose N-parallel NCOs with different phases are sampled by a LVDS, as shown in Figure 4.

Figure 4. Polyphase NCOs



If the clock rate of the NCO is f_{NCO}, the sampling rate of the LVDS serializer is Nf_{NCO}, which equals the sampling rate of the high-speed DAC f_{dac}. Denote f_{out} as the output signal carrier frequency (in Hz) of the LVDS serializer. Define the normalized digital frequency θ as:

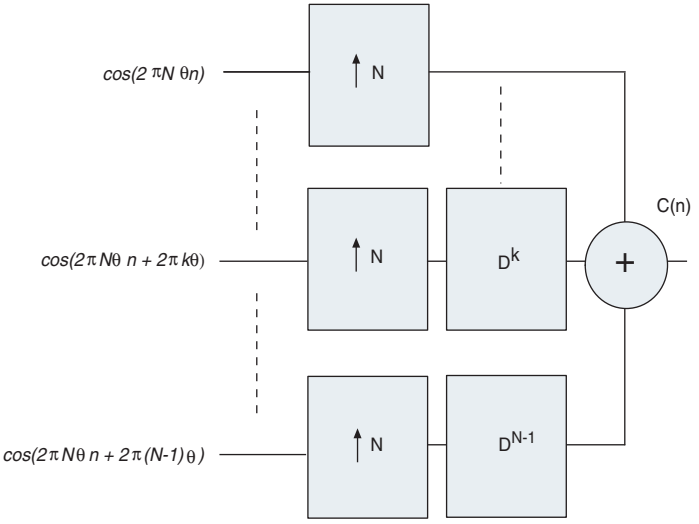
(1)
$$\theta = \frac{f_{out}}{f_{dac}} = \frac{f_{out}}{Nf_{NCO}}$$

The goal is to achieve a high f_{out} that is not limited to $f_{NCO}/2$.

To generate a sinusoidal output signal with frequency θ, control the parameters of the k-th polyphase NCO so that it generates $\cos(2\pi N\theta + 2\pi k\theta)$ and $\sin(2\pi N\theta + 2\pi k\theta)$. k is an integer between [0, N-1].

Note that the polyphase NCOs operate at low frequency f_{NCO}. Therefore, the signal model of Figure 4 is given in Figure 5.

Figure 5. Polyphase NCO with Aliasing



The multiplex operation of the LVDS serializer in Figure 4 can be modeled as a delayed sum of N-upsampled data sources. Therefore, the final output data off the FPGA to DAC is upsampled by an additional factor of N. D^k denotes k-sample delay. Because delay is easily modeled in the Z-transform domain, you will express the signals in the Z-domain. Recall that the Z-transform of a cosine signal is given by [3]

(2)
$$\cos(2\pi N\theta n)u(n) \xrightarrow{Z} \frac{1}{2}\left[\frac{1}{1-e^{j2\pi N\theta}z^{-1}} + \frac{1}{1-e^{-j2\pi N\theta}z^{-1}}\right]$$

with $u(n)$ denoting the step function. You can express upsampling by a factor of N by raising the power of the delay factor z^{-1} to z^{-N}.

Therefore, the Z-transform of the combined signal at the output of the LVDS serializer can be written as:

(3)

$$C(z)=\sum_{k=0}^{N-1}\frac{1}{2}\left[\frac{e^{j2\pi k\theta}z^{-k}}{1-e^{j2\pi N\theta}z^{-N}}+\frac{e^{-j2\pi k\theta}z^{-k}}{1-e^{-j2\pi N\theta}z^{-N}}\right]=\frac{1}{2}\left[\frac{1}{1-e^{j2\pi\theta}z^{-1}}+\frac{1}{1-e^{-j2\pi\theta}z^{-1}}\right]$$

$C(z)$ is the Z-transform of a sinusoidal signal $\cos(2\pi N\theta + 2\pi k\theta)$. More importantly, the output of the LVDS serializer has a high sampling rate Nf_{NCO}; therefore, the output carrier signal relative to this high sampling frequency can exceed the FPGA clock. For instance, at f_{dac} = 1 GHz, N = 4, and $\theta = 2/5$, the output carrier frequency equals 400 MHz. In contrast, the polyphase NCOs operate at merely 250 MHz, giving the NCO Nyquist frequency $f_{NCO}/2$ at 125 MHz.

Effect of Aliasing

After the DAC sampling frequency and desired output carrier frequency are decided, determine the polyphase factor N and digitized output frequency θ. Next, configure the polyphase NCOs to generate proper sinusoidal signals. When using the Altera NCO MegaCore,® note that the discrete normalized frequency is in the range (0, ½). Therefore, when $N\theta$ exceeds ½, $\cos(2\pi N\theta + 2\pi k\theta)$ is an aliased signal. Suppose $N\theta = m + \omega$, where m is an integer (m can be non-positive), ω is a fractional number in the range (0, 1). We have:

(4)

$$\cos(2\pi N\theta n+2\pi k\theta)=\cos(2\pi\omega n+2\pi k\theta)=\begin{cases}\cos(2\pi\omega n+2\pi k\theta) & \text{if } 0<\omega<1/2\\ \cos(2\pi(1-\omega)n-2\pi k\theta) & \text{if } 1/2<\omega<1\end{cases}$$

(5)

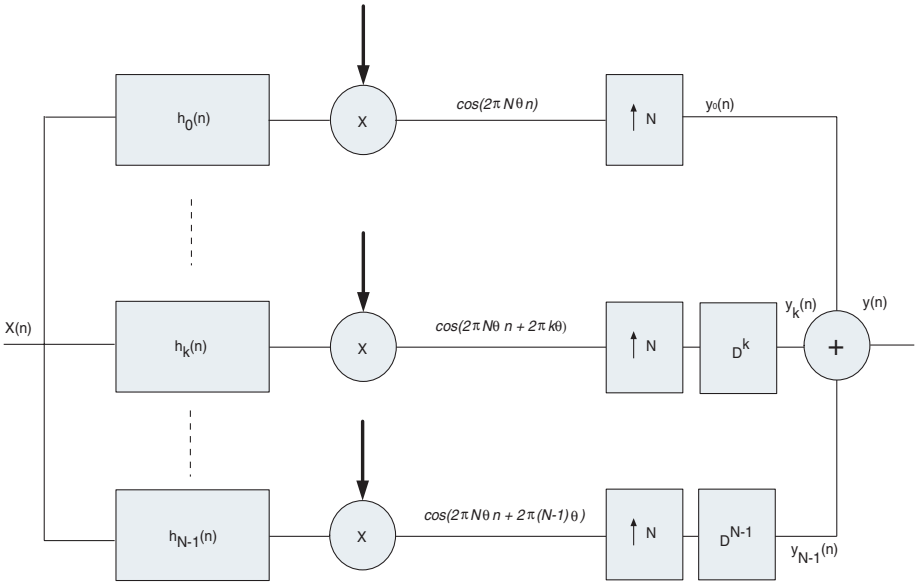
$$\sin(2\pi N\theta n+2\pi k\theta)=\sin(2\pi\omega n+2\pi k\theta)=\begin{cases}\sin(2\pi\omega n+2\pi k\theta) & \text{if } 0<\omega<1/2\\ -\sin(2\pi(1-\omega)n-2\pi k\theta) & \text{if } 1/2<\omega<1\end{cases}$$

For example, at $\theta = 2/5$ and N = 4, the discrete NCO carrier frequency is $1 - \omega = 2/5$. If the NCO clock is 250 MHz, the polyphase cosine and sine signals are centered at 100 MHz. In other words, when exploiting the high sampling frequency of the LVDS serializer (which can reach up to 1 GHz), you can generate a zero-phase 400 MHz carrier signal using four 100 MHz sinusoidal signals with different phases.

Polyphase Modulation

Using the polyphase technique discussed in the previous sections, modulate an IF signal to a high-frequency carrier by adding a low-pass polyphase filter, as shown in Figure 6.

Figure 6. Inphase Signal Path of the Polyphase Up-Converter



In the following, we analyze the inphase signal path. The quadrature signal path can be analyzed similarly. Denote the impulse response of the k-th sub-DUC polyphase component in Figure 3 as $h_k(n)$. Aggregate the N-parallel paths of the inphase signal, as shown in Figure 6. Let $x(n)$ denote the interpolated inphase signal at the output of the variable rate CIC filter. Note that the polyphase FIR filters are single rate; therefore, the upsampling effect is due to the high-speed sampling by the LVDS serializer.

You can now derive the spectrum of the LVDS serializer output. The Z-transform of each polyphase signal $y_k(n)$ is:

(6)

$$Y_k(z) = \frac{1}{2} e^{j2\pi\theta} H_k(e^{-j2\pi N\theta} z) X(e^{-j2\pi N\theta} z) + \frac{1}{2} e^{-j2\pi\theta} H_k(e^{j2\pi N\theta} z) X(e^{j2\pi N\theta} z)$$

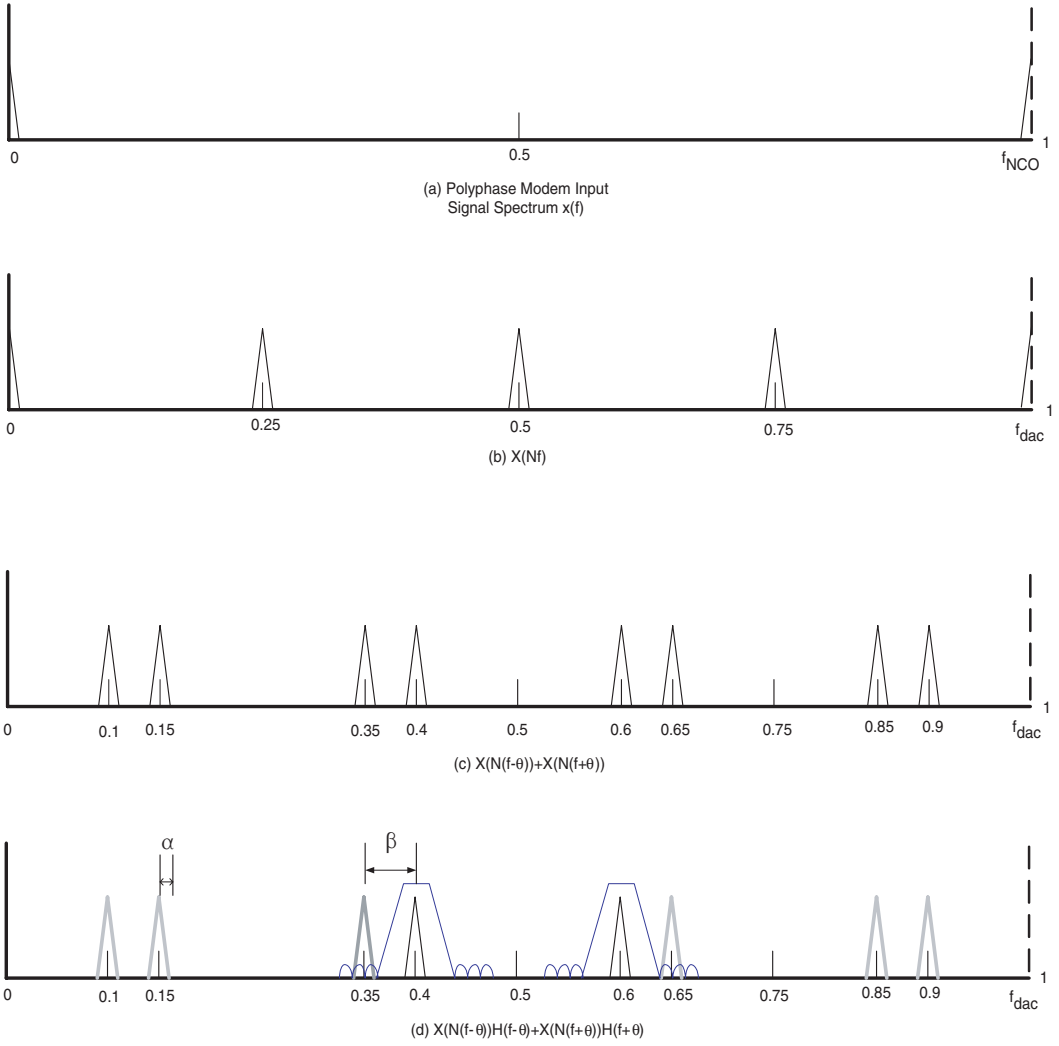
$H_k(z)$ is the Z-transform of the k-th polyphase filter, and $X(z)$ is the input signal. Let $z = j2\pi f$, where f is the digitized frequency. With the sum from equation (6) over N-polyphase components, we have:

(7)

$$\begin{aligned} Y(f) &= \frac{1}{2} \sum_{k=0}^{N-1} e^{j2\pi k\theta} X(N(f-\theta)) H_k(N(f-\theta)) e^{-j2\pi kf} + \\ &\frac{1}{2} \sum_{k=0}^{N-1} e^{-j2\pi k\theta} X(N(f+\theta)) H_k(N(f+\theta)) e^{-j2\pi kf} \\ &= \frac{1}{2} X(N(f-\theta)) H(f-\theta) + \frac{1}{2} X(N(f+\theta)) H(f+\theta) \end{aligned}$$

Equation (7) indicates that the N "squeezed" input spectrum images are shifted to center at θ [4], then low-pass filtered by the interpolation filter H(f). The output signal spectrum, where N = 4 and θ = 2/5, is shown in Figure 7.

Figure 7. Polyphase Modem Output Signal Spectrum



Polyphase Filter Design

Equation (7) and Figure 7 show that the input signal is modulated onto a carrier that centers at θf_{dac}. Therefore, the desired energy clusters appear at θ and 1 – θ when the frequency is normalized. However, in addition to the desired signal spectrum, N pairs of images of the input signal spectrum are also observed due to the N-factor interpolation embedded

in the LVDS N-factor serialization. These image energy clusters appear at: $m/N \pm \theta$, where m is an integer, which satisfies $0 \le m/N \pm \theta \le 1$. Due to modulation, some of the image spectrum may appear very close to the desired signal spectrum.

Denote m_0 as the integer that gives the closest image to the desired signal. m_0 can be found as the integer that minimizes:

(8)
$$\beta = \min_{m \neq 0, m = m_0} \left(\left| \left(\frac{m}{N} \pm \theta \right) - \theta \right| \right)$$

For instance, in the example shown in Figure 7, the desired signal spectrum occurs at $m = 0$ and $f = \theta = 0.4$. Its closest image occurs at $m_0 = 3$ and $f = \theta - \beta = 0.35$.

To reject the images, a well-designed, polyphase low-pass filter is necessary.

Suppose the signal frequencies are normalized by f_{dac}. The input signal to the polyphase modem is band limited to α . Therefore, choose the pass band edge of the low-pass filter H(f) to be:

(9)
$$w_p = \alpha$$

The stop band edge depends on where the closest image occurs; therefore, it is a function of the LVDS serialization factor N and the desired output frequency θ. Suppose the distance between the desired signal and the closest image is β, which is defined in Equation (8).
The stop band edge of the polyphase filter is given by:

(10)
$$w_s = \beta - \alpha$$

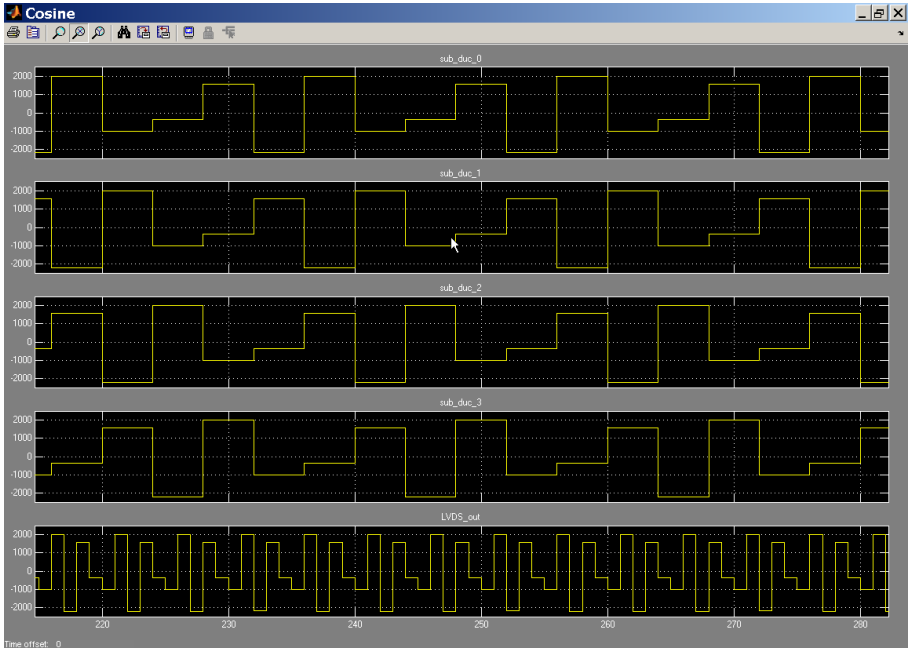
Combine equations (9) and (10), and the transition bandwidth of the polyphase filter is $\beta - 2\alpha$. Note that this transition bandwidth is usually much sharper than the transition bandwidth of a conventional interpolation filter in an IF modem. In a conventional IF modem, whether it is a half-band filter cascade or an interpolation FIR filter cascade, the last stage filter usually has a relaxed transition bandwidth requirement [2] due to the spectrum squeezing effect of interpolation.[4] Unfortunately, this is not the case for the polyphase modem filter.

Although the polyphase filtering operation happens before polyphase modulation, the overall filtering effect exhibits some band-pass filtering properties. This causes the polyphase filter to have a higher order and to have enough stop-band attenuation for image rejection.

Filter Design Example

A proof of concept polyphase modem is implemented on an Altera Cyclone® II device (2C70F672C6), clocked at 100 MHz. The LVDS serializer has a serialization factor of N = 4 and a high-speed sampling frequency of 400 MHz. The normalized output frequency is $\theta = 0.4$. Figure 8 shows the simulated LVDS serializer output for a polyphase NCO system described in Figure 4. Obviously, by taking samples from phase-shifted cosine signals, you can construct a higher frequency sinusoidal signal.

Figure 8. Simulation of High Frequency Carrier Generation from Phase-Shifted Sinusoidal Signals



When random input data with 3.185 MHz bandwidth are used, you can set up the system as in Figure 3. In this case, the polyphase modem modulates the 3.185 MHz input signal onto 160 MHz carriers, well exceeding the device clock rate of 100 MHz. The output signal spectrum follows Figure 7.

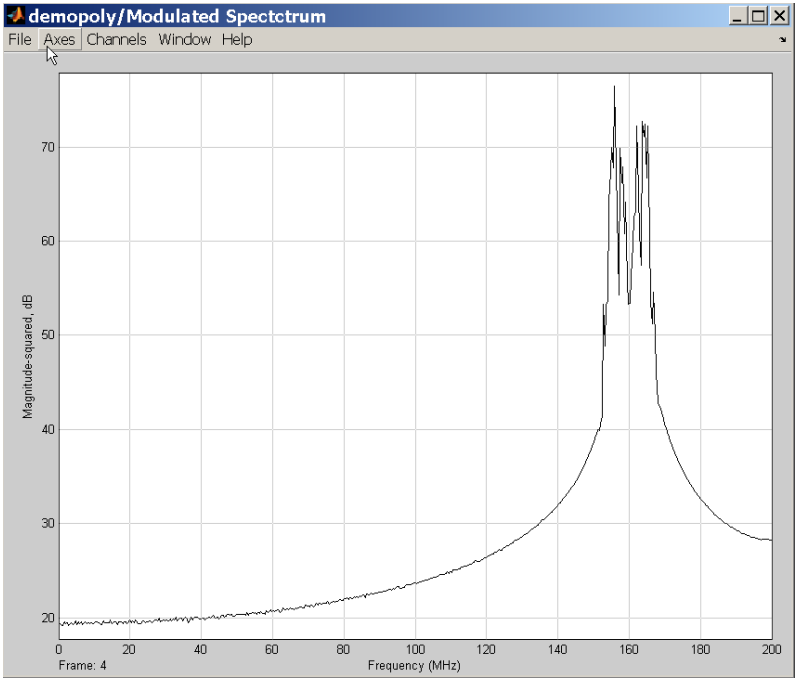
You can find a design example implementing the polyphase scheme in *Polyphase Modulation With Aliasing for Data Up-Conversion*.

To obtain a clean output signal spectrum, the polyphase filter design is based on:

- $w_p = 3.185/400 = 0.0039$
- $w_s = 0.05 - w_p = 0.0344$

Our simulation shows that a low-pass filter at order 100 gives sufficient stop band attenuation with pass-band ripple at approximately 0.003 dB. The signal spectrum at the LVDS output is shown in Figure 9. Notice that no visible interfering image spectrums are observed.

Figure 9. Simulation of LVDS Output Signal Spectrum



Conclusion

This application note analyzes a polyphase modulation technique that generates high-frequency carriers using Altera FPGAs with high-speed LVDS serializers. This application note also discusses the construction of high-frequency carriers and the design of the polyphase filter.

Referenced Documents

This application note references the following documents:

1. Rob Pelt, *Implementing an FPGA-Based Broadband Modem Using Model-Based Design*, GSPx, Nov. 2005.
2. F. J. Harris, *Multirate Signal Processing for Communication Systems*, Prentice Hall, 2004.
3. A. V. Oppenheim and A. S. Willsky and S. H. Nawab, *Signals and Systems*, 2nd ed., Prentice Hall, 1996.
4. A. V. Oppenheim, R. W. Schafer and J. R. Buck, *Discrete-time Signal Processing*, 2nd ed., Prentice Hall, 1999.
5. *Polyphase Modulation With Aliasing for Data Up-Conversion*

Document Revision History

Table 1 shows the revision history for this application note.

Table 1. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
February 2008 v1.0	Initial release.	—

101 Innovation Drive
San Jose, CA 95134
www.altera.com
Technical Support:
www.altera.com/support
Literature Services:
literature@altera.com