Integrating Uplink Desubchannelization & Ranging Modules for WiMAX

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Introduction

Altera provides building blocks to accelerate the development of a worldwide interoperability for microwave access (WiMAX) compliant basestations. All of Altera's WiMAX modules have input and output interfaces that ease integration into WiMAX systems with both Altera® and non-Altera modules. This application note describes a reference design that demonstrates the integration of the Altera® desubchannelization and ranging modules. The integration requires no glue logic, as the modules have been designed to seamlessly connect to one another.

WiMAX is an emerging broadband wireless technology that promises high-speed data services. The *IEEE 802.16e-2005* standard enables mobility. There is significant market potential for this technology and it is currently being deployed by equipment manufacturers. Altera devices are the ideal platform for high throughput DSP designs such as those found on a WiMAX basestation channel card, because of the dedicated multiplier blocks and inherent parallel structure. This structure gives a significant cost and performance advantage over general purpose processors for this type of design.

For more information on *IEEE 802.16e-2005*, refer to the *IEEE Standard for Local and Metropolitan Area Networks, Part 16: Air Interface for Fixed Broadband Wireless Access Systems, IEEE P802.16e-2005, February 2006.*

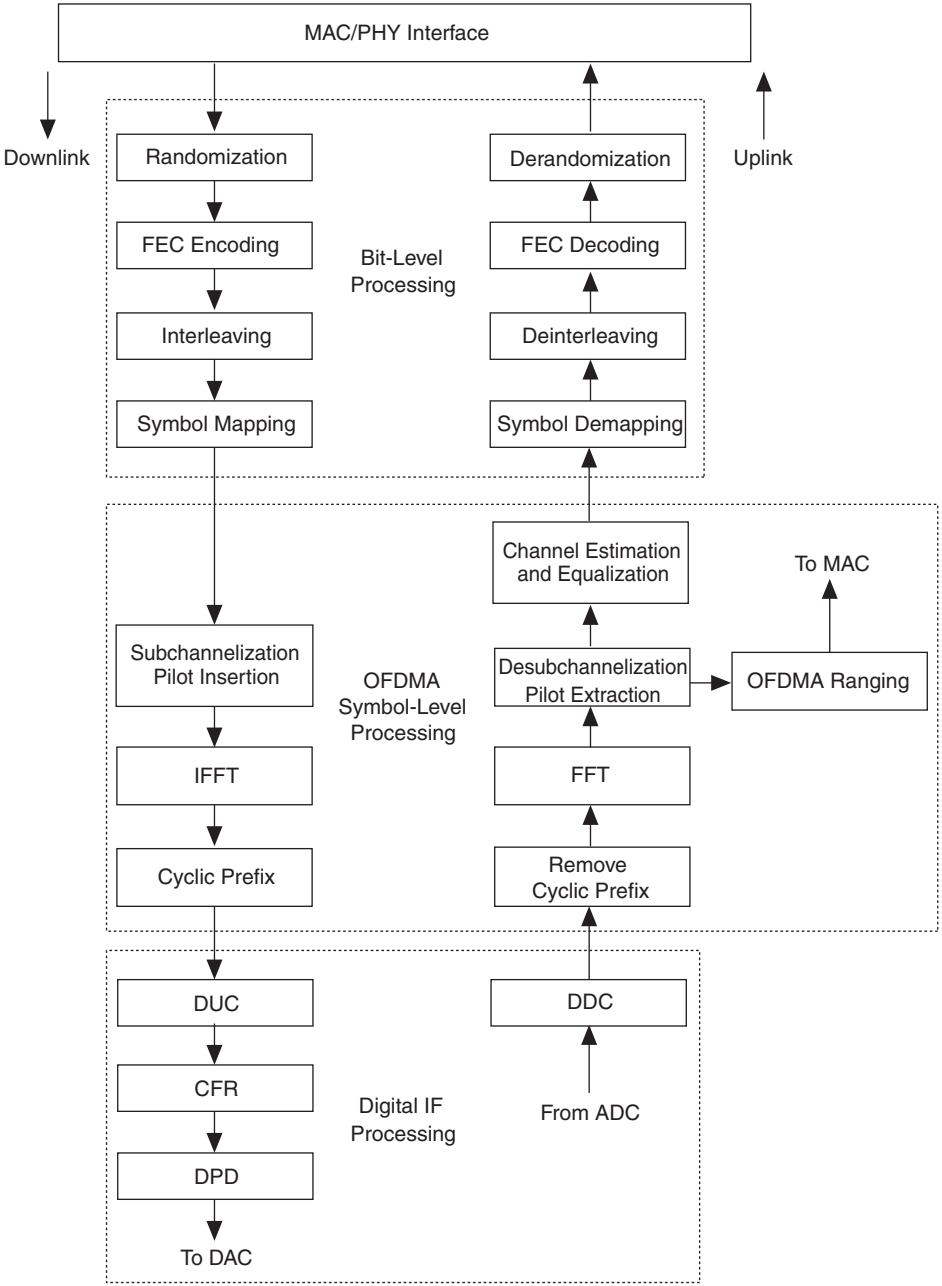
The reference design has the following features:

- Wrapper file that integrates the desubchannelization and ranging modules
- Works for all fast Fourier transform (FFT) sizes (128, 512, 1,024, and 2,048)
- Self-testing RTL testbench
- Four different test case data for each FFT size provided
- ModelSim simulation script
- Quartus® II synthesis script
- Perl script to perform batch RTL simulations

WiMAX Physical Layer

Figure 1 shows an overview of the *IEEE 802.16e-2005* scalable OFDMA physical layer (PHY) for WiMAX basestations.

Figure 1. WiMAX PHY Implementation



Altera's WiMAX building blocks include bit level, OFDMA symbol-level, and digital intermediate frequency (IF) processing blocks. For bit-level processing, Altera provides symbol mapping reference designs and support for forward error correction (FEC) using the Reed-Solomon and Viterbi MegaCore® functions.

The OFDMA symbol-level processing blocks include reference designs that demonstrate subchannelization and desubchannelization with cyclic prefix insertion supported by the fast Fourier transform (FFT) and inverse FFT (IFFT) MegaCore functions. Other symbol-level reference designs illustrate ranging, channel estimation, and channel equalization.

The digital IF processing blocks include single antenna and multi-antenna digital up converter (DUC) and digital down converter (DDC) reference designs, and advanced crest factor reduction (CFR) and digital predistortion (DPD).

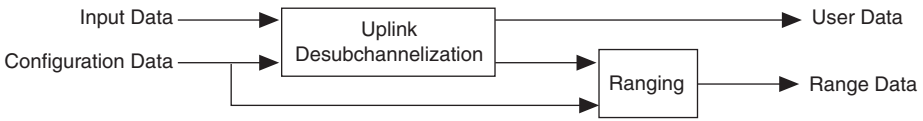
For more information on Altera WiMAX solutions, refer to the following application notes:

- *AN 412: A Scaleable OFDMA Engine for WiMAX*
- *AN 421: Accelerating DUC & DDC System Designs for WiMAX*
- *AN 430: OFDMA Ranging for WiMAX*
- *AN 434: Channel Estimation & Equalization for WiMAX*
- *AN 439: Constellation Mapper and Demapper for WiMAX*
- *AN 451: Downlink Subchannelization for WiMAX*
- *AN 452: An OFDM FFT Kernel for WiMAX*

Functional Description

Figure 2 shows the reference design block diagram.

Figure 2. Block Diagram



The design takes input data from the FFT and some configuration information is fed into the desubchannelization module. The desubchannelization module has two output interfaces: user slot data and the ranging channel data. The user slot data is output from the

integrated system; the ranging channel data is fed into the ranging module. The output from the ranging module forms the second output interface from the integrated system.

Getting Started

This reference design only includes the wrapper and associated scripts.

This reference design requires the following reference designs:

- Uplink desubchannelization reference design
- Ranging reference design
- CORDIC reference design (included with ranging reference design)
- Test data files (included with the desubchannelization and ranging reference designs

For more information on the ranging reference design, refer to *AN 430: WiMAX OFDMA Ranging*; for more information on the uplink desubchannelization reference design, refer to *AN 450: Uplink Desubchannelization for WiMAX*.

This application note assumes you are familiar with *AN 412: A Scalable OFDM Engine for Mobile WiMAX*.

Install the Reference Design

Install the uplink desubchannelization, ranging, and integration of desubchannelization and ranging reference designs.

The reference design installs by default into the **c:\altera\reference_designs** directory, but you can change the default.

Figure 2 shows a high-level view of the directory structure, where <*path*> is the top-level directory, **wimax_ofdma\source\rtl\common\ul_rx**.

Figure 3. Directory Structure

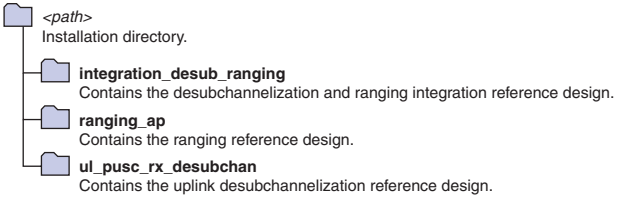


Table 1 describes the files in the **integration_desub_ranging** directory.

Table 1. Files in the integration_desub_ranging Directory

File Name	Directory	Description
integration_desub_ranging.vhd	**\source**	Wrapper file.
integration_desub_ranging_tb.vhd	**\tb**	RTL testbench.
integration_desub_range_msim.tcl	**\scripts**	ModelSim simulation script.
integration_desub_range_batch.pl		Perl batch script for RTL simulations.
integration_desub_range_quartus.tcl		Quartus II Tcl synthesis script.

Simulate the Design

The same testbench simulates all supported FFT sizes of desubchannelization and ranging.

The testbench reads input data and input configuration data from text files (provided with the desubchannelization and ranging reference designs), and feeds them into the integrated system. Also, it writes the user slot data output and ranging output from the integrated system to separate text files. In addition, it checks these outputs with the golden data read from some more text files and logs any differences to log files (one log file for user data and one for ranging data).

The testbench requires all data files (input, output, and expected output) to be located in the **simulation** directory. The simulation script (**integration_desub_range_msim.tcl**) simulates the design in the **\integration_desub_ranging\sim** directory, so you must copy data files to this directory.

The desubchannelization module has different HDL files for each different FFT size.

You must copy the relevant HDL files for each FFT size to be simulated to the **\ul_pusc_rx_desubchan\ul_pusc_rx_process** directory.

The ranging module has the same HDL files for each FFT size. However, it may have different VHDL package files depending on the configuration of the ranging module. Before compilation, the correct versions of **range_io_pkg.vhd** and **range_pkg.vhd** must be present.

For the location of these package files, refer to *AN 430: WiMAX OFDMA Ranging*.

Simulate in the ModelSim Simulator

To simulate in the ModelSim simulator, follow these steps:

1. Copy data text files to the **\integration_desub_ranging\sim** directory.

2. Copy desubchannelization files for the relevant FFT size to **\ul_pusc_rx_desubchan\ul_pusc_rx_process** directory.

3. Ensure the ranging package files **range_io_pkg.vhd** and **range_pkg.vhd** are correct.

4. Open the simulation script **integration_desub_range_msim.tcl** in the **\integration_desub_ranging\scripts** directory in text editor and modify the following lines to match the location of the design on your PC:

```
set proj_topdir "D:/work/WiMax/wimax_ofdma"
set cordic_srcdir "D:/work/cordic/source/verilog"
```

5. To ensure that the waveform viewer is opened in ModelSim with appropriate signals loaded into it, set following variable defined in the script to the appropriate value:

```
set batch_mode 0
```

6. In the ModelSim simulator, execute the simulation script **integration_desub_range_msim.tcl**.

7. After the simulation finishes, view the output and log files in the **\integration_desub_ranging\sim** directory.

Run Automated Batch Mode Simulations

The Perl script **integration_desub_range_batch.pl** in the **\integration_desub_ranging\scripts** directory performs steps 1 through 3 in "Simulate the Design" on page 5, then it opens the ModelSim simulator and runs the simulation. Finally it stores the output files to **\integration_desub_ranging\sim\op** with unique names for each simulation.

It can run simulations for all or some of the four test cases for each FFT size.

To run automated batch mode simulations, follow these steps:

1. Open the simulation script **\integration_desub_ranging\scripts\integration_desub_range_msim.tcl** in a text editor and modify the following lines to match the location of the design on your PC:

```
set proj_topdir "D:/work/WiMax/wimax_ofdma"
set cordic_srcdir "D:/work/cordic/source/verilog"
```

2. To ensure that the ModelSim simulator is run in command mode and the waveform viewer does not open, set the following variable defined in the script to the appropriate value:

```
set batch_mode 1
```

3. Open a Command prompt.

4. Change the directory to **\integration_desub_ranging\scripts**.

5. To provide some basic help on input arguments to running this script, type the following command:

```
integration_desub_range_batch.pl -help ↵
```

For example, **integration_desub_range_batch.pl** runs simulations on all four FFT sizes and all four test cases (16 simulations in total). Also **integration_desub_range_batch.pl n1024 n128 t4 t2** runs simulations on FFT sizes 1,024 points and then 128 points, for test cases four and two.

As the script runs, information is printed to the command window, indicating which files it is copying and their locations.

Examine the Perl script to determine which data files comprise each test case and where they are stored. Alternatively, just run the script and examine the messages printed to the command prompt window.

Synthesize the Design

To synthesize the design, follow these steps:

1. Open the synthesis script **\integration_desub_ranging\scripts\integration_desub_range_quartus.tcl** in a text editor. Modify the following lines:

   - `set fftsize 1024`
   - `set proj_topdir "D:/work/WiMax/wimax_ofdma"`

- `set cordic_srcdir "D:/work/cordic/source/verilog"`
- `# set to one if Quartus S/W is earlier than Quartus 6.1`
- `set pre_quartus61 1`

The script automatically uses the appropriate uplink desubchannelization files depending on the `fftsize` setting.

2. Ensure the ranging package files **range_io_pkg.vhd** and **range_pkg.vhd** are correct.

3. In the Quartus II software execute the Tcl script.

Synthesis files are stored in the **\integration_desub_ranging\build** directory.

As the integration of the uplink desubchannelization and ranging modules is glueless, you can assume the synthesis results are the summation of the synthesis results from the individual modules. Also, the $f_{MAX}$is the slowest of the two modules.

Revision History

Table 2 shows the revision history for this application note.

Table 2. Revision History

Version	Date	Description
1.0	February 2007	First release.

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