Cyclone II DDR2 SDRAM Demonstration

April 2005, ver 1.0 Application Note 383

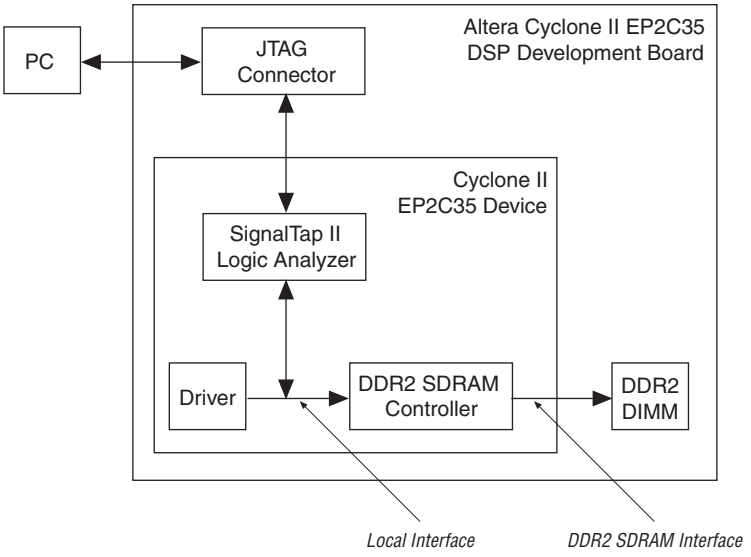
Introduction

This application note describes a 167-MHz DDR2 SDRAM demonstration on an Altera® Cyclone™ II EP2C35 DSP Development Board.

The Altera Cyclone II EP2C35 DSP development board provides a low-cost hardware platform for developing high performance DSP designs based on Altera Cyclone II FPGA devices and interfaces to a DDR2 SDRAM. This application note describes how to run a pregenerated Quartus® II project that demonstrates a DDR2 SDRAM interface operating at 167 MHz. This application note also details how to modify the demonstration project, and how the demonstration was created so you can create a custom DDR2 interface.

Figure 1 shows the demonstration overview.

Figure 1. Demonstration Overview



A PC running the Quartus II software downloads the device programming file and monitors the activity on the DDR2 SDRAM interface.

The Quartus II SignalTap® II utility captures the activity on the DDR2 SDRAM Controller local interface via the JTAG connector.

The driver is a self-checking test generator for the DDR2 SDRAM controller. It uses a state machine to write data patterns to a range of column addresses, within a range of row addresses in all memory banks. It then reads back the data from the same locations, and checks that the data matches. The `inv_pnf` (inverted pass not fail) output transitions high if any read data fails the comparison. There is also an `inv_pnf_per_byte` output, which shows the comparison on a per byte basis. The `test_complete` output transitions high for a clock cycle at the end of the write then read sequence. After this transition the test restarts from the beginning.

The data patterns are generated with an 8-bit linear feedback shift register (LFSR) per byte—each LFSR has a different initialization seed.

This application note includes the following steps:

Before You Begin

This application note requires the following hardware and software:

- Altera Cyclone II EP2C35 DSP Development Board
- Board power supply and cable
- An Altera USB-Blaster™ JTAG programming cable
- DDR2 SDRAM Controller MegaCore® function v3.2.0 (for "Modify the Demonstration Project" on page 6 only)
- A PC running the Windows NT/2000/XP operating system
- Quartus II software version 5.0

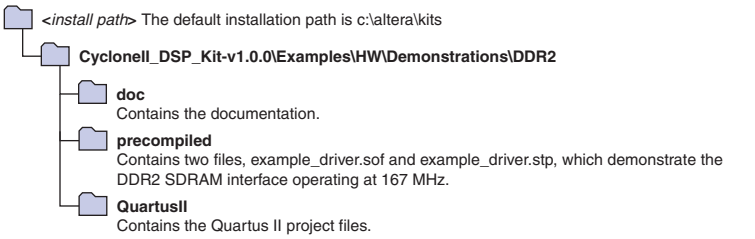
The Altera Cyclone II EP2C35 DSP Development Board is part of the DSP Development Kit, Cyclone II Edition.

For more information on the DDR2 SDRAM Controller MegaCore function, see the *DDR & DDR2 SDRAM Controller Compiler User Guide*.

Before you run the demonstration, follow these steps:

1. Install the DSP Development Kit, Cyclone II Edition, which installs the **DDR2** directory on your PC. Figure 2 shows the directory structure.

Figure 2. Directory Structure



2. Connect the USB-Blaster™ download cable between the Altera Cyclone II EP2C35 DSP Development Board connector J9 and the PC.

3. Connect the power supply to J1 (9 to 20-V DC input on the board).

Run the Demonstration

To run the demonstration, follow these steps:

1. Start the Quartus II software

2. Choose **Open** (File menu).

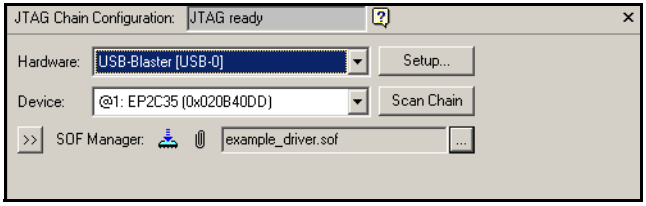
3. Browse to the **DDR2\precompiled** directory and choose **example_driver.stp**.

4. Click **Open**.

5. Choose your appropriate programming hardware (see Figure 3).

If you do not have the appropriate driver software installed, see the Altera website **www.altera.com/support/software/drivers**.

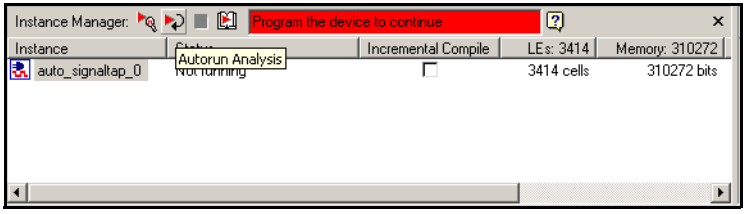
Figure 3. Choose the Programming Hardware



6. Click the **Program Device** icon, to download the **.sof** file to the board.

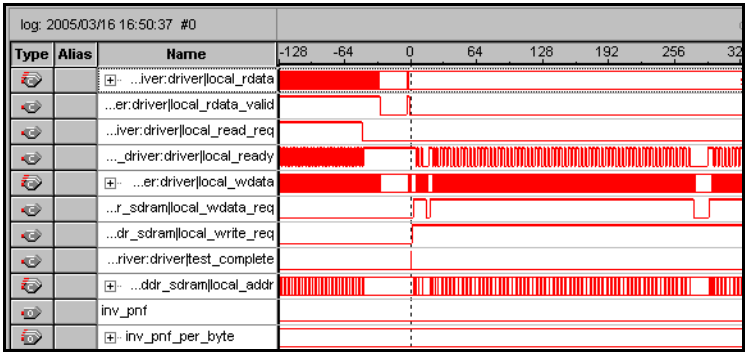
7. To monitor the transactions on the DDR2 interface, click **Autorun Analysis** (see Figure 4).

Figure 4. Click Autorun Analysis



Ensure the inv_pnf signal is continuously low (see Figure 5).

Figure 5. Monitor Transactions



You can zoom in and out with the SignalTap II capture tool to see the writes successfully read back.

The following indicators on the board show the demonstration is running:

- LED0 flashes when inv_pnf is low
- LED7 illuminates when test_complete is high
- The 8-segment LED illuminates when inv_pnf_per_byte is low

Conversely:

- When inv_pnf is high, LED0 does not illuminate or flash
- When test_complete is low, LED7 does not illuminate
- When inv_pnf_per_byte is high, the 8-segment LED does not illuminate

The demonstration is complete—you are now watching the 167-MHz DDR2 SDRAM interface operating. Zoom in on the local_wdata and local_addr signals, to see the data and address changing on each clock cycle. The cycles refer to capture cycles and are based on the SignalTap II clock setting, which is set to the_ddr2_core_example_driver:driver|clk (the PLL c0 output). The PLL has a 100-MHz input clock and a 166.6-MHz output clock. With these PLL settings the address and data changes on each cycle must occur at 167 MHz.

Modify the Demonstration Project

To modify the demonstration project, follow these steps:

1. Choose **Programs > Altera > Quartus II** <*version*> (Windows Start menu) to run the Quartus II software. You can also use the Quartus II Web Edition software.
2. Choose **Open Project** (File menu).
3. Browse to the **DDR2\QuartusII** directory, choose **example_driver.qpf**, and click **Open**.
4. Choose **MegaWizard Plug-In Manager** (Tools menu).
5. Select **Edit an existing custom megafunction variation**.
6. Click **Next**.
7. Choose **the_ddr2_core.vhd** and click **Next**. IP Toolbench launches.
8. Click **Step 4: Generate** (see Figure 6).

Figure 6. Step 4: Generate

9. On the **File overwrite/conflict warning**, click **OK**.

10. Click **Exit** to exit IP Toolbench.

11. Copy and paste the **the_ddr2_core_example_driver.vhd** file from the **DDR2\QuartusII\keep** directory to the **DDR2\QuartusII** directory.

    This file is rewritten every time you click **Generate** in IP Toolbench. The file in the **\keep** directory has edits to the address range in the example driver to increase the address range.

12. Choose **Start Compilation** (Processing menu).

When the compilation finishes, you have the same complete project that is in the **\precompiled** directory.

For instructions on downloading the **.sof** file to the board, see "Run the Demonstration" on page 3.

101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
www.altera.com
Applications Hotline:
(800) 800-EPLD
Literature Services:
literature@altera.com