Using Stratix GX Transceivers for CPRI

Introduction

Common Public Radio Interface (CPRI) is a protocol specification for the high-speed serial link between the radio equipment (RE) and the radio equipment controller (REC). The data rates specified are 614 megabits per second (Mbps), 1.228 gigabits per second (Gbps), and 2.4576 Mbps with 8B/10B encoded data. The Stratix® GX transceiver has dedicated circuitry that enables it to fully support the CPRI protocol.

Stratix GX Transceiver Settings for CPRI

You set the Stratix GX transceiver options for CPRI through the MegaWizard® Plug-In Manager in the Quartus® II software. This application note describes the `altgxb` megafunction settings that are required for CPRI support or are used in the Altera® CPRI reference design. This application note does not describe configuration settings that are not specific to CPRI.

See the *Stratix GX Transceiver User Guide* section of the *Stratix GX Device Handbook, Volume 2* for more information on those settings.

To launch the wizard in the Quartus II software, follow these steps:

1. Choose the **MegaWizard Plug-In Manager** (Tools menu). The **MegaWizard Plug-In Manager** dialog box appears.

2. Specify that you want to create a new custom megafunction variation and click **Next**.

3. Choose the device family you are using (in this case, Stratix GX).

4. From the list of megafunctions, choose **ALTGXB** (from the Installed Plug-ins> I/O directory).

5. Choose the output file type for your design. The wizard supports AHDL, VHDL, and Verilog HDL.

6. Specify a name for the output file, *<directory name>\<variation name>*. Click **Next**.

The first page of the `altgxb` megafunction configuration (Figure 1) appears.

Figure 1. MegaWizard Plug-In Manager - ALTGXB (page 3 of 9) - General (1)
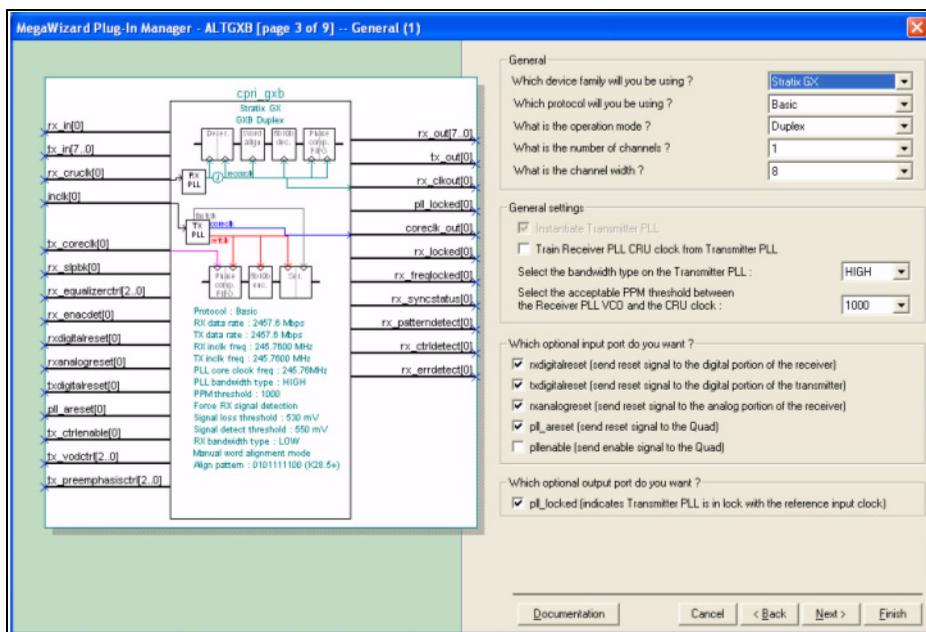
The Stratix GX device CPRI configuration uses the basic protocol mode because it provides 8B/10B encoding across the needed data rates in a single channel configuration. The Altera CPRI reference design uses a single duplex channel with an 8-bit data width. However, you can change the number of channels and the data width to suit your design requirements. The reference design uses the 8-bit transceiver data width because it is easier to construct a dynamically sizable bus-width interface to the altgxb block as outlined by the CPRI specification for automatic negotiation of the link data rate.

For CPRI usage, the **Train Receiver PLL CRU clock from Transmitter PLL** option can either be on or off, (the CPRI data rates do not require the transmitter PLL output to exceed 350 MHz). This option allows you to train the clock recovery unit (CRU) separately from the transmitter PLL. This is beneficial if the output of the transmitter PLL exceeds the 350 MHz phase-frequency detector (PFD) limit on the receiver PLL. The Altera CPRI reference design has this option turned off because this is a legacy feature on earlier test designs.

All the reset signals were selected and used by the reset sequence state machine. The reset sequence prevents the pointers in the phase-compensation FIFO from moving when the PLLs are not yet locked.

See the *Stratix GX Transceiver User Guide* section of the *Stratix GX Device Handbook, Volume 2* for additional information about the reset state machine.

Figure 2 shows the second page of the ALTGXB MegaWizard Plug-In Manager configuration.

Figure 2. MegaWizard Plug-In Manager - ALTGXB (page 4 of 9) - General (2)
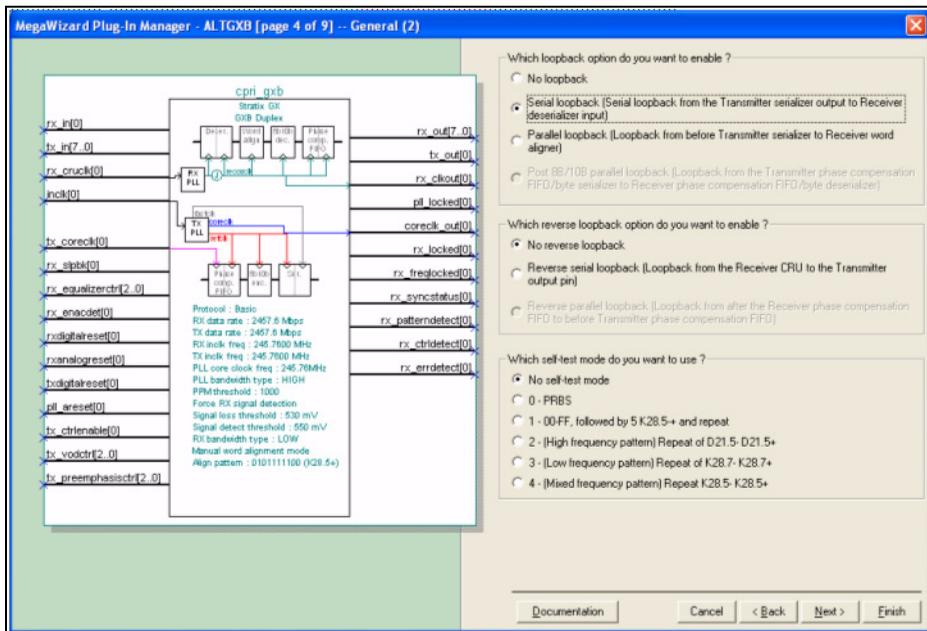
Loopback and self test are not required to implement CPRI. The reference design uses serial loopback to validate functionality with a single link.

See the *Stratix GX Transceiver User Guide* section of the *Stratix GX Device Handbook, Volume 2* for information about these options.

Figure 3 shows the settings for the 8B/10B decoder and word aligner.

Figure 3. MegaWizard Plug-In Manager - ALTGXB (page 5 of 9) - Receiver (1)
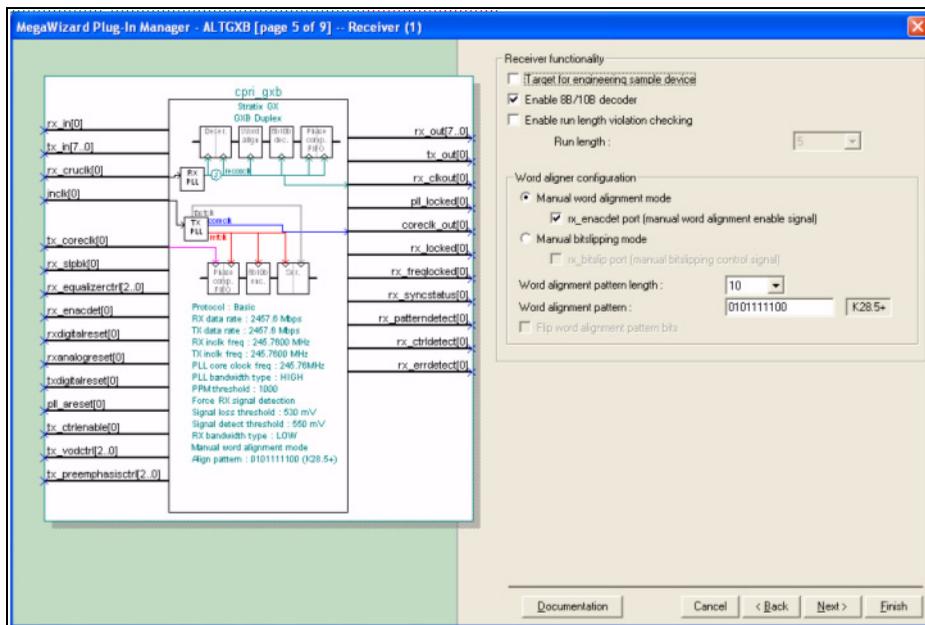
The 8B/10B decoder for the receiver provides proper decoding for the CPRI protocol. If you do not turn on this option, you must create an 8B/10B decoder in the PLD core to properly decode the data stream.

The word aligner aligns to the K28.5 comma character and recognizes positive and negative disparity commas automatically, as long as the `rx_enacdet` port is used and is tied high (`1'b1` on `rx_enacdet`). If the `rx_enacdet` port is not used, the word aligner does not align to the comma. Altera recommends that you keep the `rx_enacdet` port tied to `1'b1` because the K28.5 code group does not appear between any valid code group boundaries.

☞ It is not necessary to turn on the **Enable run length violation checking** option. The maximum run length with 8B/10B encoding is 5.

Figure 4 shows the page where you set the data rate for the Stratix GX device and for CPRI configuration.

Figure 4. MegaWizard Plug-In Manager - ALTGXB (page 6 of 9) - Receiver (2)
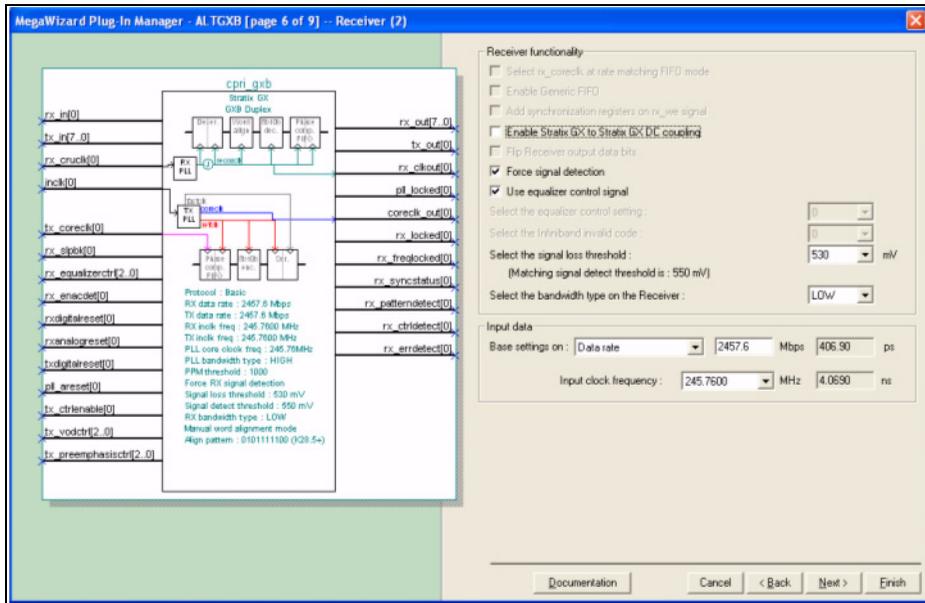
The data rate for the Altera CPRI reference design is set at 2.4576 Gbps to accommodate the three data rates specified for CPRI. You can change the data rate to 614.4 Mbps or 1.2288 Gbps, depending on your design requirements. The data-rate setting optimizes the transceiver PLL to operate at the specified data rate. It is possible to support multiple data rates for a given setting. In the reference design, the reference clock for a data-rate setting of 2.4576 Gbps was set at 245.76 MHz. To support 1.2288 Gbps, change the reference clock frequency to 122.88 MHz. You can use a reference clock of 61.44 MHz to support 614.4 Mbps. There may be an increase in jitter if the operational data rate differs from the specified data rate in the MegaWizard Plug-In Manager. For example, with a specified data rate of 2.4576 Gbps in the wizard, operating at 614.4 Mbps yielded a jitter increase of approximately 30 ps, as measured with the Stratix GX demonstration board, compared to a data-rate setting of 614.4 Mbps. Altera recommends that you ensure your system can toleratee the increase in jitter. The Altera CPRI reference design, operating at 614.4 Mbps with a data rate setting of 2.4576 Gbps, did not encounter any bit errors when going between two Stratix GX development boards through approximately 1 m of SMA cables.

When using the 2.4576 Gbps setting for lower data-rate support, only the reference clock must change. The reference design example uses the enhanced PLL (EPLL) in dynamic reconfiguration mode to provide the

245.76 MHz, 122.8 MHz, or 61.4 MHz reference clock for the transceiver PLLs. However, the output of the EPLL might violate the CPRI specification for reference clock jitter. You can use an external VCXO PLL after the EPLL to reduce the amount of jitter of the reference clock.

The dynamic equalizer control port is not required to implement CPRI on a Stratix GX device, but you can use it as an optional port to dynamically change the equalization setting of the receiver. The Altera CPRI reference design uses the dynamic control port to provide flexibility to the link. The equalization control for the RE and REC is given to the upper layers and uses the in-band CPRI Vendor Specific control space to communicate equalization settings across the link. If your design requires a specific equalization value, turn off the **Use equalizer control signal** option and set the equalizer settings statically (see Figure 4) in the MegaWizard Plug-In Manager.

You set the optional output ports for the receiver on the page shown in Figure 5.

☞   The optional input ports are not required for CPRI and are not used in the reference design.

Figure 5. MegaWizard Plug-In Manager - ALTGXB (page 7 of 9) - Receiver (3)
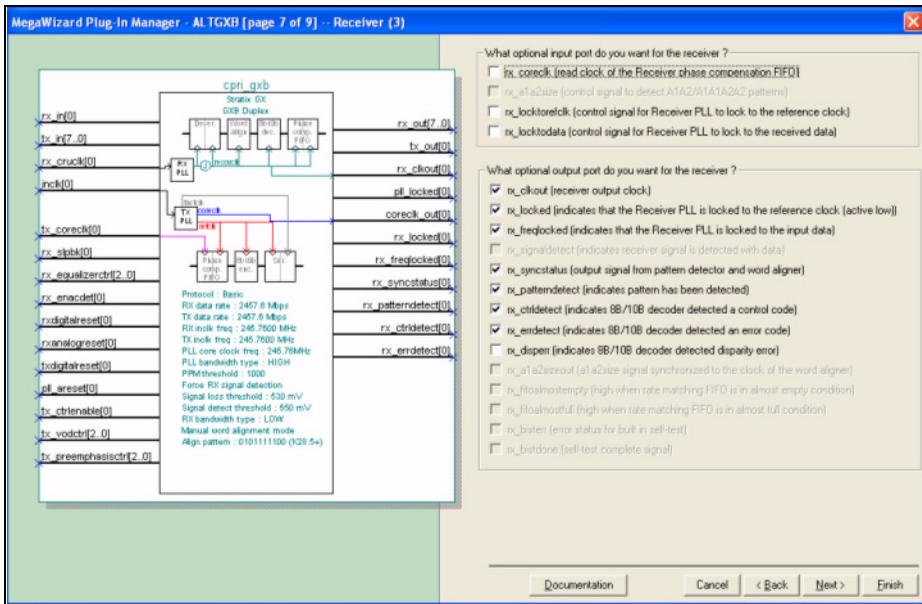
Altera recommends that you use the `rx_clkout` port to carry the recovered clock from the receiver channel to the PLD core. This clock clocks a phase-compensation FIFO to decouple the PLD clock domain from the recovered clock domain.

The `rx_locked` port is optional and indicates when the receiver PLL is locked to the reference clock. This signal toggles when the receiver is locked to the reference clock. The Altera CPRI reference design does not use this port.

Altera recommends that you use the `rx_freqlocked` port to indicate when the receiver is in lock-to-data mode. This port is used in the Altera CPRI reference design in the reset state machine.

See the *Stratix GX Transceiver User Guide* section of the *Stratix GX Device Handbook, Volume 2* for additional information about the reset state machine.

The `rx_syncstatus` and `rx_patterndetect` ports are outputs of the word aligner and indicate when the word aligner is aligned to the word alignment pattern and when the pattern is detected in the current word boundary. Altera recommends that you use these ports for CPRI operations because the indicators can be used to transition between states in a startup state machine and to detect if start-of-frame occurs in the expected time frame. The Altera CPRI reference design uses both these ports in the startup state machine as well as the loss-of-frame (LOF) logic for LOF indication.

Altera recommends that you use the `rx_ctrldetect` port if you use the 8B/10B decoder. The `rx_ctrldetect` port indicates which received 8B/10B codes are data (Dx.y) and which codes are control words (Kx.y).

Altera recommends that you use the `rx_errdetect` port for CPRI operations. This port indicates when there is an 8B/10B code violation that includes invalid code groups and disparity errors. The CPRI specification requires the detection of bad code groups to trigger a loss of signal (LOS) state. Because the CPRI specification does not require the differentiation of invalid code group errors from disparity errors, the `rx_errdetect` is sufficient and the `rx_disperr` port is not necessary.

For more information on the operation of these ports, see the *Stratix GX Transceiver User Guide* section of the *Stratix GX Device Handbook, Volume 2*.

Figure 6 shows the page where you set the transmitter functionality.

Figure 6. MegaWizard Plug-In Manager - ALTGXB (page 8 of 9) - Transmitter
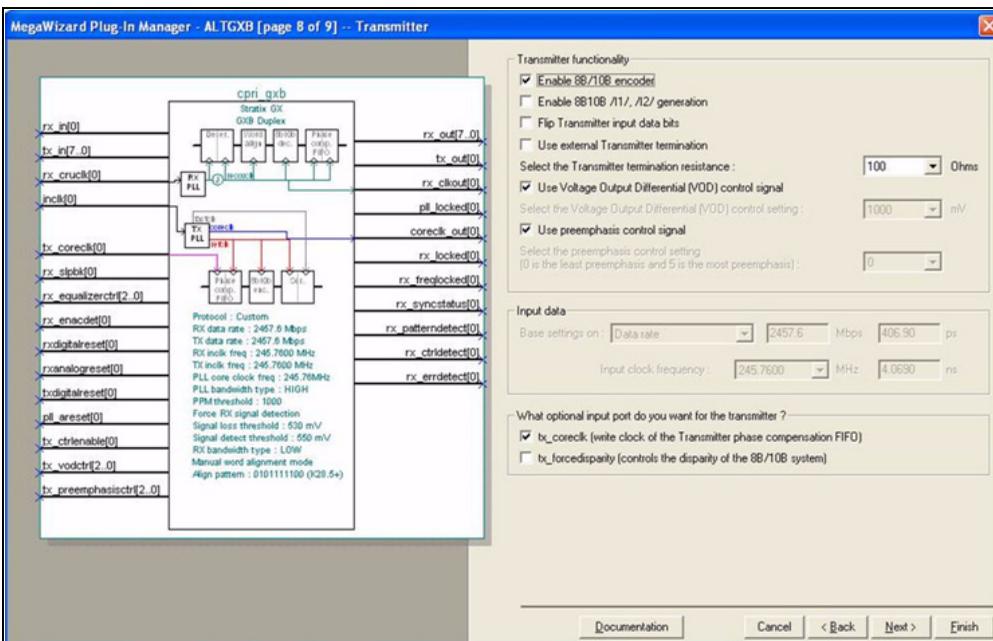
You must turn on the **Enable 8B/10B encoder** option for the transmitter to provide proper encoding for the CPRI protocol. If you do not turn on this option, you must create an 8B/10B encoder in the PLD core to properly encode the data stream.

The dynamic V_{OD} and pre-emphasis controls are not required for CPRI implementation, but can be used an optional port to dynamically alter the transmitter output characteristics. The Altera CPRI reference design uses the dynamic control port and gives the upper layers the ability to control V_{OD} and pre-emphasis on the fly. The CPRI Vendor Specific control space communicates these settings across the link. If your design requires a specific V_{OD} or pre-emphasis value, you can turn off the **Use Voltage Output Differential (VOD) control signal** and **Use preemphasis control signal** options and set these values statically.

Figure 7 shows the final page of the ALTGXB megafunction MegaWizard Plug-In Manager. This page lets you choose the output files you require. The Variation file is required.

Figure 7. MegaWizard Plug-In Manager - ALTGXB (page 9 of 9) - Summary

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