Stratix II Device System Power Considerations

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Introduction

Altera developed Stratix® II devices using a 90-nm process technology optimized for performance and power. New challenges accompany the introduction of 90-nm devices. In addition to the usual core power and I/O power, 90-nm devices dissipate a larger leakage power compared with previous process technology devices. This leakage power can be a significant contributor to device power dissipation. To avoid excessive power leakage, Stratix II devices use low leakage transistor technology wherever possible to reduce power loss due to standby current. This application note addresses these items along with a comprehensive power management strategy.

Power Components

The total power consumed by the Stratix II device and the termination networks is comprised of the standby power, dynamic power, and I/O power.

total power = standby power + dynamic power + I/O power

The standby power is determined by the I_{CCINT} current required by the device when it is in standby. The dynamic power is the power the device consumes through internal switching (charging and discharging capacitance at internal nodes). The I/O power is the power consumed by external switching (charging and discharging external load capacitance connected to device pins) and the termination network.

Standby Power

The device consumes power during standby due to leakage currents. The amount of leakage current varies with die size, temperature, and process variations. Standby power is simulated before device characterization and is automatically determined. It is defined in two categories: typical and worst-case power.

You do not need to enter a standby power value into the Power Calculator tool. See *Stratix II Design Utilities: Power Calculator* for more information.

Dynamic Power

Internal nodes changing logic levels causes device internal power consumption. Power is required to charge and discharge the capacitance on each node to change its state (e.g., from a logic 0 to logic 1). This power term is called dynamic because it is the power required for states to change within the device logic array.

Dynamic power includes both the load power and the adaptive logic module (ALM) power. The ALM power is consumed internally by the cell primitives. This accounts for the power required to charge and discharge the ALM capacitance. Load power represents the currents required to charge and discharge the external load capacitance driven by each ALM.

Altera has developed a power model to allow you to calculate the estimated power your design will consume before you program a device. Power estimation is based on simulation and initial characterization data of the architectural features, including:

- RAM blocks (M512, M4K, and M-RAM blocks)
- DSP blocks
- Enhanced and fast phase locked loops (PLLs)
- ALMs
- Global, regional, and fast clock networks
- HSDI receivers and transmitters

Each feature may be used multiple times by design modules. Module power is first summed as total power per feature. The total dynamic power is calculated by multiplying the V_{CCINT} by the sum of the usage of each architectural feature listed above.

$$\text{Dynamic power} = V_{CCINT} \times I_{CCINT}$$

Device power calculation is based on the utilization of each of these features within the device. The Stratix II power calculator uses a detailed algorithm to estimate device power as part of the FPGA design creation process.

Contact Altera® Applications for more information on the Stratix II power calculator.

Altera devices use equivalent capacitance values for the devices to calculate power. These values are based on the sum of multiple capacitances. For example, you would add up the capacitance for the pin, trace, and package for a signal that drives an input or output. This general equation is useful if internal switching frequencies are accurately

determined. Altera uses a set of approximation curves (based on characterization data) to determine the internal switching frequencies. These graphs provide an estimate of active power for most designs.

Estimating the total power consumed by all of a device's blocks and elements takes into account the maximum switching frequency of the item, estimated toggle rates, fanouts to connected circuits, and constants related to each module obtained through device characterization. These considerations are included in the power model. See *Stratix II Design Utilities: Power Calculator* for more information.

I/O Power

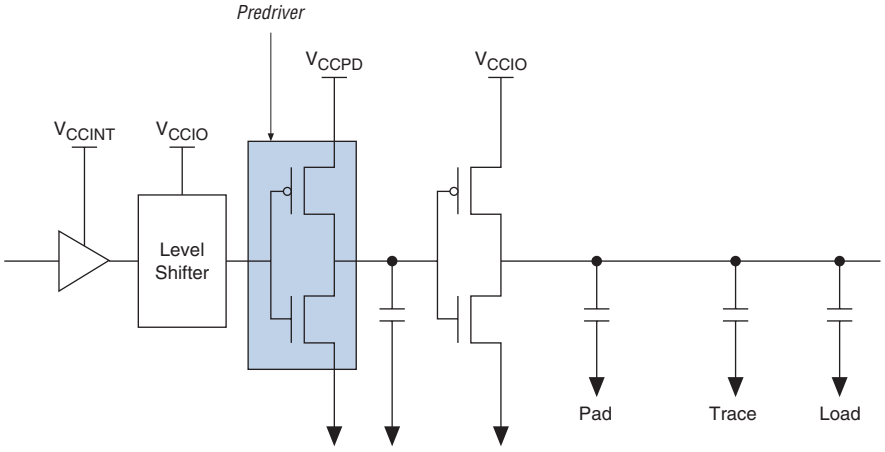
I/O power is the V_{CCIO} power. It is dissipated due to the charging and discharging of external load capacitors connected to the device pins, and includes the termination network. You can calculate a device's I/O power with the following equation:

> I/O power = (number of driven outputs × power dissipation constant) + 0.5 × (capacitance of the device package and associated pad or pin + capacitive load) × output voltage swing for I/O standard × f_{MAX} × (toggle rate/1,000) × V_{CCIO}

The number of driven outputs includes bidirectional outputs.

This equation does not include other elements of the I/O buffer which are also powered by V_{CCIO}, including the I/O element (IOE) registers, I/O predrivers, level shifters, and pad and package capacitance. Figure 1 shows a model of the I/O buffer.

Figure 1. Stratix II I/O Buffer



Thermal Management

Thermal issues determine device reliability. The items that control the temperature of the device include standby power, power dissipation, external capacitive loading, total power dissipation in the device, thermal resistance, ambient temperature, and airflow. These items must be managed to maintain junction temperature (T_j). This section discusses the power concerns that must be managed to improve thermal issues and device reliability, including standby power, power dissipation, and external capacitive loading.

Standby Power

In 90-nm devices, the leakage current can be significant and is proportional to the die size because it depends on the number of transistors in the device. Leakage power is an exponential function of T_j. High leakage increases T_j, which, in turn, further increases the leakage, forming a potential positive feedback loop.

$$T_j = T_a + \theta_{ja} \times (\text{standby power} + \text{dynamic power})$$

T_a is the ambient temperature, and θ_{ja} is the thermal resistance between the device junction and ambient air. Ensure that the junction temperature remains within its operating range and does not enter a positive feedback loop.

For more information on standby power and the junction temperature operating range, see the *DC & Switching Characteristics* chapter in the *Stratix II Device Handbook.*

External Capacitive Loading

The internal capacitance is associated with the power dissipated by the device. The external capacitance is associated with power dissipated outside the device. You cannot control the internal capacitance However, the external capacitance is usually a function of printed circuit board (PCB) trace loading and other IC loads, which are constrained by other aspects of the design. You should keep external capacitive load to a minimum where possible.

Other Power Requirements

This section provides information on other power requirements.

V_{CCPD}

V_{CCPD} is a separate, small load current power supply for predrivers as well as configuration and JTAG I/O buffers. Refer to the *DC & Switching Characteristics* chapter in the *Stratix II Device Handbook* for the V_{CCPD} specification.

Inrush Current

Inrush current is the initial current that goes to the device when you power it up. At power-up, a minimum level of logic array current (I_{CCINT}) must be provided to the Stratix II device. Furthermore, the V_{CCINT} ramp time must be between 100 µs and 100 ms. The amount of time the system requires to ramp V_{CCINT} up depends on the amount of current available from the power supply. If more current is available, V_{CCINT} can ramp up faster. When the voltage reaches 90% of its typical value, the initial high current is no longer required. The inrush current varies inversely with the temperature of the device. As device temperature increases, although the standby power also increases, the inrush current available when you power up the device decreases.

Configuration Power

Configuration power is the power required to configure the device. During initialization, the device requires power to reset registers, enable I/O pins, and enter operating mode. The I/O pins are tri-stated during power-up, both before and during configuration to conserve power and prevent the I/O pins from driving out during this time.

Connect V_{CCPD} to 3.3 V in order to power the 3.3-V/2.5-V buffer available on the configuration input and JTAG pins. V_{CCPD} applies to all the JTAG pins and some configuration pins. V_{CCPD} must ramp-up from 0.0 to 3.3 V within 100 ms. If V_{CCPD} does not ramp up within the specified time, the Stratix II device may not configure successfully. If the system does not allow for a V_{CCPD} ramp-up time of 100 ms or less, `nCONFIG` must be held low until all power supplies are stable.

See the *Configuring Stratix II Devices* chapter in Volume 2 of the *Stratix II Device Handbook* for more information about configuration schemes in Stratix II devices as well as which configuration pins the V_{CCPD} voltage applies to.

Bypass Considerations

Proper power bypassing and decoupling improves the overall signal integrity, which is important for reliable designs. When a logic device changes state (e.g., switches from a logic 1 to a logic 0), the output structure is momentarily at a low impedance across the power supply. When the voltage on a signal changes, the transition requires a signal line to charge or discharge. When this occurs, a current must be available immediately on the signal line to reach the voltage. The bypass capacitor provides local energy storage for this current.

The transient response for this energy storage system must cover a large range. Small capacitors with low series inductance can provide fast current for the high-frequency transitions. Large capacitors continue to supply current after the high-frequency capacitors have been depleted. Designs require capacitors in three ranges (0.001 to 0.1 µF, 47 to 100 µF, and 470 to 3,300 µF) with frequencies ranging from 1 KHz to 500 MHz.

The amount of logic used in the device and the output switching requirements define decoupling requirements. Additional decoupling capacitance is needed as the number of I/O pins and the capacitive load on the pins increases. Connect as many 0.2-µF power-supply decoupling capacitors as possible to the V_{CCINT}, V_{CCIO}, and ground pins or planes. These capacitors should be located as close as possible to the Stratix II device. Decouple each V_{CCINT} or V_{CCIO} and ground pin pair with a 0.2-µF capacitor. If your design uses high-density packages (e.g., ball grid array (BGA) packages), you may not be able to use one decoupling capacitor per V_{CCINT} or V_{CCIO} and ground pin pair. In this case, you should use as many decoupling capacitors as possible. Decoupling capacitors should have a good frequency response, such as monolithic-ceramic capacitors.

Capacitor Choice & Placement

Proper placement is very important for high-frequency capacitors (0.1 to 0.001 µF low inductance ceramic chip). Keep the trace lengths as short as possible to reduce the inductance in the path from capacitor terminals to the Stratix II power pins. This includes paths that go through a solid ground or power plane (V_{CCINT} or V_{CCIO}) because the inductance of one inch of solid copper plane is about 1 nH. Route bypass capacitor vias directly to the ground, V_{CCINT}, or V_{CCIO} plane.

Low-frequency capacitors (47- to 100-µF medium-frequency and 470- to 3,300-µF low-frequency capacitors) are referred to as "bulk" capacitance and can be mounted anywhere on the board. However, Altera recommends mounting them as close to the device as possible.

Place V_{CCINT} or V_{CCIO} high-frequency bypass capacitors within one centimeter of the associated V_{CCINT} or V_{CCIO} pin on the PCB. Place V_{CCINT} or V_{CCIO} medium-frequency bypass capacitors within 3 cm of the V_{CCINT} or V_{CCIO} pins.

V_{CCINT} Bypass Calculations

The Stratix II logic array voltage can be subjected to very small, short-duration currents (< 50 ps). Although these currents are small, when you add them up for the architectural features utilized across the entire device, they can add up to many amperes of current. Since there are a lot of individual switches, bypass calculation is based on an average energy storage requirement. Use the following equation to determine this requirement for the high-frequency capacitors:

$$\text{Logic array power} = \text{equivalent switched logic array capacitance} \times (V_{CCINT})^2 \times \text{clock frequency}$$

or

$$\text{Equivalent switched logic array capacitance} = (\text{logic array power})/((V_{CCINT})^2 \times \text{clock frequency})$$

The equivalent switched logic array capacitance is the equivalent switched capacitance of the entire Stratix II logic array powered by V_{CCINT}. In order to reduce the V_{CCINT} noise, the bypass capacitor must be much larger than the equivalent switched logic array capacitance. The high-frequency bypass capacitors should be 25 to 100 times larger than the equivalent switched logic array capacitance. A factor of 50 will result in a 2% variation of V_{CCINT}.

High-frequency bypass capacitance = <*25 to 100*> × equivalent switched logic array capacitance

Every V_{CCINT} and ground pin pair must have a high-frequency bypass capacitor. To determine the optimum size of each high-frequency bypass capacitor, divide the total high-frequency bypass capacitance by the number of V_{CCINT} pins on the device, and round up to the next commonly available value.

Thus, the minimum size of each high-frequency V_{CCINT} capacitor is:

Capacitor size
= (<*25 to 100*> × equivalent switched logic array capacitance)/number of V_{CCINT} pins
= (<*25 to 100*>/number of V_{CCINT} pins) × logic array power / $(V_{CCINT})^2$ × clock frequency

For example, if the device consumes 5 W, the logic array voltage is 1.2 V, the system clock frequency is 150 MHz, the high-frequency bypass capacitor multiplier is 50, and the design uses 36 V_{CCINT} pins, then the capacitor size should be 0.032 µF. This is the minimum size for the capacitor, and you should select a capacitor that is at least this large.

The medium-frequency capacitors should be tantalum capacitors from 47 to 100 µF. If tantalum is not available, you can use a low-inductance aluminum electrolytic capacitor. Stratix II devices require at least four medium-frequency capacitors mounted within 3 cm of the device. In addition, place at least one low frequency capacitor (470 µF to 3300 µF) on the PCB.

V_{CCIO} Bypass Calculations

Stratix II I/O bypass requirements are based on an average energy storage requirement. The loads driven by the Stratix II device determine the size of the equivalent switched capacitance. Since different I/O banks can operate at different voltages, you must design bypassing networks individually. Use the following equations to determine the requirement for high-frequency capacitors.

In order to reduce the amount of V_{CCIO} noise, the bypass capacitance must be greater than the load capacitance. The high-frequency bypass capacitance should be 25 to 100 times the load capacitance:

Every V_{CCIO} and ground pair should have a high-frequency bypass capacitor to provide immediate current needs when the system has a large current draw. Use the following equations to determine the optimum size of each capacitor.

equivalent switched I/O capacitance (one bank or voltage level) = number of loads × value of load of one bank or voltage level

high-frequency I/O capacitance = <*25 to 100*> × equivalent switched I/O capacitance

capacitor size
= (<*25 to 100*> × high-frequency I/O capacitance)/number of V_{CCIO} pins in the bank
= (<*25 to 100*>/number of V_{CCIO} pins) × number of signals driven × high-frequency I/O capacitance

For example, if the system drives 40 signals, the equivalent switched I/O capacitance is 10 pF, the high-frequency bypass capacitor is 50 times larger than the equivalent switched logic array capacitance, and the bank has five V_{CCIO} pins, then the capacitor size should be 0.004 µF. This is the minimum size for the capacitor, and you should select a capacitor that is at least this large. The next larger available capacitor size should be chosen (0.047 or 0.01 µF).

Select the medium-frequency capacitors (47 to 100 µF) next. You need one middle-frequency capacitor for every two V_{CCIO} banks. If tantalum capacitors are not available, you can use low-inductance aluminum electrolytic capacitors. Place these capacitors within 3 cm of the V_{CCIO} pins.

In addition, place at least one low-frequency capacitor (470 to 3,300 µF) on the PCB for each V_{CCIO} voltage level.

Conclusion

This document presented power considerations for the Stratix II 90-nm devices. An additional power component, standby power, was discussed along with its effect on the thermal system. The application note also discussed the calculation of key power parameters, giving attention to proper bypass capacitor solutions for applications.

Stratix II devices are created on 90-nm process technology that provides fast performance and high logic density. This new process technology also creates new challenges with power usage and leakage power. Altera has analyzed these power requirements and provides designers with accurate methods to estimate power usage for Stratix II designs.

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