ASI Demonstration

April 2006, version 2.0 Application Note

Introduction

A digital video broadcast asynchronous serial interface (DVB-ASI) is a serial data transmission protocol that transports MPEG-2 packets over copper-based cables or optical networks. DVB-ASI is used as a serial link between equipment in broadcast facilities.

The Altera® ASI demonstration demonstrates how to use Cyclone™ devices to transmit and receive packets over an ASI. The demonstration is a two-receiver and transmitter demonstration with loopback and includes a transport stream (TS) generator and TS packet checker.

The ASI demonstration uses the Altera® ASI MegaCore® function and the Cyclone video demonstration board.

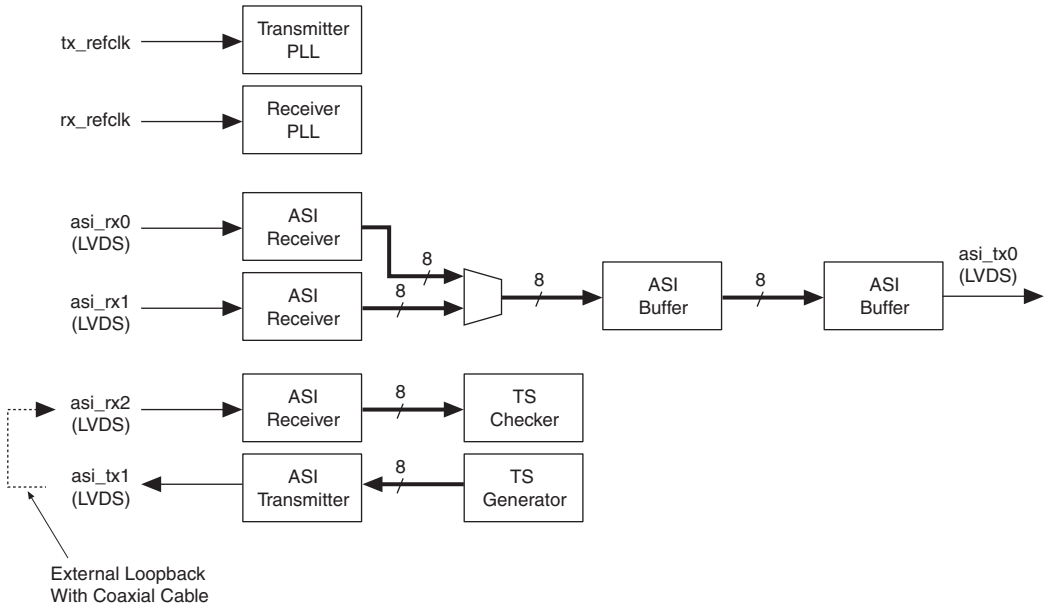
For information on the Altera Cyclone Video Demonstration Board, refer to the *Cyclone Video Demonstration Board Data Sheet*.

For information on the ASI MegaCore function, refer to the *ASI MegaCore Function User Guide*.

Functional Description

Figure 1 shows the ASI demonstration block diagram.

Figure 1. Block Diagram



Note to Figure 1:

(1) The LVDS standard copes with a 270-Mbps bit rate and enables better noise integrity than LVTTL/LVCMOS.

The design consists of the following elements:

- Cyclone low voltage differential signalling (LVDS) inputs and outputs (I/Os) for the receiver and transmitter
- ASI receiver
- ASI transmitter
- ASI buffer
- TS generator
- TS checker
- Two PLLs for frequency multiplication—one for the transmitter, one for the receiver

For more information on the ASI transmitter and receiver, refer to the *ASI MegaCore Function User Guide*.

The two reference clocks can be either asynchronous to each other or the two PLLs can be driven from the same clock source.

For the TS check mode, the transmit and receive paths are independent—the design can transmit and receive at the same time. For loopback, the transmit path is coupled to the receive path through a rate matching first-in first-out (FIFO) buffer.

The design uses two PLLs. For the receiver logic, the first PLL generates a 5× oversample scheme 337.5-MHz clock (27 MHz × 50/4) and a 337.5-MHz clock phase shifted by 90°. The second PLL generates a transmit serial clock at 270 MHz.

ASI Buffer

The ASI buffer rate matches between the incoming byte rate and transmit or system clock rate, because of phase and frequency difference between the two rates. The frequency difference can be up to +/- 100 ppm.

TS Generator

The TS generator generates null TS packets of either 204 or 188 bytes. These packets can be spaced with idle cycles. In this demonstration design, this idle time can be switched between 10 and 1,023 cycles. The packets start with a `NULL 47 1F FF 10` header followed by a byte indicating the channel ID, then 4 bytes for the packet count. The rest of packet is filled with values from an incrementing counter.

TS Checker

The TS checker checks for the correct reception of ASI packets. The packets must be of the same format as those generated by the TS generator. This block checks that the packets are of the correct length and that the header, channel ID, packet counts, and payload are correct.

Getting Started

This section involves the following steps:

1. System Requirements
2. Install the Design
3. Compile the Design
4. Use the Demonstration

System Requirements

The design requires the following hardware and software:

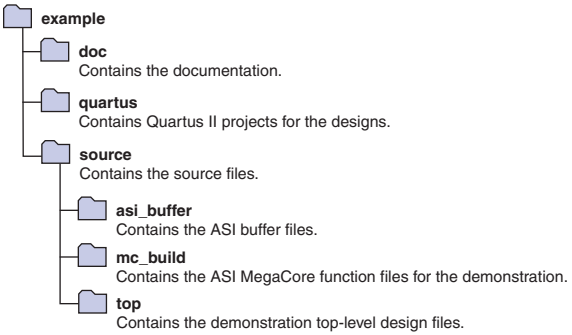
- Cyclone video demonstration board
- ASI MegaCore function v1.0.0
- Quartus II software version 6.0

To obtain a Cyclone video demonstration board, contact your local Altera representative.

Install the Design

Figure 2 shows the directory structure of the demonstration, which is in the example directory of the ASI MegaCore function.

Figure 2. Directory Structure



Compile the Design

Quartus II project files are provided for the demonstration mapped to the Cyclone video demonstration board. The **.qsf** file defines the pinout and other compilation directives for the design. You must compile the design to produce the device images required for the demonstration.

To compile the demonstration design, open the relevant project in the Quartus II software and choose **Start Compilation** (Tools menu).

Use the Demonstration

The ASI demonstration exercises both the ASI receiver and transmitter. The loopback part of the design uses two receive ports—one with a cable equalizer (BNC J1) and one without (BNC J2). Both ASI inputs are received and decoded.

The design selects the input that is indicating lock and connects this stream to the ASI buffer. If both receivers are indicating lock, `asi_rx0` is chosen.

The output of the ASI buffer is connected to an ASI transmitter and is output on the `asi_tx` connector.

Additional to this loopback function, a packet generator and checker are included to test the correct operation of the design.

To use the demonstration design, follow these steps:

1. Select the required clock source by editing the **source\top\cvdb_demo_mc.v** file and uncommenting the appropriate define statement.
2. Compile the design using the Quartus II software. The **.qpf** and **.qsf** files are in the **quartus** directory.
3. In TS check mode, connect a coaxial cable between BNC J9 and J3.

   or

   If in loopback mode, connect an ASI source to BNC J2 or J1 and connect an ASI monitor to BNC J8.
4. Connect a 5-V power supply to the development board.
5. Program the **cvdb_demo_mc.sof** file to the board.
6. In TS check mode switch 6 alters the length of the TS packets. Open is 188; closed is 204.
7. In TS check mode switch 4 alters the gap between the TS packets. Open is 10; closed is 1,023.
8. Push button S1 to reset the system.

The board has the following LEDs:

- LED 0 illuminates to indicate if receiver 0 is in synchronization
- LED 1 illuminates to indicate if receiver 1 is in synchronization
- LED 2 illuminates to indicate if receiver 2 is in synchronization and has passed the TS packet check
- LED 3 illuminates to indicate if either receiver 0 or 1 is in synchronization

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