# Analog Devices Link-Port Reference Design

February 2005, version 1.3 Application Note

## Introduction

The link-port reference design implements link-port transmitters and receivers in Altera® FPGAs. It demonstrates that Altera Stratix® and Cyclone™ devices are suitable in performance to implement link-port interfaces to Analog Devices TigerSharc digital signal processing (DSP) functions.

Altera supplies the reference design as Verilog HDL source code. The reference design includes a testbench that allows you to test the Verilog HDL source code.

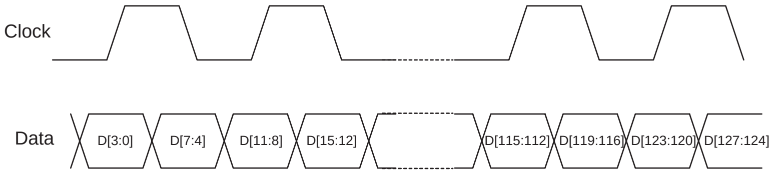
## Background

The link-port interface is a high-speed communications interface available on Analog Devices TigerSharc TS20x DSP functions (see www.analog.com) with an low-voltage differential signaling (LVDS) electrical interface using double data rate (DDR) data. Each link-port interface is either a transmitter or a receiver with one or four data pins, an LVDS clock and a number of single ended status signals. The link-port interface has the following features:

- Discontinuous clock runs only when data is being transmitted
- Quad word (128 bit) minimum data size
- Optional checksum byte

The link-port reference design concentrates on the four-bit version of the link-port interface. Figure 1 shows the data format of a quad word D[127:0] on a four bit link-port interface.

*Figure 1. Link-Port Data Format*



The single-ended status signals are:

- Acknowledge output from the receiver, which signals the transmitter to cease transmitting when the receivers buffers are full.
- Block complete output from the transmitter, which indicates the end of a transmission of a number of quad words.

> ☞ The block complete output is particularly useful when used in with Altera's Atlantic™ interface end of packet signal.

The link-port clock may operate at up to 500 MHz. The DDR data gives a maximum data rate of 1 gigabits per second (Gbps) for a single bit data link or 4 Gbps for a four bit data link.

The link-port receiver in the TigerSharc DSP operates independently of the core clock. There are no particular target frequencies for the FPGA transmitter other than the fastest achievable in a particular speed grade.

The link-port transmitter in the TigerSharc DSP can operate from the DSP core clock divided by 1, 1.5, 2, or 4. Assuming the core is running at 500 MHz, this gives useable link-port clocks of 500, 333, 250, or 125 MHz. The FPGA receiver can target these frequencies.

The high data rates achievable across a link-port interface mean that great care has to be taken in the design, which has to be highly pipelined to achieve the $f_{MAX}$ required. Logic and I/O placement is crucial—logic lock regions and location assignments are used where necessary to achieve the best performance. These assignments vary with the targeted device.

## Functional Description

This section describes the link-port reference design transmitter and receiver.

### Transmitter

Figure 2 shows the transmitter block diagram.

*Figure 2. Transmitter Block Diagram*

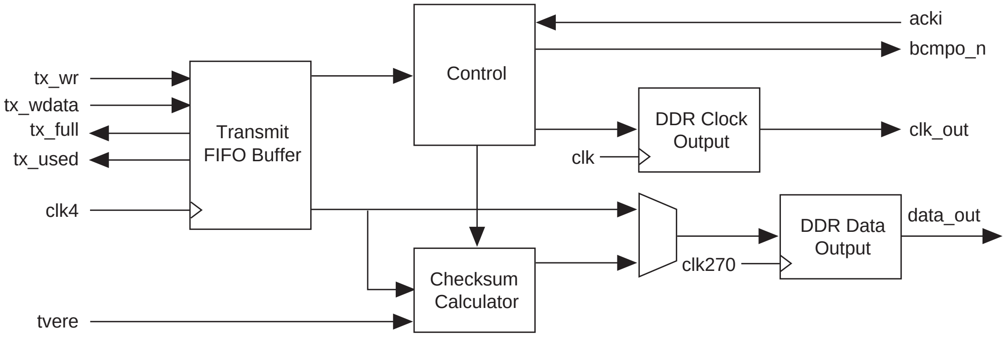


Table 1 shows the transmitter pinouts

*Table 1. Transmitter Pinouts*

| Pin | Width (Bits) | Direction | Interface | Description |
|---|---|---|---|---|
| `rst_n` | 1 | Input | Local | Active low reset. |
| `clk` | 1 | Input | Local | Clock. |
| `clk270` | 1 | Input | Local | Clock delayed 270 degrees. `Clk` and `clk270` are used to generate the link-port clock and DDR data. |
| `clk4` | 1 | Input | Local | Clock divided by 4 for the local FIFO interface. |
| `tvere` | 1 | Input | Local | Verification byte enable. Enables transmission of optional checksum. |
| `tx_wr` | 1 | Input | Local | Transmit FIFO write strobe. |
| `tx_wdata` | 33 | Input | Local | Transmit FIFO write data. `Tx_wdata[32]` indicates the end of a block of data to cause `bcmpo` to be asserted. |
| `tx_used` | 4 | Output | Local | Transmit FIFO status, entries used. |
| `tx_full` | 1 | Output | Local | Transmit FIFO full status. |
| `clk_out` | 1 | Output | Link-Port | Clock at the same frequency as `clk` and `clk270`. |
| `data_out` | 4 | Output | Link-Port | Data. |
| `acki` | 1 | Input | Link-Port | Acknowledge from the receiver. Inhibits further transmission when asserted. |
| `bcmpo_n` | 1 | Output | Link-Port | Block complete to receiver. Asserted when transmitting a quad word with `tx_wdata[32]` set. |

### Operation

The transmitter requires three clock inputs for operation, the link-port clocks (`clk` and `clk270`) and the local system clock, `clk4`, which is one-quarter of the link-port frequency and synchronous to it. Each 128-bit quad word for transmission is written in four cycles over the 33-bit `tx_wdata` bus into the transmit FIFO buffer, `tx_fifo`.

Figure 3 shows a quad word being written. Transmit FIFO status signals, `tx_used` and `tx_full`, indicate when more data may be written to the transmit FIFO buffer.

*Figure 3. Transmitter Local Data Write Cycles*

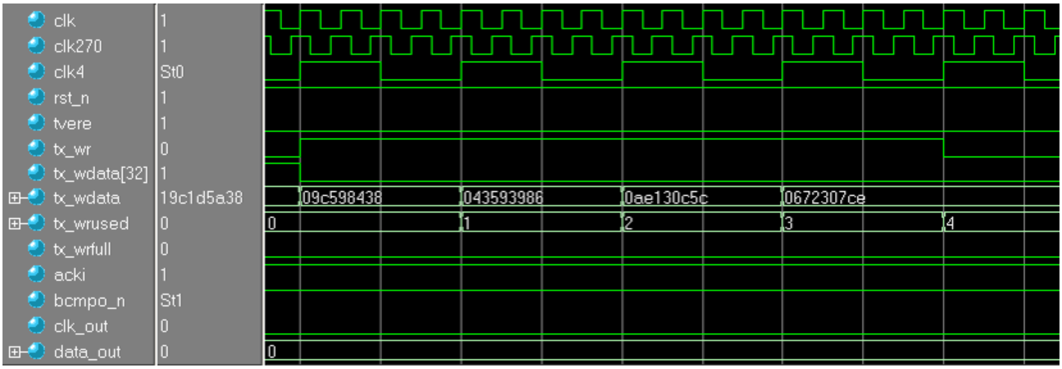
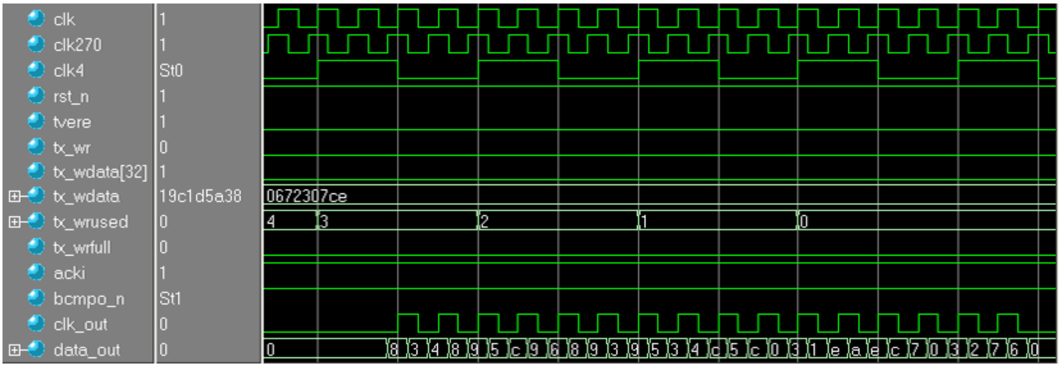


Figure 4 shows the same data as it is transmitted through the link-port interface. Becasue of the internal pipelining, `tx_used` begins decrementing before the transmission.

*Figure 4. Transmitter Operation*



If `tx_wdata[32]` is asserted (it should be asserted for all write cycles), the quad word is transmitted with the block complete output, `bcmpo_n`, asserted. Figure 5 shows the same data as it is transmitted through the link-port interface. Becuase of the internal pipelining, `tx_used` begins decrementing before the transmission.

Figure 5 shows a link-port transmission with block complete signalled by the assertion of `bcmpo_n`.

*Figure 5. Transmitter Block Complete*

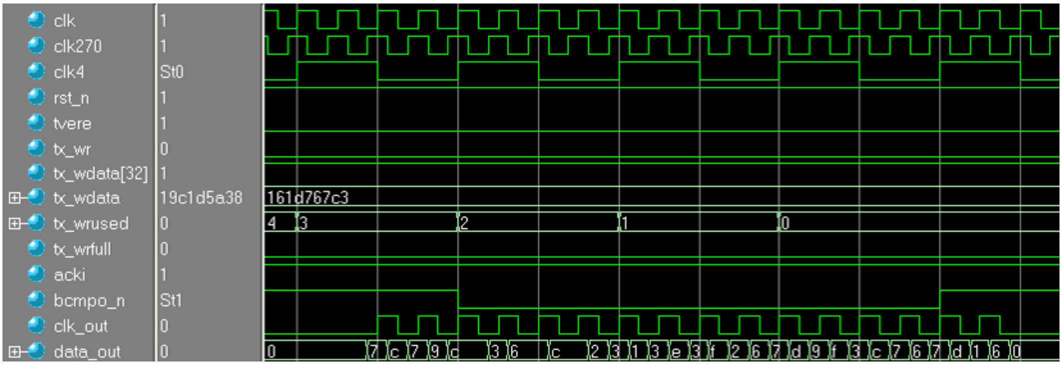
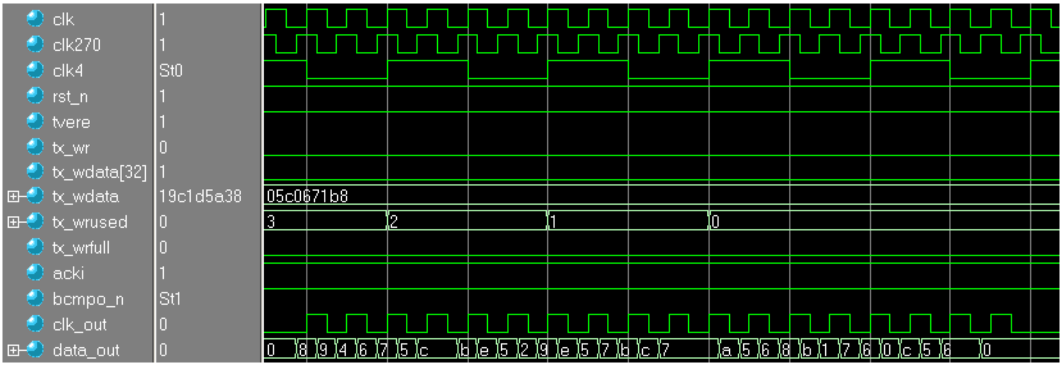


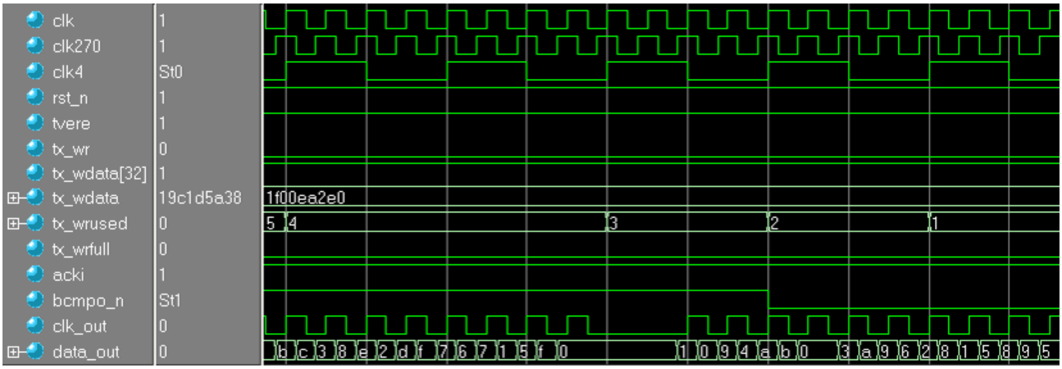
Figure 6 shows a link-port transmission with checksum enabled. Two extra link-port clock cycles are appended to the data. During the first clock the checksum is sent as two four bit nibbles on the rising and falling edges. During the second clock a dummy byte (0x00 data) is transmitted.

*Figure 6. Transmission With Checksum*



If sufficient data is available in `tx_fifo`, quad words continue to be transmitted until `tx_fifo` is empty or has less than 128 bits of data available. When the checksum is disabled, quad words are transmitted back-to-back with no intervening delay. When the checksum is enabled there is a delay of two link-port clock periods after the dummy byte, during which the link-port clock and data are inactive. Figure 7 shows this delay where the link-port clock remains low for two link-port clock periods.

*Figure 7. Inter-packet Delay—Checksum Enabled*



### *Implementation*

The transmitter design was implemented using integrated synthesis in the Quartus II software version 3.0 SP2.

The link-port receiver in the TigerSharc DSP requires 200 ns link-port data setup and hold time relative to the link-port clock. The Quartus II timing analyzer results for clock-output timing of the link-port clock and data must be examined and allowance made for timing skew on the PCB between the transmitter and receiver when determining the performance of the link-port interface.

## Receiver

Figure 8 shows the receiver block diagram.

*Figure 8. Receiver Block Diagram*

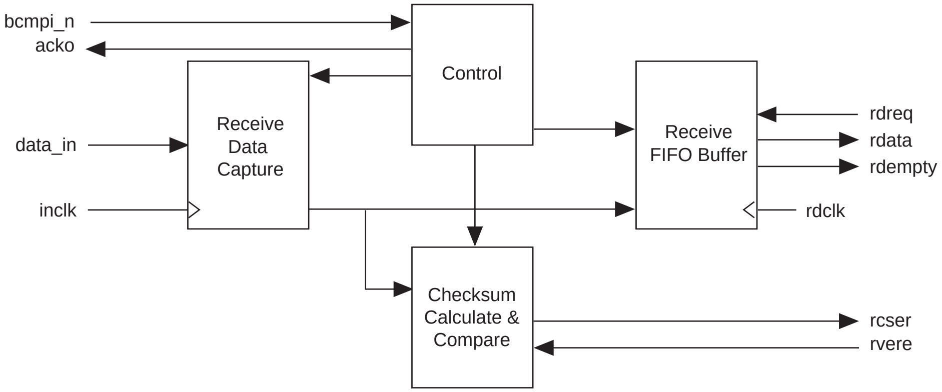


Table 2 shows the receiver pinouts.

*Table 2. Receiver Pinouts (Part 1 of 2)*

| Pin | Width | Direction | Interface | Description |
|---|---|---|---|---|
| `rst_n` | 1 | Input | Local | Reset, active low. |
| `clk` | 1 | Input | Local | Clock. |
| `datain` | 4 | Input | Link-Port | Data. |
| `inclock` | 1 | Input | Link-Port | Clock. |
| `inclocken` | 1 | Input | Link-Port | Must be an I/O pin tied high. |

*Table 2. Receiver Pinouts (Part 2 of 2)*

| Pin | Width | Direction | Interface | Description |
|---|---|---|---|---|
| `acko` | 1 | Output | Link-Port | Acknowledge out to the transmitter. Asserted to hold off further transmission when the receiver FIFO buffer is becoming full. |
| `bcmpi_n` | 1 | Input | Link-Port | Block complete input Indicates the end of a block of data. |
| `rvere` | 1 | Input | Local | Verification byte enable. Enables reception and checking of optional checksum. |
| `rcser` | 1 | Output | Local | Checksum error status. |
| `rdreq` | 1 | Input | Local | Receive FIFO read request. |
| `empty` | 1 | Output | Local | Receive FIFO empty status. |
| `rdata` | 33 | Output | Local | Receive FIFO read data. Indicates `bcmpi_n` was asserted during the transmission of the associated quadword. |

### *Operation*

The discontinuous nature of the link-port clock means that it is difficult to use a PLL to lock to the clock or a Stratix SERDES block to recover the data. The link-port clock is used directly to capture the data in two shift registers clocked by the positive and negative edges of the link-port clock, respectively. The captured data is transferred to the receiver FIFO buffer, `rx_fifo`, and also used to re-calculate and verify the checksum, if enabled.

#### Local Clock Requirement

The local clock, `clk`, is asynchronous to the link-port clock but its frequency must be at least 2/5 of the link-port clock frequency and no more than 2/3 of the link-port clock frequency. Thus, for a 500 MHz link the local clock must be in the range 200 to 333.33 MHz.

### Receiver Operation Examples

Figure 9 shows a quad word (with checksum and dummy byte) with bcmp_i asserted to indicate end of block.

*Figure 9. Quad Word With bcmpi_n*

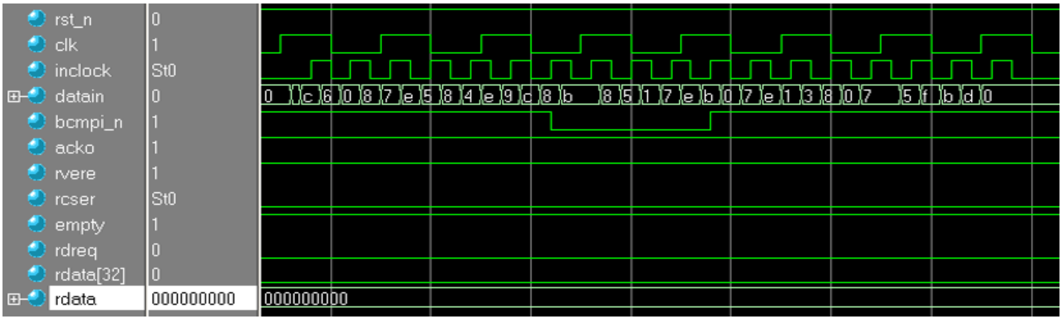


Figure 10 shows the same data being removed from the FIFO buffer. `rdata[32]` is asserted during the third word, which reflects the end of block status.

*Figure 10. Receiver Local Data Read*

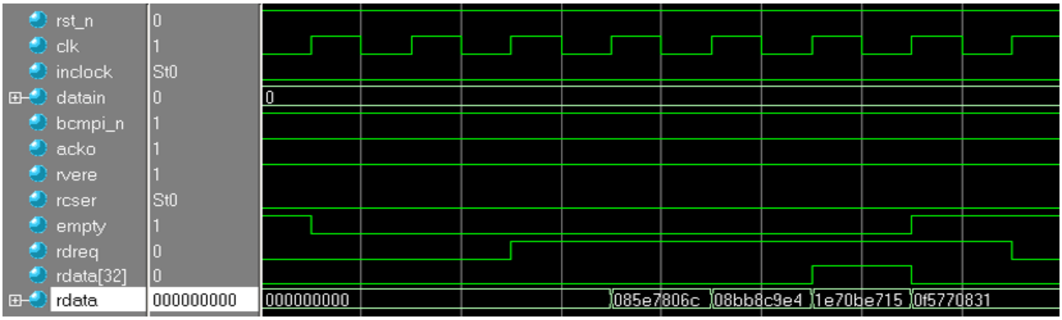
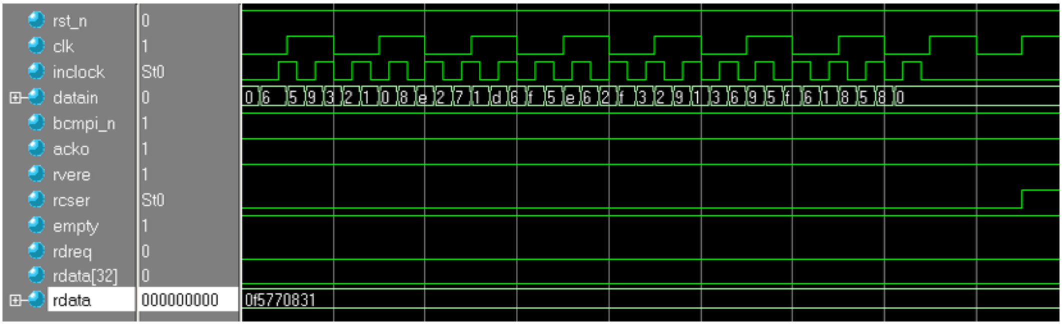


Figure 11 shows `rcser` asserted on the detection of a checksum error.

*Figure 11. Receiver Checksum Error*



|  |  |
|---|---|
| rst_n | 0 |
| clk | 1 |
| inclock | St0 |
| datain | 0 |
| bcmpi_n | 1 |
| acko | 1 |
| rvere | 1 |
| rcser | St0 |
| empty | 1 |
| rdreq | 0 |
| rdata[32] | 0 |
| rdata | 000000000 |

0 6 5 9 3 2 1 0 8 e 2 7 1 d 6 f 5 e 6 2 f 3 2 9 1 3 6 9 5 f 6 1 8 5 8 0
0f5770831

### Implementation

The transmitter design was implemented using integrated synthesis in the Quartus II software version 3.0 SP2.

### Design Considerations

The link-port transmitter in the TigerSharc DSP guarantees the timing relationship between clock and data (see Figure 12).

*Figure 12. Receiver Timing Requirements*

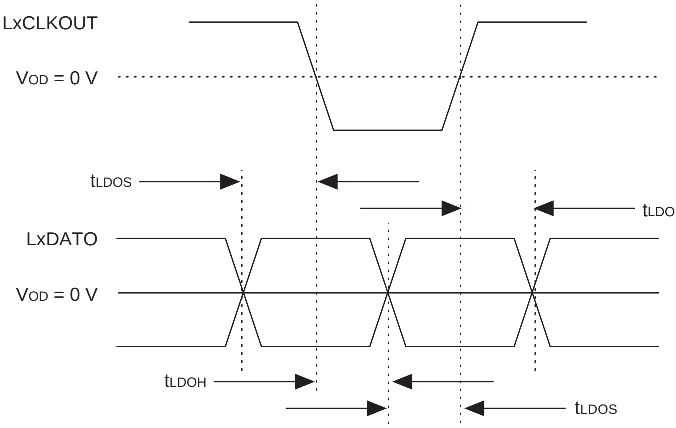


Table 3 shows the receiver setup and hold times, relative to the link-port clock and assumes a DSP core clock of 500 MHz.

*Table 3. Receiver Setup & Hold Times*

| Link-Port Clock (MHz) | $t_{LDOS}$, $t_{LDOH}$ (ns) |
|---|---|
| 250 *(1)* | 0.7 |
| 333 *(2)* | 0.6 |
| 500 | 0.35 |

*Notes to Table 3:*

(1) Core/2.

(2) Core/1.5.

These set up and hold times represent the best possible case at the receiver pins and are used as timing requirements during Quartus II compilation. The Quartus II timing analyzer results must be examined and allowance made for timing skew on the PCB between the transmitter and receiver when determining the performance of the link-port.

# Getting Started

This section involves the following steps:

1. "Software Requirements".
2. "Install the Design".

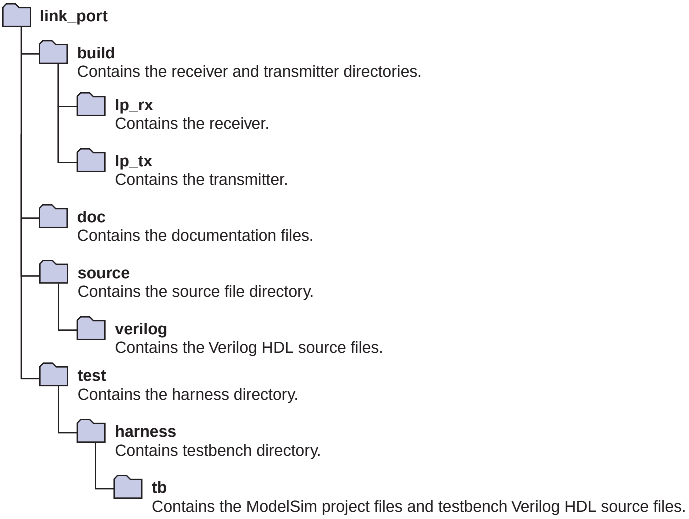
## Software Requirements

The reference design requires the Quartus® II software version 3.0 SP2, or higher.

## Install the Design

To install the reference design, run the **.exe** and follow the installation instructions. Figure 13 shows the directory structure.

*Figure 13. Directory Structure*


link_port
build
Contains the receiver and transmitter directories.
lp_rx
Contains the receiver.
lp_tx
Contains the transmitter.
doc
Contains the documentation files.
source
Contains the source file directory.
verilog
Contains the Verilog HDL source files.
test
Contains the harness directory.
harness
Contains testbench directory.
tb
Contains the ModelSim project files and testbench Verilog HDL source files.

# Performance

This section details the transmitter and receiver performance.

## Transmitter

This section details transmitter performance for Stratix and Cyclone devices.

### *Stratix Performance*

The transmitter requires 222 logic elements (LEs) and two M4K memory blocks. A PLL is also required. Pin and node assignments are used along with other assignments to guarantee performance and allow correct timing analysis of the design. These assignments should be examined in the example Quartus II projects before attempting to target different devices or change the pin assignments. If the `tvere` input is tied to logic 0, which disables the checksum option, the LE count is reduced to 131.

The **alt_ddio_out** megafunction generates the link-port clock and data. This megafunction is mapped into I/O cells in the Stratix family, which gives well defined timing for the link-port clock and data.

Table 4 shows the transmitter performance for the Stratix EP1S10F484 family.

*Table 4. Transmitter Performance—Stratix Device*

| Stratix Speed Grade | $f_{MAX}$ (MHz) | Mbps per data pin |
|---|---|---|
| -7 | 385 | 770 |
| -6 | 450 | 900 |
| -5 | 500 | 1,000 |

### Cyclone Performance

The transmitter requires 224 LEs and two M4K memory blocks. A PLL is also required. Pin and node assignments are used along with other assignments to guarantee performance and allow correct timing analysis of the design. These assignments should be examined in the example Quartus II projects before attempting to target different devices or change the pin assignments. If the `tvere` input is tied to logic 0,which disables the checksum option, the LE count is reduced to 135.

The **alt_ddio_out** megafunction generates the link-port clock and data. This megafunction is mapped into LEs in the Cyclone family and requires careful placement of these cells relative to their associated I/O cells to give an acceptable relationship between the link-port clock and data.

Table 4 shows the transmitter performance for the Cyclone EP1C3T144 family.

*Table 5. Transmitter Performance—Cyclone Device*

| Speed Grade | $f_{MAX}$ (MHz) | Mbps per data pin |
|---|---|---|
| -8 | 250 | 500 |
| -7 | 300 | 600 |
| -6 | 320 | 640 |

## Receiver

This section details receiver performance for Stratix and Cyclone devices.

### Stratix Performance

The receiver requires 301 LEs and one M4K memory block. Timing assignments are used with other assignments to guarantee performance and allow correct timing analysis of the design. These assignments should be examined in the example Quartus II projects before attempting to target different devices. If the `rvere` input is tied to logic 0, disabling the checksum option, the LE count is reduced to 269.

Table 6 shows the receiver performance for the Stratix EP1S10F484 family. The actual $f_{MAX}$ achievable may be higher but is limited in these examples to useful frequencies assuming a DSP core clock in the transmitter of 500 MHz.

*Table 6. Receiver Performance—Stratix Devices*

| Speed Grade | $f_{MAX}$ (MHz) | Mbps per data pin |
|---|---|---|
| -8 | 333 | 666 |
| -7 | 333 | 666 |
| -6 | 500 | 1,000 |

### Cyclone Performance

The receiver requires 293 LEs and one M4K memory block. Timing assignments are used with other assignments to guarantee performance and allow correct timing analysis of the design. These assignments should be examined in the example Quartus II projects before attempting to target different devices. If the `rvere` input is tied to logic 0, disabling the checksum option, the LE count is reduced to 268.

Table 6 shows the receiver performance for the the Cyclone EP1C3T144 family. The actual $f_{MAX}$ achievable may be higher but is limited in these examples to useful frequencies assuming a DSP core clock in the transmitter of 500 MHz.

*Table 7. Receiver Performance—Cyclone Devices*

| Speed Grade | $f_{MAX}$ (MHz) | Mbps per data pin |
|---|---|---|
| -8 | 250 | 500 |
| -7 | 250 | 500 |
| -6 | 333 | 666 |

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