

## Introduction

Since its introduction in 1992, PCI Local Bus has become the most widely implemented expansion bus standard in the world. The PCI Local Bus is a high performance 32-bit or 64-bit bus with multiplexed address and data lines. The bus is intended for use as an interconnect mechanism between peripheral controller components, peripheral add-in cards, and processor/memory systems. The PCI Local Bus Specification, Rev. 2.3, specifies both the 3.3 V and 5 V signaling requirements although 5 V only keyed cards are not allowed.

With ever shrinking process technologies and associated voltages, it is becoming difficult for silicon suppliers to support 5 V signaling requirements. Altera's Stratix™, Stratix II, Stratix GX and Cyclone™ devices support the 3.3 V PCI signaling requirements.

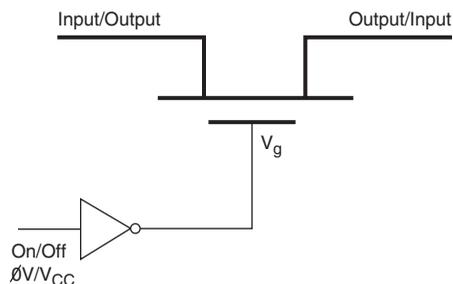
This application note describes how to connect Altera's 3.3 V PCI devices to a 5 V PCI bus by using bus switches. The application note addresses the following topics:

- Bus switches overview
- Implementation
- PCI considerations.

## Bus Switches Overview

Each bus switch consists of an N channel MOS transistor driven by a CMOS logic gate, as shown in [Figure 1](#) below.

**Figure 1. Bus Switch Block Diagram**



The switch is enabled when the gate-to-source voltage ( $V_g$ ) exceeds 1 V. As the input voltage rises, the resistance of the switch also rises and the output voltage also rises. At approximately  $V_{cc} - V_t$  [ $V_t$  - threshold voltage is typically 1 V] the output reaches its highest level [4 V when  $V_{cc} = 5$  V]. Even when the input voltage is higher than 4 V, the output remains clamped at 4 V.

The output limiting characteristic of bus switches can be used as a 5 V PCI bus to 3.3 V PCI bus converter. The operation of the switch is bi-directional. Some of the other features of a bus switch are as follows:

- 250 ps propagation delay
- typical load of 5 pF
- Available in different bus-widths

Table 1 lists some bus switch devices.

**Table 1. Bus Switch Device Information.**

Part #	Vendor	Link to data sheet	Characteristic
SN74CBTD3384	Texas Instruments	<a href="http://focus.ti.com">focus.ti.com</a>	10-bit switch with built-in diode
IDTQS3861	Integrated Device Technology	<a href="http://www.idt.com">www.idt.com</a>	10-bit switch
PI5C32X245	Pericom Semiconductor	<a href="http://www.pericom.com">www.pericom.com</a>	16-bit switch
FSTD16244	Fairchild Semiconductor	<a href="http://www.fairchildsemi.com">www.fairchildsemi.com</a>	16-bit switch with built-in diode

## Implementation

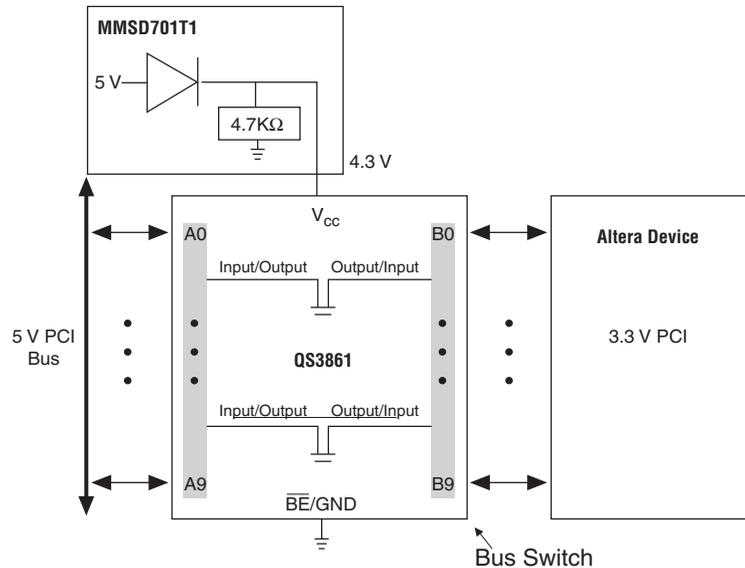
Figure 2 shows an Altera 3.3 volt PCI device connected to the 5 V PCI bus through a bus switch device. The  $V_{cc}$  pin of the bus switch device is connected to a 4.3 volts. By supplying 4.3 volts to the  $V_{cc}$  pin of a bus switch device, the output will be limited to 3.3 volts.

A 4.3 V  $V_{cc}$  is created by adding a diode, such as a MMSD701T1 between the 5 V supply and a 10-bit IDT QS3861 device.



Some devices like Texas Instrument's SN74CBTD3384 have an internal diode which does not require an external diode.

**Figure 2. Connecting 3.3 V Altera Device to a 5 V PCI Bus Using Bus Switches**



## PCI Considerations

The implementation using bus switches is a PCI compatible solution.



Altera does not recommend the use of bus switches to be used in PCI add-in cards that are required to be fully PCI compliant.



This is a non-standard bus switch implementation and is contrary to the specification as defined in section 4.4.3.4 (Signal Loading) of the PCI specification. As displayed, this implementation changes the characteristic impedance of the PCI traces. For reference see “*PCI Local Bus Specification, Revision 2.3*”.



The PCI bus uses reflected wave switching; as a result the voltage at the pins of PCI devices could be greater than the typical ground-to-V<sub>cc</sub> voltage range.



The user should verify that the bus switch devices meet the AC requirements in their systems.

## Electrical Considerations

Large undershoots can cause significant clamp current within the bus switch. If the transient pulses have a high duty cycle, the average power dissipation must be taken into account to ensure that the average DC current and power dissipation do not exceed the rated values of the bus switches.

## Layout Considerations

The PCI specifications requires the following trace lengths from the edge of the connector to the device

- 32-bit signals - 1.5 inches
- 64-bit extension signals - 2.0 inches
- clock -  $2.5 \pm 0.1$  inches



The user must ensure that the total trace lengths meet the PCI specification stated above, for an example of the layout using bus switches, refer to the *Stratix PCI development board data sheet*.

## Timing Considerations

The slew rates of PCI signals is much slower than the 250 ps delay of a bus switch, for a first order approximation the delay of the bus switch can be ignored.

### Setup Time ( $T_{su}$ )

The PCI signals need to meet stringent setup requirements (7 ns for 33 MHz operation and 3 ns for 66 MHz operation), since both the clock and data signals are delayed by the same amount (250 ps), the addition of the bus switches does not affect the setup time margins in the device.

### Clock-to-Out ( $T_{val}$ )

The clock-to-out requirement is 11 ns for 33 MHz operation and 6 ns for 66 MHz operation. This value is specified from the rising edge of the clock at the input of the chip. In order to meet the PCI requirements, the user must add an additional 500 ps of margin (250 ps for the clock and 250 ps for the data signal).

## References

- *PCI Local Bus Specification, Revision 2.3*, [www.pcisig.com](http://www.pcisig.com)
- Stratix PCI Development Board, [www.altera.com/literature/ds/ds\\_stratix\\_pci\\_bd.pdf](http://www.altera.com/literature/ds/ds_stratix_pci_bd.pdf)

- *"5 V and 3 V conversion with Zero Delay"*,  
**[www.idt.com/docs/AN\\_11.pdf](http://www.idt.com/docs/AN_11.pdf)**
- *"5-V to 3.3-V Translation With the SN74CBTD3384"*,  
**[focus.ti.com/lit/an/scda003b/scda003b.pdf](http://focus.ti.com/lit/an/scda003b/scda003b.pdf)**



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