

Introduction

Designers expect Altera® devices to perform in a variety of environments and conditions. Reliable devices decrease design and maintenance costs and increase product life cycles. Altera submits its devices to a series of strenuous tests to ensure that they provide maximum value to end users. Device reliability is generally defined as the probability that a device will perform its intended function under specified operating conditions throughout its life. As a result, industry-wide reliability guidelines were established.

Altera devices exceed the reliability requirements established by the Electronic Industries Association (EIA) and Joint Electron Device Engineering Council (JEDEC). JEDEC qualification tests ensure that Altera devices meet or exceed these reliability standards. Tests are performed under extreme conditions and the failure rate can be extrapolated to typical conditions using equations that describe the acceleration of failure mechanisms. This application note describes some of the tests used for device reliability testing, including:

- Stress-test-driven qualifications
- Moisture/reflow sensitivity
- Temperature cycling
- Humidity bias testing
- HAST testing
- Autoclave testing

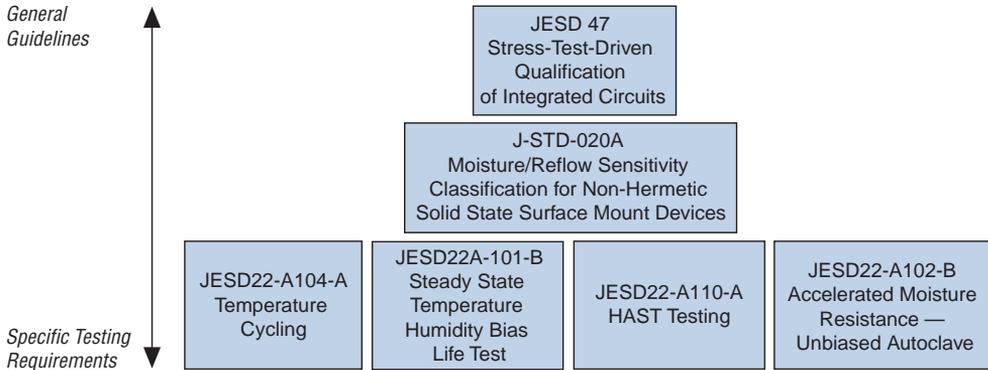


For more information on Altera device reliability, see the *Altera Device Reliability Report*, which is available from Altera literature services.

EIA/JEDEC Standards

EIA/JEDEC standards identify testing requirements that range from general to specific. For example, all plastic package testing must follow general guidelines specified by JESD 47, but only certain types of device packages may be required to undergo HAST testing. The pyramid in [Figure 1](#) illustrates the hierarchy for EIA/JEDEC testing procedures and serves as the model for Altera testing requirements.

Figure 1. EIA/JEDEC Testing Hierarchy



As new technologies are developed, Altera engineers rely on the EIA/JEDEC testing hierarchy to qualify new semiconductor architectures. New architectures may include smaller process geometries, an increased number of die layers, increased gate and I/O pin counts, decreased voltage levels, and changes in package material composition. These design changes affect the reliability of a device. As a result, the device may require a different set of tests as technologies advance.

The Stress-Test-Driven Qualification of Integrated Circuits (JEDEC Std. 47) guideline determines which tests a new design must undergo and helps product engineers identify and correct flaws that may arise. The guideline also identifies sample size requirements and testing qualifications for new devices to help expose process flaws.



For more information on EIA/JEDEC standards, visit the JEDEC web site at <http://www.jedec.org>.

Moisture/ Reflow Sensitivity

Altera uses moisture/reflow sensitivity testing (J-STD-020A) guidelines to inform customers of device sensitivity to moisture-induced stress. After testing, devices are assigned sensitivity levels. These classification levels are useful in determining the proper storage and handling of Altera devices to prevent thermal and mechanical damage during solder reflow or repair. Moisture sensitivity levels determine the length of time a device can be exposed to humidity. See [Table 1](#).

Table 1. Moisture Sensitivity Levels

Level	Floor Life		Soaking Requirements	
	Time	Conditions (1)	Time (Hours)	Conditions (1)
1	Unlimited	≤30 °C/85%	168	85 °C/85%
2	1 Year	≤30 °C/60%	168	85 °C/60%
2a	4 Weeks	≤30 °C/60%	672	30 °C/60%
3	168 Hours	≤30 °C/60%	192	30 °C/60%
4	72 Hours	≤30 °C/60%	96	30 °C/60%
5	48 Hours	≤30 °C/60%	72	30 °C/60%
5a	24 Hours	≤30 °C/60%	48	30 °C/60%
6	Time On Label	≤30 °C/60%	Time On Label	30 °C/60%

Note:

(1) Condition percentages denote relative humidity levels.

The device classification applies to all surface mount packages: ball-grid array (BGA), small-outline integrated circuit (SOIC), plastic J-lead chip carrier (PLCC), plastic thin quad flat pack (TQFP), plastic quad flat pack (PQFP), and power quad flat pack (RQFP) device packages. Because of their composition, these device packages could be damaged during solder reflow.

The vapor pressure of moisture trapped inside of a plastic package increases when the package is exposed to high solder reflow temperatures. This pressure can lead to internal delamination, internal cracks, bond damage, wire necking, bond lifting, die lifting, thin film cracking, or cratering beneath the bonds. In extreme cases, the package emits an audible crack, also known as the “popcorn” effect.

To minimize the chances of device damage, Altera recommends using a 100% convection reflow system that is capable of maintaining the reflow profiles required by the J-STD-020A standard.



For more information on reflow soldering, see [Application Note 81 \(Reflow Soldering Guidelines for Surface-Mount Devices\)](#).

Small, thin devices can reach body temperatures greater than 220 °C when reflow-soldered to boards profiled for larger devices. To compensate for this difference, some small packages have been reclassified to withstand 235 °C. [Table 2](#) defines the transition thickness/volume of packages that can reach 235 °C when reflow soldered to boards with larger devices.

Table 2. Small Device Reflow Conditions

Conditions	Package Thickness ≥ 2.5 mm & All BGA Packages	Package Thickness < 2.5 mm & Package Volume ≥ 350 mm ³	Package Thickness < 2.5 mm & Package Volume < 350 mm ³
Convection Temp.	220 +5/-0 °C	Convection 220 +5/-0 °C	Convection 235 +5/-0 °C
VPR Peak Temp.	215-219 °C	215-219 °C	N.A. (1)
IR/Convection Temp.	220 +5/-0 °C	220 +5/-0 °C	235 +5/-0 °C
Package Type	All BGA, FineLine BGA packages	All other packages	T44, Q44, T100, T32 packages

Note:

(1) VPR phase will not exceed 219 °C.

For more information on moisture/reflow sensitivity classification for plastic packages, refer to *JEDEC Standard J-STD-020A*.

Package reliability can also be affected by the rate at which a particular device reaches its testing temperature. [Table 3](#) lists classification reflow profiles for two types of reflow convection methods: full convection and infra-red convection.

Table 3. Classification Reflow Profiles

Condition	Full or Infra-Red Convection (1)
Average ramp-up rate (183 °C to peak)	1 - 3 °C/second
Preheat temperature 125 °C (± 25 °C)	120 seconds maximum
Temperature maintained above 183 °C	60 to 150 seconds
Time within 5 °C of actual peak temperature	10 to 20 seconds
Peak temperature range	(2)
Ramp-down rate	6 °C/second maximum
Time 25 °C to peak temperature	6 minutes maximum

Note:

- (1) Altera recommends using the full convection method for production.
 (2) See [Table 2](#).

Temperature Cycling

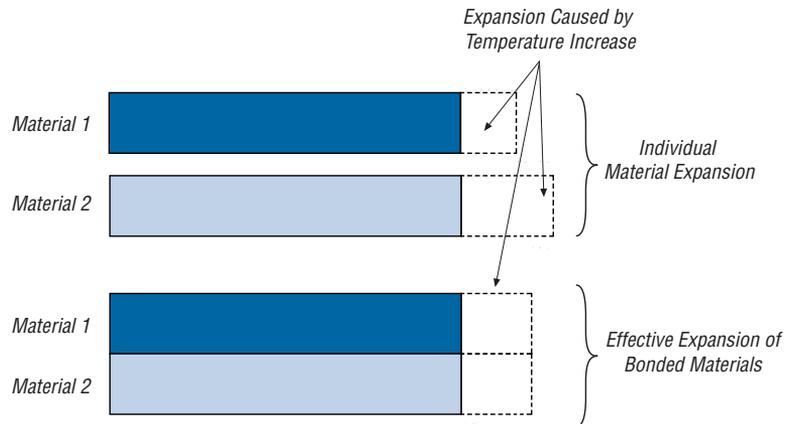
Temperature cycling (JESD22-A104-A) is performed to determine the resistance of Altera devices to high and low temperature extremes. This environmental stress test is designed to simulate the extensive changes in temperature to which devices and packages may be exposed. To pass the test, devices must not show signs of damage such as cracking, chipping, or breaking. [Table 4](#) shows the classifications for Altera devices.

Classification	Low Temperature (°C)	High Temperature (°C)
A	-55 (+0, -10)	+85 (+0, -10)
B	-55 (+0, -10)	+125 (+0, -10)
C	-65 (+0, -10)	+150 (+0, -10)
D	-65 (+0, -10)	+200 (+0, -10)
F	-65 (+0, -10)	+175 (+0, -10)
G	-40 (+0, -10)	+125 (+0, -10)
H	-55 (+0, -10)	+150 (+0, -10)

Temperature cycling may also expose weaknesses in packages that are composed of different materials. If device packages are composed of different materials, expansion and contraction of the package materials can occur at different rates when exposed to temperature extremes.

Figure 2 shows an example of the differences in the thermal coefficients of expansion between two materials with identical lengths.

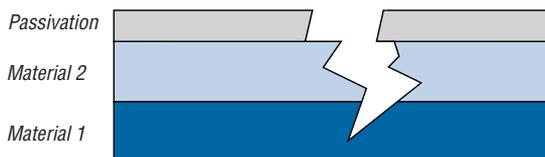
Figure 2. The Effects of Thermal Coefficient of Expansion on Two Materials



Because the materials are in contact with each other, the actual expansion of the two materials is a composite of the two. Both materials expand to the same length when placed together, which places extra stress on material 1. The materials act similarly during compression. As a result, shear stresses can occur at the joint between the two materials, which results in the passivation of metal layers.

When devices are repeatedly cycled between hot and cold temperature extremes, the shear stress of the materials change from compressive to tensile and back. If the temperature extremes are great enough, cracking and/or shear displacement of the materials could occur, resulting in displacement of the metal traces below the packaging layers. See [Figure 3](#).

Figure 3. Passivation Cracking & Layer Displacement



During this test, shear stresses are greatest at the corners of the die and are generally greater for larger die. Cracks in packaging can run down into the device, eventually breaking or severing metal layers or polysilicon below the passivation layer. Displaced metal traces cause leaking current or short circuits when metal lines are moved against other lines or power buses. To avoid these failures, Altera extensively tests devices following the procedure of test JESD22-A104-A.

To avoid these failures, Altera extensively tests devices following the procedures of test JESD22-A104-A. By following the device classifications shown in [Table 4](#) on [page 5](#), you can minimize the chance of this type of failure.

Humidity Bias Testing

The Steady-State Temperature Humidity Bias Life Test (JESD22A-101-B) evaluates the reliability of Altera devices in humid environments. The test uses temperature, humidity, and electrical bias to accelerate the penetration of moisture through device packages. The test is performed at 85 °C and 85% relative humidity with applied bias. This test can uncover flaws in device package material composition or package assembly.

The test is carried out in a temperature-humidity test chamber capable of maintaining continuous temperature and relative humidity levels. It must also provide electrical connections to the devices under test in a specified biasing configuration. The test is performed under extreme conditions. The failure rate can be extrapolated to typical conditions using equations that describe acceleration of failure mechanisms.

Altera uses two types of electrical biasing for testing: continuous bias and cycled bias.

In continuous electrical bias, DC bias is applied continuously. Continuous bias is more severe than cycled bias when die temperatures are $\leq 10\text{ }^{\circ}\text{C}$ higher than the chamber's ambient temperature or if die temperatures are not known when the power dissipation of the device is less than 200 mW. If the power dissipation of the device exceeds 200 mW, you should recalculate the die temperature (power \times thermal resistance). If this number is more than $5\text{ }^{\circ}\text{C}$ than the test specification, then you should use cycled bias. If the die temperature exceeds the chamber's ambient temperature by more than $5\text{ }^{\circ}\text{C}$, include the temperature difference in the test results because acceleration of failure mechanisms will be affected.

In cycled electrical bias, DC voltage applied to the devices is interrupted periodically with frequency and duty cycles. If biasing causes the temperature to rise $10\text{ }^{\circ}\text{C}$ above the chamber's ambient temperature, the cycled bias is more severe than continuous bias when optimized for a specific device type. Heating caused by power dissipation drives moisture away from the die and slows moisture-related failure. Cycled bias lets moisture collect on the die during the off periods. Cycling electrical bias with one hour on and one hour off is optimal for most devices.

HAST Testing

Highly Accelerated Stress Testing (HAST) (JESD22-A110-A) evaluates the reliability of Altera devices in humid environments. Like humidity bias testing, HAST testing uses a combination of electrical bias, high temperature, and high humidity. However, HAST testing also includes high pressure to accelerate corrosion-type failures. The test is performed at $130\text{ }^{\circ}\text{C}$ and 85% relative humidity with applied bias. HAST testing can uncover flaws in packaging material, seals, and joints between the package material and pins.

The electrical bias patterns used for HAST testing are similar to the ones used for humidity bias testing. The bias is used for powering the devices inside a HAST chamber. Wherever possible, an alternating sequence of V_{CC} and ground is used so that signal pins that are biased with one voltage are placed closest to signal pins that are biased with the opposite voltage. For HAST testing, V_{CC} is set to the minimal condition.

Specially designed boards are used in HAST chambers. Ordinary boards cannot be used because of severe HAST chamber conditions. For testing, Altera uses special polyimide printed circuit boards (PCBs) with buried traces.

Autoclave Testing

Autoclave (JESD22-A102-B) testing uses a temperature/humidity environment with no applied electrical bias to accelerate failure caused by metallization corrosion. This test subjects devices to saturated steam at 121 °C and 15 PSIG pressure. This pressure is “gauge” pressure, and is twice the atmospheric pressure of 15 PSI. The pressure can also be represented as two atmospheres. Autoclave testing tests the resistance of passivation layers on the die and exposes flaws in package design.

High pressure in autoclave testing drives water vapor through device packages until it reaches the die surface. Bond pads and poorly passivated metals can corrode. Several other failures can also occur. For example, non-volatile memory—using charge storage on floating gates (flash and EEPROM devices)—could be subject to charge loss from the floating gates. This charge loss is caused by moisture penetrating through passivation layers. If the moisture reaches the floating gate, it can quickly leak the stored charge off the floating gate. Altera uses the results of autoclave testing to minimize device failure.

Other failure mechanisms that can be aggravated are external package damage, shorts, or leakage paths. Improper rinsing/cleaning following lead finish can result in contamination migrating between the leads. This contamination causes leakage paths. Tin and lead migration, via dendritic growth from one lead to another, is another possible failure mechanism for autoclave testing.

Conclusion

To ensure a consistent level of quality, Altera subjects its plastic packaged devices to a series of EIA/JEDEC tests. These tests are designed to accelerate failure in devices, uncovering any process or design flaws in Altera devices. Altera uses the results of these tests to improve packages and minimize field failures. The information is useful to help designers match their stress and environment requirements and to establish guidelines for handling, soldering, classifying, and storing Altera devices.



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