Understanding MAX 7000 Timing

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Introduction

Altera® devices provide performance that is consistent from simulation to application. Before programming a device, you can determine the worst-case timing delays for any design. You can calculate propagation delays with either the MAX+PLUS® II Timing Analyzer or the timing models given in this application note and the timing parameters listed in individual device data sheets. Both methods yield the same results.

This application note defines internal and external timing parameters, and illustrates the timing models for the MAX® 7000 device family (including MAX 7000E, MAX 7000S, MAX 7000A, MAX 7000AE, and MAX 7000B devices).

Familiarity with device architecture and characteristics is assumed. Refer to specific device or device family data sheets in this data book for complete descriptions of the architectures, and for the specific values of the timing parameters listed in this application note.

Internal Timing Parameters

Within a device, the timing delays contributed by individual architectural elements are called internal timing parameters, which cannot be measured explicitly. All internal timing parameters are shown in italic type. The following section defines the internal timing parameters for the MAX 7000 device family and applies to all MAX 7000 devices unless otherwise indicated.

t_{IN} Dedicated input pad and buffer delay. t_{IN} represents the time required for a dedicated input pin to drive the input signal into the programmable interconnect array (PIA) or into the global control array.

t_{IO} I/O input pad and buffer delay. The t_{IO} delay applies to I/O pins used as inputs. t_{IO} is the delay from the I/O pin to the PIA.

t_{PIA} PIA delay. The delay incurred by routing a signal through the PIA.

t_{SEXP} Shared expander array delay. The delay of a signal through the `AND-NOT` structure of the shared expander product-term array that is fed back into the logic array.

t_{PEXP} Parallel expander delay. The additional delay incurred by adding parallel expander product terms to the macrocell product terms. For each group of up to five parallel expanders added to a single function, an additional t_{PEXP} delay is added to the timing path.

t_{GLOB} Global control delay. The delay from a dedicated input pin to any global control function in a macrocell or I/O control block.

t_{IOE} Internally generated output enable delay. The delay from an internally generated signal on the PIA to the output enable of the tri-state buffer.

t_{LAC} Logic array control delay. The AND array delay for register control functions such as preset, clear, and output enable.

t_{IC} Array clock delay. The delay through a macrocell's clock product term to the register's clock input.

t_{EN} Register enable delay. The AND array delay from the PIA to the register enable input.

t_{CLR} Register clear time. The delay from the assertion of the register's asynchronous clear input to the time the register output stabilizes at logical low.

t_{PRE} Register preset time. The delay from the assertion of the register's asynchronous preset input to the time the register output stabilizes at logical high.

t_{LAD} Logic array delay. The time a logic signal requires to propagate through a macrocell's AND-OR-XOR structure.

t_{RD} Register delay. The delay from the rising edge of the register's clock to the time the data appears at the register output.

t_{SU} Register setup time, for data and enable signals before clock. The time required for a signal to be stable at the register's data and enable inputs before the register clock's rising edge to ensure that the register correctly stores the input data.

t_{H} Register hold time, for data and enable signals after clock. The time required for a signal to be stable at the register's data and enable inputs after the register clock's rising edge to ensure that the register correctly stores the input data.

t_{FSU} Fast-input register setup time. When the fast-input register is used, t_{FSU} is the time required for a signal to be stable at the register's data and enable inputs before the register clock's rising edge to ensure that the register correctly stores the input data.

t_{FH} Fast-input register hold time. When the fast-input register is used, t_{FH} is the time required for a signal to be stable at the register's data and enable inputs after the register clock's rising edge to ensure that the register correctly stores the input data.

t_{FIN} Fast input delay. The delay from the I/O pin to the macrocell register when fast input registers are used.

t_{COMB} Combinatorial buffer delay. The delay from the time when a combinatorial logic signal bypasses the programmable register to the time it becomes available at the macrocell output.

t_{OD1} Output buffer and pad delay with the slow slew rate logic option turned off and $V_{CCIO} = V_{CCINT}$.

t_{OD2} Output buffer and pad delay with the slow slew rate logic option turned off and V_{CCIO} = low voltage.

t_{OD3} Output buffer and pad delay with the slow slew rate logic option turned on.

t_{XZ} Output buffer disable delay. The delay required for high impedance to appear at the output pin after the output buffer's enable control is disabled.

t_{ZX1} Output buffer enable delay with the slow slew rate logic option turned off and $V_{CCIO} = V_{CCINT}$. The delay required for the output signal to appear at the output pin after the tri-state buffer's enable control is enabled.

t_{ZX2} Output buffer enable delay with the slow slew rate logic option turned off and V_{CCIO} = low voltage. The delay required for the output signal to appear at the output pin after the tri-state buffer's enable control is enabled.

t_{ZX3} Output buffer enable delay with the slow slew rate logic option turned on. The delay required for the output signal to appear at the output pin after the tri-state buffer's enable control is enabled.

t_{LPA} Low-power adder. The delay associated with macrocells in low-power operation. In low-power mode, t_{LPA} must be added to the logic array delay (t_{LAD}), the register control delay (t_{LAC}, t_{IC}, t_{ACL}, or t_{EN}), and the shared expander delay (t_{SEXP}) paths.

External Timing Parameters

External timing parameters represent actual pin-to-pin timing characteristics. Each external timing parameter consists of a combination of internal timing parameters. The data sheet for each device gives the values of the external timing parameters. These external timing parameters are worst-case values, derived from extensive performance measurements and ensured by testing. All external timing parameters are shown in bold type. The following list defines external timing parameters for MAX 7000 devices.

t_{PD1} Dedicated input pin to non-registered output delay. The time required for a signal on any dedicated input pin to propagate through the combinatorial logic in a macrocell and appear at an external device output pin.

t_{PD2} I/O pin input to non-registered output delay. The time required for a signal on any I/O pin input to propagate through the combinatorial logic in a macrocell and appear at an external device output pin.

t_{PZX} Tri-state to active output delay. The time required for an input transition to change an external output from a tri-state (high-impedance) logic level to a valid high or low logic level.

t_{PXZ} Active output to tri-state delay. The time required for an input transition to change an external output from a valid high or low logic level to a tri-state (high-impedance) logic level.

t_{CLR} Time to clear register delay. The time required for a low signal to appear at the external output, measured from the input transition.

t_{SU} Global clock setup time. The time that data must be present at the input pin before the global (synchronous) clock signal is asserted at the clock pin.

t_{H} Global clock hold time. The time that data must be present at the input pin after the global clock signal is asserted at the clock pin.

t_{FSU} Fast-input clock setup time. When the fast-input path is used, **t_{FSU}** is the time that data must be present at the input pin before the global (synchronous) clock signal is asserted at the clock pin.

t_{FH} Fast-input clock hold time. When the fast-input path is used, t_{FH} is the time that data must be present at the input pin after the global clock signal is asserted at the clock pin.

t_{CO1} Global clock to output delay. The time required to obtain a valid output after the global clock is asserted at the clock pin.

t_{CNT} Minimum global clock period. The minimum period maintained by a globally clocked counter.

t_{ASU} Array clock setup time. The time data must be present at an input pin before an array (asynchronous) clock signal is asserted at the input pin.

t_{AH} Array clock hold time. The time data must be present at an input pin after an array clock signal is asserted at the input pin.

t_{ACO1} Array clock to output delay. The time required to obtain a valid output after an array clock signal is asserted at an input pin.

t_{ACNT} Minimum array clock period. The minimum period maintained by a counter when it is clocked by a signal from the array.

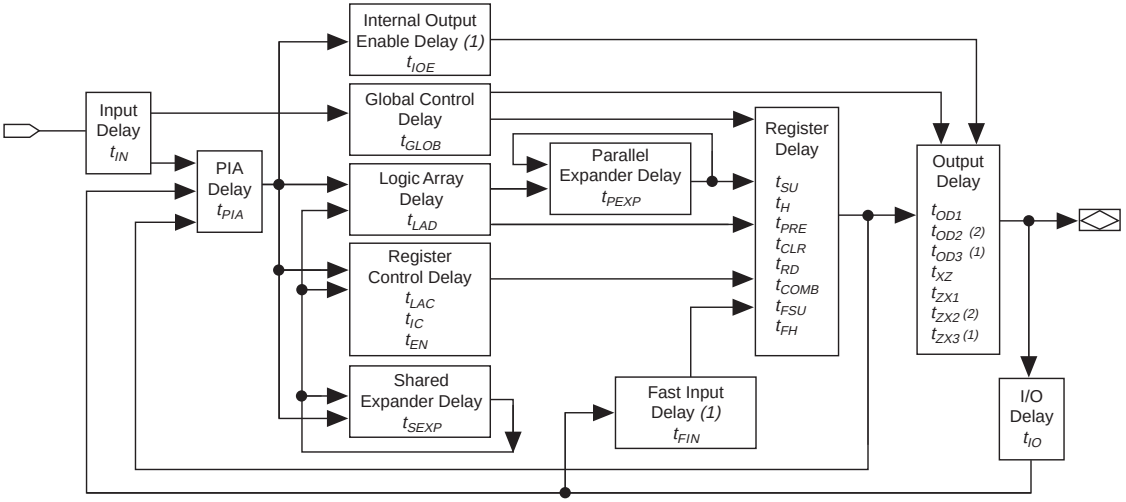
Timing Models

Timing models are simplified block diagrams that illustrate the propagation delays through Altera devices. Logic can be implemented on different paths. You can trace the actual paths used in your design by examining the equations listed in the MAX+PLUS II Report File (**.rpt**) for the project. You can then add up the appropriate internal timing parameters to calculate the propagation delays through the device.

The MAX 7000 architecture has globally routed register clock, clear, and tri-state buffer output enable signals. Two types of expander product terms—shared and parallel—can be used to implement complex logic. Each macrocell can be set for low-power operation to reduce power dissipation in the device.

Figure 1 shows the timing model for MAX 7000 devices.

Figure 1. MAX 7000 Device Timing Model



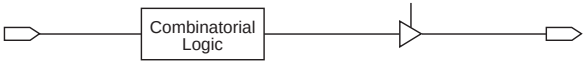
Notes:
(1) This parameter is available in MAX 7000E, MAX 7000S, MAX 7000A, MAX 7000AE, and MAX 7000B devices only.
(2) This parameter is not available in 44-pin devices.

Calculating Timing Delays

You can calculate pin-to-pin timing delays for any device with the appropriate timing model and internal timing parameters. Each external timing parameter is calculated from a combination of internal timing parameters. Figure 2 shows the external timing parameters for the MAX 7000 device family. To calculate the delay for a signal that follows a different path through the device, refer to the timing models shown in Figure 1 to determine which internal timing parameters to add together.

Figure 2. External Timing Parameters (Part 1 of 3)

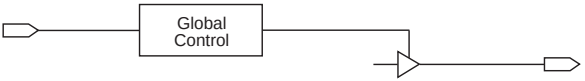
Combinatorial Delay



$$t_{PD1} = t_{IN} + t_{PIA} + t_{LAD} + t_{COMB} + (t_{OD1} \text{ or } t_{OD2} \text{ or } t_{OD2})$$

$$t_{PD2} = t_{IO} + t_{PIA} + t_{LAD} + t_{COMB} + (t_{OD1} \text{ or } t_{OD2} \text{ or } t_{OD3})$$

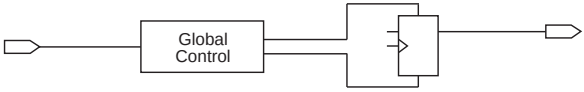
Tri-State Enable/Disable Delay



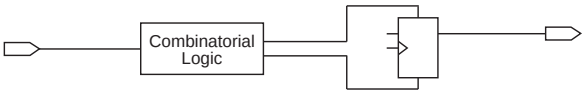
$$t_{PXZ}, t_{PZX} = t_{IN} + t_{GLOB} + (t_{XZ} \text{ or } t_{ZX1} \text{ or } t_{ZX2} \text{ or } t_{ZX3})$$

Figure 2. External Timing Parameters (Part 2 of 3)

Register Clear & Preset Time

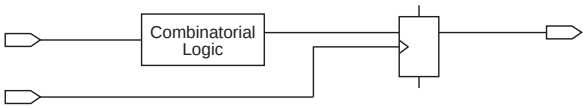


$$t_{GCLR} = t_{IN} + t_{GLOB} + t_{CLR} + (t_{OD1} \text{ or } t_{OD2} \text{ or } t_{OD3})$$



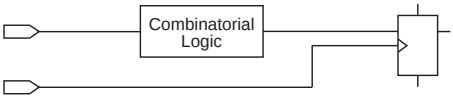
$$t_{PRE}, t_{CLR} = t_{IN} + t_{PIA} + t_{LAC} + (t_{PRE} \text{ or } t_{CLR}) + (t_{OD1} \text{ or } t_{OD2} \text{ or } t_{OD3})$$

Setup Time



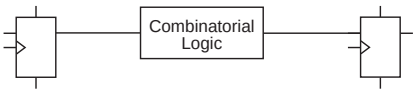
$$t_{SU} = (t_{IN} + t_{PIA} + t_{LAD}) - (t_{IN} + t_{GLOB}) + t_{SU}$$

Hold Time



$$t_{H} = (t_{IN} + t_{GLOB}) - (t_{IN} + t_{PIA} + t_{LAD}) + t_{H}$$

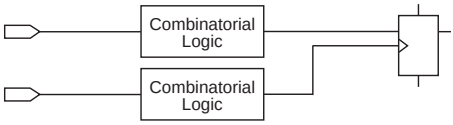
Counter Frequency



$$t_{CNT} = t_{RD} + t_{PIA} + t_{LAD} + t_{SU}$$

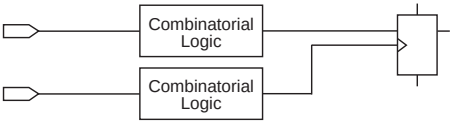
Figure 2. External Timing Parameters (Part 3 of 3)

Asynchronous Setup Time



$$t_{ASU} = (t_{IN} + t_{PIA} + t_{LAD}) - (t_{IN} + t_{PIA} + t_{IC}) + t_{SU}$$

Asynchronous Hold Time

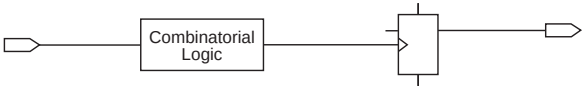


$$t_{AH} = (t_{IN} + t_{PIA} + t_{IC}) - (t_{IN} + t_{PIA} + t_{LAD}) + t_{H}$$

Clock-to-Output Delay

$$t_{CO1} = t_{IN} + t_{GLOB} + t_{RD} + (t_{OD1} \text{ or } t_{OD2} \text{ or } t_{OD3})$$

Array Clock-to-Output Delay



$$t_{ACO1} = t_{IN} + t_{PIA} + t_{IC} + t_{RD} + (t_{OD1} \text{ or } t_{OD2} \text{ or } t_{OD3})$$

Examples

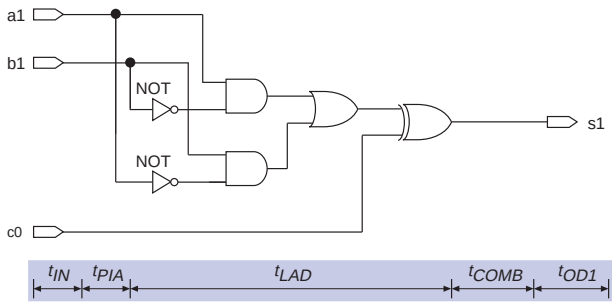
The following examples show how to use internal timing parameters to calculate the delays for real applications.

Example 1: First Bit of 7483 TTL Macrofunction

You can analyze the timing delays for macrofunctions that have been subjected to minimization and logic synthesis. A MAX+PLUS II Report File (**.rpt**) that includes the optional Equations Section lists the synthesized logic equations for the project. These equations are structured so you can quickly determine the logic implementation of any signal. For example, Figure 3 shows part of a 7483 TTL macrofunction (a 4-bit full adder). The Report File gives the following equations for s1, the least significant bit of the adder:

```
s1      = OUTPUT (_LC021, VCC);
_LC021  = LCELL (_EQ026 $ C0);
_EQ026  = b1 & !a1
        # !b1 & a1;
```

Figure 3. Adder Logic Timing for MAX 7000 Architecture



The s1 output is the output of macrocell 21 (_LC021), which contains combinatorial logic. The combinatorial logic LCELL(_EQ026 $ C0) represents the XOR of the intermediate equation _EQ026 and the carry-in, c0. In turn, _EQ026 is logically equivalent to the XOR of inputs b1 and a1. Therefore, the timing delay for s1 in MAX 7000 devices is as follows:

$$t_{IN} + t_{PIA} + t_{LAD} + t_{COMB} + t_{OD1}$$

Example 2: Second Bit of 7483 TTL Macrofunction

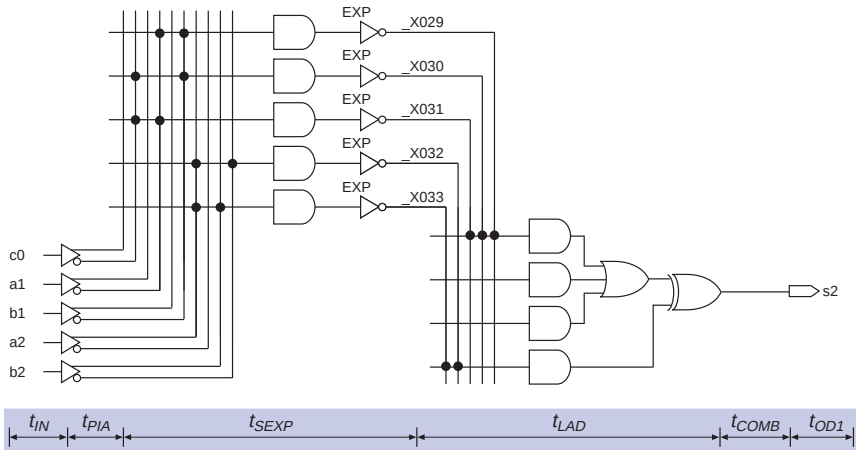
For complex logic that requires expanders (represented as _X<*number*> in MAX+PLUS II Report Files), the expander array delay, t_{SEXP}, is added to the delay element. The second bit of the 7483 adder macrofunction, s2, requires shared expanders. The equations are as follows:

```
s2      = _LC019;
_LC019  = LCELL(_EQ023 $ _EQ024 );
_EQ023  = _X029 & _X030 & _X031;
_X029   = EXP(!b1 & !a1);
_X030   = EXP(!b1 & !c0);
_X031   = EXP(!a1 & !c0);
_EQ024  = _X032 & _X033;
_X032   = EXP(!b2 & a2);
_X033   = EXP(b2 & a2);
```

Figure 4 shows how you can map the logic structure onto the MAX 7000 architecture with these equations. The timing delay for s2 in MAX 7000 devices is as follows:

$$t_{IN} + t_{PIA} + t_{SEXP} + t_{LAD} + t_{COMB} + t_{OD1}$$

Figure 4. Adder Equations Mapped to MAX 7000 Architecture



Example 3: Second Bit of 7483 TTL Macrofunction with Parallel Expanders

The MAX+PLUS II Compiler implements logic with parallel expanders if the Parallel Expanders logic option is turned on when a project is compiled for MAX 7000 devices. When parallel expanders are used, none of the shareable expanders are used, so the timing delay for the `s2` bit of the `7483` becomes:

$$t_{IN} + t_{PIA} + t_{LAD} + t_{PEXP} + t_{COMB} + t_{OD1}$$

Example 4: First Bit of 7483 TTL Macrofunction in Low-Power Mode

If a MAX 7000 device macrocell is set for low-power mode, you must add the low-power adder delay to the total delay through that macrocell. Thus, the `s1` delay in Figure 3 becomes:

$$t_{IN} + t_{PIA} + t_{LPA} + t_{LAD} + t_{COMB} + t_{OD1}$$

Conclusion

The MAX 7000 architecture has fixed internal timing delays that are independent of routing. Therefore, you can determine the worst-case timing delays for any design before programming a device. Total delay paths can be expressed as the sums of internal timing delays. Timing models illustrate the internal delay paths for devices and show how these internal timing parameters affect each other. You can use the MAX+PLUS II Timing Analyzer to automatically calculate delay paths, or hand-calculate delay paths by adding the internal timing parameters for an appropriate timing model. With the ability to predict worst-case timing delays, you can be confident of a design's in-system timing performance.