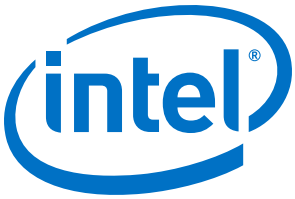

AN 721: Creating an FPGA Power Tree

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Creating an FPGA Power Tree

An FPGA power tree is a graphical representation of your system's power management architecture. The power tree shows the main supply power flow through a tree of power converters that convert the main supply power to the voltage and current required to drive various loads. Every FPGA design has unique power consumption requirements requiring a unique power tree. This topic describes optimizing an FPGA power tree for your FPGA design.

FPGAs have several inputs requiring power for the FPGA to operate. These inputs produce power to various resource blocks within the FPGA, including logic, RAM, digital signal processing (DSP), phase-locked loops (PLLs), clocks, I/Os, and transceivers. These resource blocks have static and dynamic power requirements that vary by your selected FPGA and utilization. Your selected FPGA does not have a fixed power requirement. The total power consumption, and your FPGA power tree, depends on your design. To create an FPGA tree:

1. Obtain power requirements with the Early Power Estimator (EPE).
2. Determine the power tree input supply voltage.
3. Extract power rails.
4. Group power rail inputs.
5. Select power converters.

Related Information

- Intel® Enpirion® Power Solutions
- Intel Intel FPGAs and Programmable Devices

Obtaining Power Requirements with the Early Power Estimator

Your FPGA's power consumption is determined by the implementation of your FPGA design. Design components such as logic requirements, the quantity and type of I/Os, the quantity and speed of transceivers, and the use of other FPGA features contribute to your FPGA's power consumption. You must understand your FPGA power requirements to create an FPGA power tree.

1. Calculate your FPGA power requirements with the Microsoft Excel-based Early Power Estimator (EPE) spreadsheet.
2. Estimate power consumption at any point in your design cycle, including before you begin your design, or before your design is complete.

   The EPE spreadsheet allows you to submit estimates of how you will use the various resource blocks in your FPGA. When you enter your estimates, the EPE spreadsheet automatically estimates the required power consumption. For detailed information on using the EPE spreadsheet, see the *Early Power Estimator for Intel® Arria® 10 User Guide*.

Intel recommends switching from the EPE spreadsheet to the Power Analyzer in the Intel Quartus® Prime software when your design is available. The Power Analyzer can access the implemented design details to produce more accurate results. For detailed information on using the Power Analyzer, refer to*Intel Quartus Prime Pro Edition User Guide: Power Analysis and Optimization*.

Related Information

- Early Power Estimator on page 9
- Early Power Estimators and Power Analyzers
- Early Power Estimator for Intel Arria 10 User Guide
- Intel Quartus Prime Pro Edition User Guide: Power Analysis and Optimization

Power Tree Input Supply Voltage

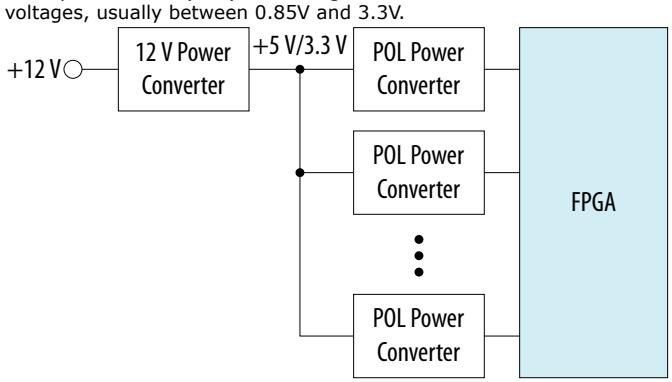
Determine the input supply voltage before creating an FPGA power tree. Systems typically favor one of two implementations: a 12V input source, or a low voltage (5V or 3.3V) input source.

Most FPGA inputs require a voltage of ≤3.3V. Building an FPGA power tree from a low voltage input source often allows for a smaller, more efficient system. If you use an input source of 12V or higher, or if the Early Power Estimator (EPE) spreadsheet estimates the total FPGA current consumption is very high, Intel recommends that you use a two-stage voltage solution, where:

- A first-stage power converter converts a high voltage to a lower intermediate voltage, and
- A second-stage power converter converts the intermediate voltage to the final FPGA input voltages

Figure 1. Two-Stage FPGA Power Tree

This two-stage FPGA power tree voltage solution allows you to power the FPGA inputs with efficient, low-voltage converters. The figure shows a 12V power converter converting the input supply to a lower 5V or 3.3V intermediate voltage. The point of load (POL) low-voltage converter then converts the intermediate voltage to the final FPGA input voltages, usually between 0.85V and 3.3V.



You must determine the input supply voltage and voltage architecture before you select power converters.

Related Information

Power Converters on page 8

Power Rails

You should extract the power rails that your design requires. Your power tree only needs to supply power to the used power rails. It is unlikely that all of your FPGA resource blocks are in use, even in a heavily-loaded design.

The **Report** tab in the Early Power Estimator (EPE) spreadsheet describes the expected voltage and current requirements for each FPGA power rail based on your design. The EPE spreadsheet indicates which FPGA power rails require a power supply in two ways:

- The FPGA input line has a non-zero value in the **Total Current (A)** column.
- For EPE spreadsheet versions 18.0 and later, the FPGA input line has an assigned (not gray) entry in the **Power Regulator Settings Regulator Group** column next to the **Total Current (A)** column.

Figure 2. I_{CCIO} Section Call Out from the EPE Spreadsheet Report Tab

This figure shows the **Report** tab of the EPE spreadsheet highlighting utilized inputs. Some inputs, such as FPGA I/O (I_{CCIO}), are generic inputs that may have a total current value that is the sum of the currents required for various I/O inputs at different voltage levels. In this case, while the individual I_{CCxx} rows indicate the various I/O input currents at each voltage level. In this example, you must use different power rail groupings for the I_{CCIO} (1.2 V) and I_{CCIO} (1.8 V) power rails.

	User Mode Current Requirement					Power Regulator Settings
Power Supply	Static Current (A)	Standby Current (A)	Dynamic Current (A)	Total Current (A)	Recommended Margin	Regulator Group
V_{CC}						
V_{CC} (0.90V)	2.264	-	3.099	5.363	19%	1
V_{CC} (0.95V)						
V_{CCP}						
V_{CCP} (0.90V)	0.211	0.021	0.589	0.820	25%	1
V_{CCP} (0.95V)						
V_{CCERAM}						
V_{CCERAM} (0.90V)	0.030	-	0.078	0.108	5%	1
V_{CCERAM} (0.95V)						
V_{CCA_PLL} (1.80V)	0.028	0.002	0.006	0.036	25%	3
V_{CCPT} (1.80V)	0.267	0.006	0.009	0.282	25%	3
V_{CCIO}						
V_{CCIO} (1.20V)	3.58E-04	1.63E-04	0.011	0.011	25%	4
V_{CCIO} (1.25V)						
V_{CCIO} (1.35V)						
V_{CCIO} (1.50V)						
V_{CCIO} (1.80V)	0.002	0.003	0.003	0.008	25%	3
V_{CCIO} (2.50V)						
V_{CCIO} (3.00V)						
V_{CCH_GXB} (1.80V)	0.112	0.543	0.701	1.356	15%	3
V_{CCT_GXB}						
V_{CCT_GXB} (0.95V)	0.087	0.057	1.231	1.375	15%	2
V_{CCT_GXB} (1.03V)						
V_{CCT_GXB} (1.12V)						
V_{CCR_GXB}						
V_{CCR_GXB} (0.95V)	0.175	0.062	0.925	1.162	15%	2
V_{CCR_GXB} (1.03V)						
V_{CCR_GXB} (1.12V)						
V_{CCL_HPS}						
V_{CCL_HPS} (0.90V)						
V_{CCL_HPS} (0.95V)						
V_{CCIO_HPS}						
V_{CCIO_HPS} (1.80V)						
V_{CCIO_HPS} (2.50V)						
V_{CCIO_HPS} (3.00V)						
V_{CCPLL_HPS} (1.80V)						
$V_{CCIOREF\_HPS}$ (1.80V)						
V_{CCPGM} (1.20V)	1.12E-05	-	-	1.12E-05	25%	4
V_{CCBAT} (1.20V)	8.00E-05	-	-	8.00E-05	25%	4

You must identify the power rails requiring power in your design before creating a group of the power rails.

Related Information

Power Rail Inputs on page 6

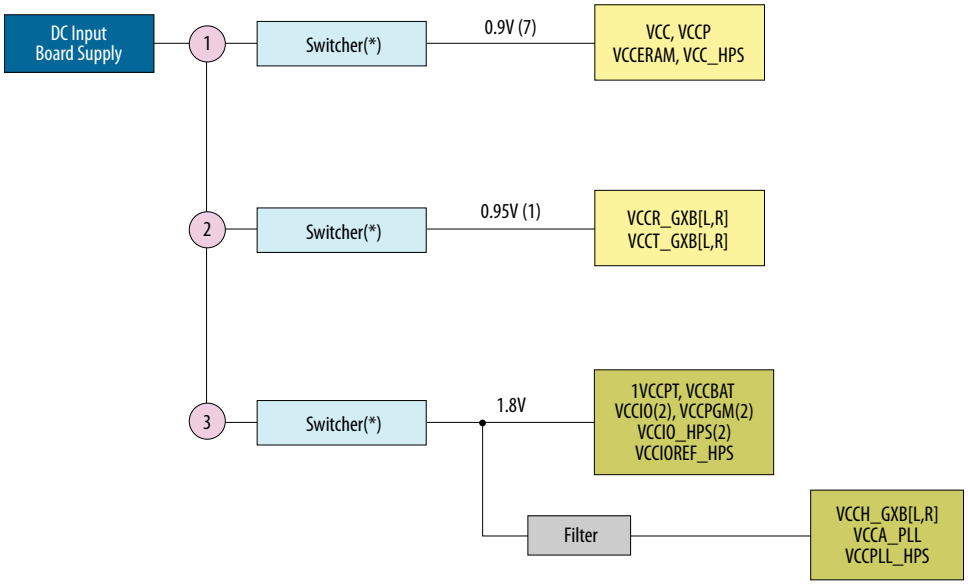
Power Rail Inputs

Intel FPGAs have several inputs requiring power, but each input does not necessarily require a dedicated power converter. You can place multiple inputs together in a group with a single regulator supplying the sum total of the power. Creating a group of these inputs can reduce the space used on your PCB and reduce your system costs. When creating your FPGA power tree, you should create a group of all relevant extracted FPGA power rails for use with a single regulator.

Refer to the *Pin Connection Guidelines* for your selected Intel FPGA to determine what inputs you can group together; the *Pin Connection Guidelines* recommend a power supply block architecture for each FPGA configuration and provide details about each input pin required during hardware design.

Figure 3. Example Power Sharing Guidelines

This figure shows Intel Arria 10 SX Device with Transceiver Data Rates ≤ 11.3 Gbps for Chip-to-Chip application Thsi figure shows a recommended Intel Arria 10 power tree. Refer to the *Intel Arria 10 GX, GT, and SXDevice Family Pin Connection Guidelines.*



Note:

1. When using a switcher to supply these voltages, the switcher must be a low noise switcher as defined in note 7 in the notes in the *Intel Arria 10 SX Pin Connection Guidelines*.
2. The supported tolerance for the VCCIO power supply varies depending on the I/O standards. For more details, refer to the I/O standard specification in the *Intel Arria 10 Device Datasheet*. Use the EPE tool to determine the power required for your specific design.
3. Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements.

Intel suggests power rail groupings in the *Pin Connection Guidelines* for each Intel FPGA, but there are two other factors to consider when grouping your power rails. First, each of the FPGA power rail inputs in a group must have the same supply voltage requirement. This limitation is important for FPGA resource blocks such as I/O inputs that might require different voltages depending on the specific interface protocols used in your design. For example, a PCI Express® (PCIe®) I/O interface

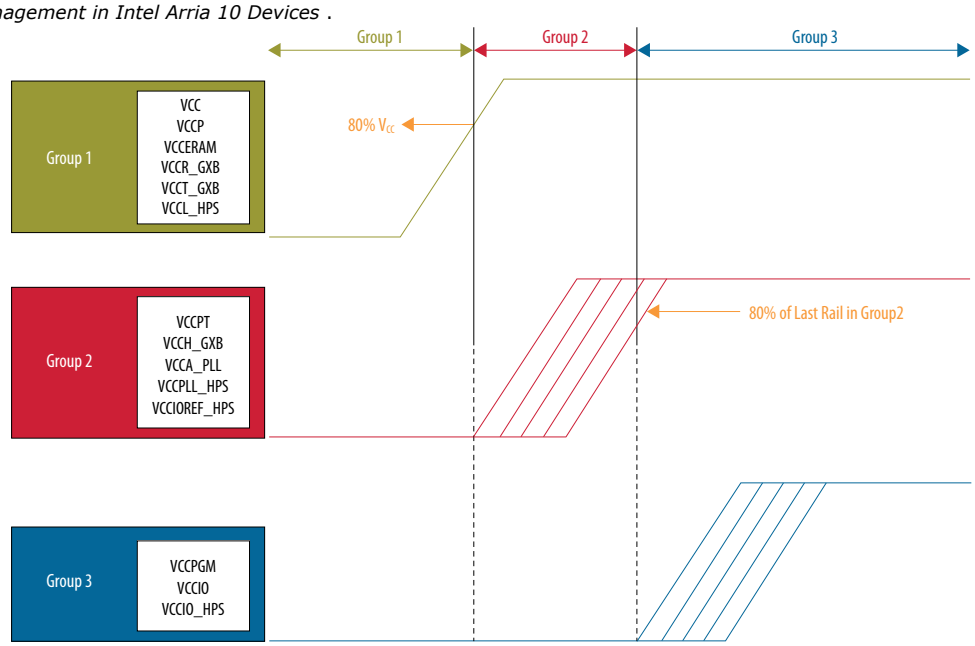
might require a 3 V input supply and an LVDS I/O interface might require a 2.5 V input supply; while both are I/O inputs, and the *Pin Connection Guidelines* simplified the I/O inputs as a single VCCIO rail, these two I/O inputs must be powered by different converters.

The second power rail grouping factor to consider is power-up sequencing. Not every FPGA or system requires power-up sequencing, but many advanced FPGAs require that power is supplied to various inputs in a specific order during system power-up. You can locate the power-up sequence guidelines for your selected Intel FPGA in the device's *Pin Connection Guidelines* or *Handbook*. If your design requires power-up sequencing, you must ensure that grouped power rail inputs meet the sequence requirements for your Intel FPGA. You cannot provide power to a power rail if it depends upon another rail in the same group or a rail in a later group.

You can provide power to any inputs in your design individually, or in combination with another group of FPGA inputs that share their voltage and sequencing requirements.

Figure 4. Power-Up Sequence Requirement for Intel Arria 10 Devices

This figure shows power-up sequence requirements for the Intel Arria 10 V device as described in *Power Management in Intel Arria 10 Devices* .



Once you determine your power rail input groupings, use the Early Power Estimator (EPE) spreadsheet to determine the total power required for the input group. The EPE spreadsheet combines the current requirements for each load by summing each FPGA input's current requirement. The result are in in the **Total Current (A)** column in the EPE spreadsheet **Report** tab.

Figure 5. Power Groups in the EPE

	User Mode Current Requirement					Power Regulator Settings
Power Supply	Static Current (A)	Standby Current (A)	Dynamic Current (A)	Total Current (A)	Recommended Margin	Regulator Group
V_{CC}						
V_{CC} (0.90V)	2.264	-	3.099	5.363	19%	1
V_{CC} (0.95V)						
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V_{CCP} (0.90V)	0.211	0.021	0.589	0.820	25%	1
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V_{CCL_HPS} (0.90V)						
V_{CCL_HPS} (0.95V)						
V_{CCIO_HPS}						
V_{CCIO_HPS} (1.80V)						
V_{CCIO_HPS} (2.50V)						
V_{CCIO_HPS} (3.00V)						
V_{CCPLL_HPS} (1.80V)						
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V_{CCPGM} (1.20V)	1.12E-05	-	-	1.12E-05	25%	4
V_{CCBAT} (1.20V)	8.00E-05	-	-	8.00E-05	25%	4

In the EPE spreadsheet you can group inputs at any point in your design cycle, including before you start your design, or before your design is complete.

Related Information

- Power Rails on page 5
- Pin Connection Guidelines
- Intel Arria 10 GX, GT, and SX Device Family Pin Connection Guidelines
- Power Management in Intel Arria 10 Devices
- Early Power Estimators and Power Analyzers
- Early Power Estimator for Intel Arria 10 User Guide

Power Converters

After determining your FPGA power tree architecture and power requirements, you must select your power converters; every FPGA power rail input group requires a power converter. The converters must meet the minimum electrical requirements for input voltage, output voltage, and output load current.

Once you determine what converters meet the minimum electrical requirements, you must prioritize your system requirements, including size, efficiency, switching frequency, power supply noise, and cost. Optimizing some parameters or resources may degrade the performance of others. For example, increasing the switching frequency allows for a smaller system size with lower switching noise in critical frequency bands, but higher switching frequency requires more DC-DC switching and reduces efficiency by generating more switching loss. The Intel Enpirion® power solutions use special design techniques and laterally diffused metal oxide semiconductor technology to reduce loss at high switching frequencies to minimize this trade-off.

Figure 6. Equations Relating Switching Frequency, Inductance, Capacitance, and Switch Loss

These four equations can help you prioritize your system requirements. Equation *a* describes how inductance gets smaller with higher switching frequencies. Lower inductance enables the use of smaller, more efficient inductors. Equations *b* and *c* illustrate that input and output capacitance are smaller with higher switching frequency. Lower capacitance generally enables the use of smaller, cheaper capacitors. Equation *d* represents power loss, or a combination of conduction losses and switching losses. Power loss, even at high switching frequencies, can be minimized by Intel Enpirion devices designed to minimize C_{ISS} and C_{OSS}.

a. $$L = \frac{V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{\Delta I_{OUT} F_{SWITCH}}$$

b. $$C_{IN} = \frac{D(1 - D)}{\Delta V_{IN} F_{SWITCH}}$$

c. $$C_{OUT} = \frac{\Delta I_{OUT}}{\Delta V_{OUT} F_{SWITCH}}$$

d. $$P_{LOSS} = \underbrace{I^2 R_{ON}}_{\text{Conduction Losses}} + \underbrace{C_{ISS} V_{GS}^2 F_{SW} + C_{OSS} V_{DS}^2 F_{SW}}_{\text{Switching Losses}}$$

Where:
F_{SWITCH} is the switching converter switching frequency
ΔI_{OUT} is the change in current (ripple)
D is the switching converter duty cycle
R_{ON} is the MOSFET on resistance
C_{ISS} is the MOSFET equivalent input capacitance
C_{OSS} is the MOSFET equivalent input capacitance

System priorities also vary depending upon the load. For example, the FPGA core power rail input (V_{CC}) requires high power supply accuracy and low ripple to meet tight tolerance specifications, while power supply noise is a key parameter for sensitive power rails (such as transceiver voltage rails) to minimize both jitter and the bit error rate (BER).

Some power management decisions impact designs at the system level and must be considered early in the design process for successful implementation in the final system design. Some components support more advanced system power management and FPGA power reduction techniques; these components typically require special interfaces and feature sets that you should specify early in the FPGA design process. For example, you can include Enpirion power solutions that support SmartVID in Intel Arria 10 10 device designs, or use Intel Enpirion digital controllers and PowerSoCs with a PMBus interface to implement system telemetry.

Related Information

Intel Enpirion Power Solutions

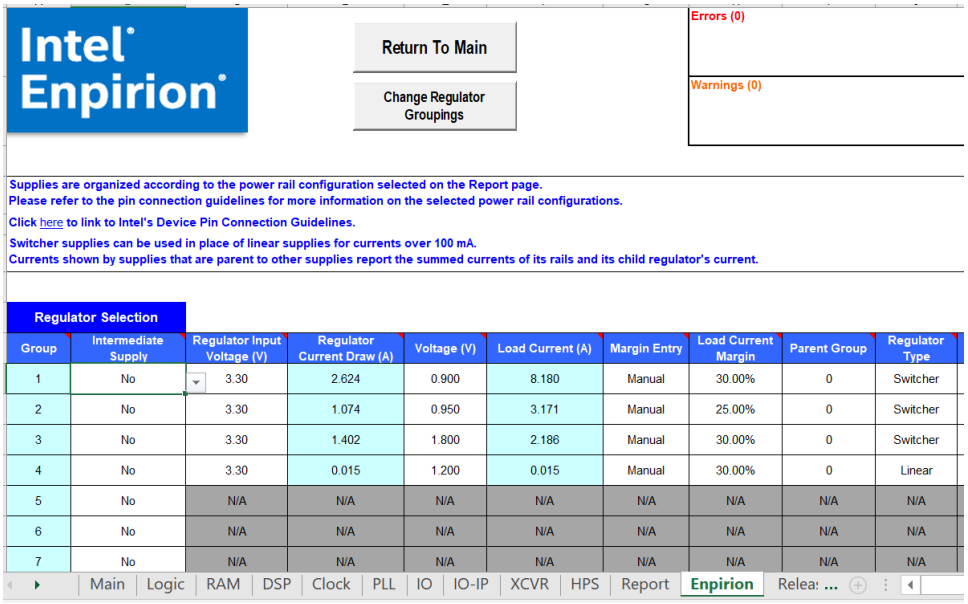
Early Power Estimator

Intel added power converter groupings and recommendations to Early Power Estimator (EPE) versions 13.1 and later. The EPE tool automatically and seamlessly groups relevant FPGA power rails according to the recommendations in your selected Intel FPGA's *Pin Connection Guidelines*. Based on the resulting current requirements, the EPE recommends Intel Enpirion power solutions that best meet your requirements. The **Enpirion** tab of the EPE spreadsheet shows the recommended power solution.

The **Report** tab of the PowerPlay EPE spreadsheet allows you to manually adjust groupings based on your design. Modifications can include: using I/O protocols at different voltages; separating sensitive rails; and implementing sequencing.

The **Enpirion** tab allows you to adjust the power solution recommendations based on your design priorities. Modifications can include: selecting rails to choose a low-dropout (LDO) regulator for lower noise or lower cost; and selecting devices with a "Power Good" (POK) flag for sequencing or other fault monitoring.

Figure 7. The Intel Enpirion Tab in the EPE Spreadsheet



Related Information

- FPGA Pin Connection Guidelines
- Early Power Estimator for Intel Arria 10 User Guide
- Early Power Estimators and Power Analyzers

Document Revision History for AN 721: Creating an FPGA Power Tree

Table 1. Document Revision History for AN 721: Creating an FPGA Power Tree

Date	Changes
2019.06.30	• Updated hyperlinks • Updated EPE example for Intel Arria 10 devices • Deleted *Online Power Grouping Tool* section .
October 2014	Initial release.