White Paper

FPGA
Direct RF

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Altera® Analog-Enabled Direct-RF Device Portfolio

Altera delivers a Game-Changing Portfolio of Analog-Enabled Agilex™ 9 FPGAs Direct RF-Series, Structured ASICs, and ASICs

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Introduction

Usually, people discussing "The Edge" are talking about the farthest reaches of a network, whether it's the Internet, cellular telecommunications, cable television, or some other type of communications network. Large and small cloud data centers process data received from the edge, but often, distributed processing is required at the edge to enable low-latency, real-time processing.

This paper focuses on data passed between the radio frequency (RF) and digital domains at the edge. Digital information is encoded into and decoded from RF waves using analog-to-digital converters (ADCs) and digital-to-analog converters (DACs). Advancing converter technology has enabled higher sample rates that permit larger portions of the RF spectrum to be directly accessed in an agile manner, allowing more information to be captured and transmitted at the edge. To date, RF analog conversion has been a difficult engineering problem to solve due to technology and manufacturing limitations. Solutions, when feasible at all, have been large, heavy, and have consumed significant amounts of power.

Intel has created a new portfolio of analog-enabled Intel Agilex® 9 FPGA Direct-RF Series, structured ASICs, and ASICs that can perform direct analog RF signal conversion for multiple analog input and output channels at groundbreaking rates as fast as 12 gigasamples/sec (Gsps) over sixteen channels, and 64 Gsps over as many as eight channels. These new Direct-RF Series FPGAs enable optimized edge solutions for many RF applications.

Solving Difficult Problems

The programmable logic devices in this new Direct-RF Series FPGA portfolio employ Intel's embedded multi-die interconnect bridge (EMIB) and Advanced Interconnect Bus (AIB) tile (chiplet) interconnect technology to combine RF-capable ADCs and DACs with Intel® Stratix® 10 FPGA and Intel Agilex® 9 FPGA die. EMIB and AIB packaging technologies currently provide the lowest possible latency and power consumption when converting between the analog and digital domains.

Combined with Intel's heterogeneous chiplet-based architecture, these interface standards allow analog tiles to be integrated with advanced FPGA die and enable the design of composable systems in packages with very high performance and low operating power that far outperform the abilities of systems built with conventional monolithic IC technology in multiple discrete chip packages. These technologies also allow Intel to offer a comprehensive portfolio of packaged, integrated direct RF conversion products that bridge the analog RF and digital domains much better than earlier RF technologies, while simultaneously improving figures of merit along size, weight, and power (SWAP) dimensions.

Initially, the Direct-RF Series FPGA portfolio includes members of the Intel Agilex 9 SoC FPGA and Intel Stratix 10 SoC FPGA families. These devices deliver a game-changing combination of performance-per-watt and performance-per-area while providing system developers with great design flexibility. These solutions combine several important Intel innovations representing semiconductor technology leadership in multiple areas and they deliver significant value to end-product development at

the edge. Further, these devices have relatively small form factors that fit into RF edge applications that previously could not be built, thereby giving RF edge equipment a much-needed upgrade to access more data than ever before.

Intel Stratix 10 and Intel Agilex 9 FPGAs combine FPGA core die, fabricated with the Intel 14 nm and 10 nm SuperFin manufacturing processes respectively, with function specific and general-purpose I/O tiles using Intel's EMIB, AIB, and advanced chiplet-based semiconductor packaging technologies. Different semiconductor tiles provide these Intel FPGAs with a variety of additional I/O functionality including high bandwidth memory (HBM) DRAM, PCIe 4.0 and 5.0, and 58/116 Gbps serial transceiver ports that allow these Intel FPGAs to interface with a wide variety of devices. Figure 1 illustrates the construction of an Intel Agilex 9 FPGA.

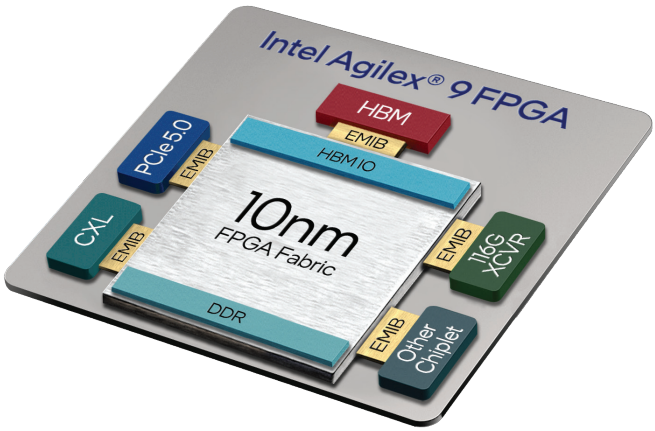

Figure 1. The construction of an Intel Agilex 9 FPGA relies on the use of semiconductor tiles, EMIB, and chiplet-based packaging technology

In Figure 1 above, the central FPGA fabric die connects with five surrounding tiles using EMIB and AIB interconnect technologies. Each of the five tiles – labeled "PCIe 5.0," "CXL," "116 G XCVR," "HBM," and "Other Chiplet" shown at the periphery of the central FPGA fabric die – is different, but the EMIB and AIB interconnect technologies used to connect these tiles to the FPGA fabric die remain constant. If required by the application, any tile shown in Figure 1 can be changed out for another function using Intel's advanced packaging technology. Even the central FPGA fabric die shown in Figure 1 can be replaced by other types of logic die including Intel® eASIC™ structured ASICs and full-custom ASICs.

The new devices in this Direct-RF Series FPGA portfolio now extend the I/O capabilities of Intel Agilex 9 and Intel Stratix 10 FPGAs to the analog domain using RF ADC and DAC chiplets that have been co-developed with industry leaders and then composed into packaged devices using Intel's EMIB and AIB interconnect technologies. These RF ADC and DAC chiplets operate as fast as 64 Gsps with 36 GHz of bandwidth. Tile-based design and the heterogeneous die-and-tile manufacturing approach to developing Direct-RF Series FPGA allow Intel to quickly address a broad array of analog signal processing applications in the RF frequency domain.

EMIB and AIB In-Depth

EMIB is a practical and reliable die-to-die interconnect technology that's relatively easy for chip designers to implement. EMIB greatly resembles high-density PCB wiring but at a much smaller scale that is aimed at the device package level, with trace-to-trace and pad spacing appropriate for chip-scale packaging.

AIB is a very wide, multi-channel, high-speed, low-power parallel bus with a simple clocked interface bus protocol designed specifically to meet the requirements for die-to-die interconnect. Intel released AIB as a royalty-free chiplet interconnect standard to DARPA's Common Heterogeneous Integration and Intellectual Property (IP) Reuse Strategies (CHIPS) program in 2018. The CHIPS Alliance subsequently published the AIB specification as a standard.

Intel developed the EMIB and AIB technologies to support many types of next-generation platforms, which must evolve quickly to keep pace with emerging system trends in a variety of application domains including data centers, the Internet of Things (IoT), 400 Gbps to terabit networking, optical transport, 8K video, 5G wireless, and military/aerospace equipment such as radar and EW systems. In the rarefied RF space, those trends include higher RF carrier frequencies, more antennas, more complex modulation schemes, and much more digital signal processing (DSP).

All these systems must meet increasingly difficult project goals including:

- Higher bandwidth
- Lower power
- Smaller footprint or form factor
- Increased functionality
- Increased flexibility

Historically, system architects have responded to these requirements by packing more discrete components onto standard printed circuit boards (PCBs), but this strategy yields diminishing returns for high-frequency RF applications because:

- Chip-to-chip bandwidth is limited by the interconnect density and trace impedances of the underlying PCB
- System interconnect power is too high due to the need to drive long PCB traces between components
- PCB form factors become too large due to the growing number of components placed on the board to meet increasing functionality requirements

For many years, system architects largely relied upon monolithic integration to address these limitations. However, monolithic integration for RF applications increasingly produces more challenges. The first such challenge is IP maturity and suitability of certain functions for a given process node. Analog converter IP is not generally well-suited to the same CMOS process nodes used to build dense digital circuitry – like the circuity found within FPGAs. Trying to implement high-speed analog data converters on a monolithic process node that is optimized for dense digital logic compromises the performance of both the converters and the logic. This problem becomes worse with each new semiconductor process node.

There's a Better Way

Manufacturing high-performance analog converters in a process technology that's well suited to the converters' requirements and then connecting the resulting tiles to a high-performance FPGA die using EMIB and AIB packaging technology makes a lot of engineering sense. Using EMIB and AIB, Intel can integrate advanced functions into its FPGAs from any IP vendor, manufactured with any semiconductor process node, from any silicon vendor. Intel's Ponte Vecchio GPU is an extreme example of Intel's multi-die integration capabilities. The Ponte Vecchio GPU combines 47 active semiconductor tiles manufactured with five different process technologies in one device package.

Intel worked directly with leading high-speed converter companies to develop high-performance RF ADC and DAC tiles compatible with EMIB packaging technology and the AIB standard to add high-speed analog converters to its tile inventory, enabling the development of the Direct-RF Series FPGA portfolio. The same EMIB and AIB packaging technologies used to create the new portfolio of Direct-RF Series FPGAs can also be used to create integrated devices that combine high-speed analog converters with Intel eASIC structured ASICs. Full-custom ASIC die can also be used for customer designs that require it. From a packaging perspective, the Intel FPGAs and SoCs in the new Direct-RF Series FPGA portfolio are not nearly as complex as the 47-tile Ponte Vecchio GPU.

The Evolution of RF Processing

Before the development of high-speed data converters and DSPs, the RF domain was almost entirely analog. A series of filters and mixers – drawn from the rich, decades-long heritage of tube-based superheterodyne radio receivers first developed by Edwin Armstrong during World War I – down-converts RF signals to baseband frequencies. These early RF receivers were typically limited to 10's or 100's of MHz. With the advent of analog converters that can operate at tens of gigasamples/sec, it's possible to design direct-RF architectures for these and even higher frequencies. The advantage of direct-RF front-end architectures is that they eliminate most of the expensive analog components, which increases performance, decreases system-level costs, and reduces SWAP. Figure 2 illustrates the evolution of RF front-end architecture from superheterodyne to direct RF.

The list of direct-RF front-end advantages made possible by the new Direct-RF Series FPGA/Intel eASIC device/ASIC portfolio includes:

- Direct-RF architectures deliver increased performance while eliminating many expensive analog components, which lowers system-level costs
- Direct-RF architectures deliver many SWAP advantages, so applications with ambitious size, weight, and power requirements benefit the most from these devices
- Platforms with long lifespans (as many as 30 to 50 years for some military applications) need solutions that fit within existing size and power infrastructure constraints during the platform's entire lifespan..
- Direct-RF solutions allow engineers to create systems that were once considered impossible to implement
- Solutions with lower power requirements can leverage Intel's full logic continuum, substituting an Intel eASIC structured ASICs or a custom ASIC for the Intel FPGA die in a packaged design
- Intel's direct-RF implementation architecture delivers the lowest latency between the analog domain and the network

When discrete analog converters capable of direct RF conversion started to become available, the parallel interfaces used by high-speed converters began to bog down and create bottlenecks as data rates soared. Converter vendors ultimately standardized on the JESD204 serial interface standard to handle these faster analog converters.

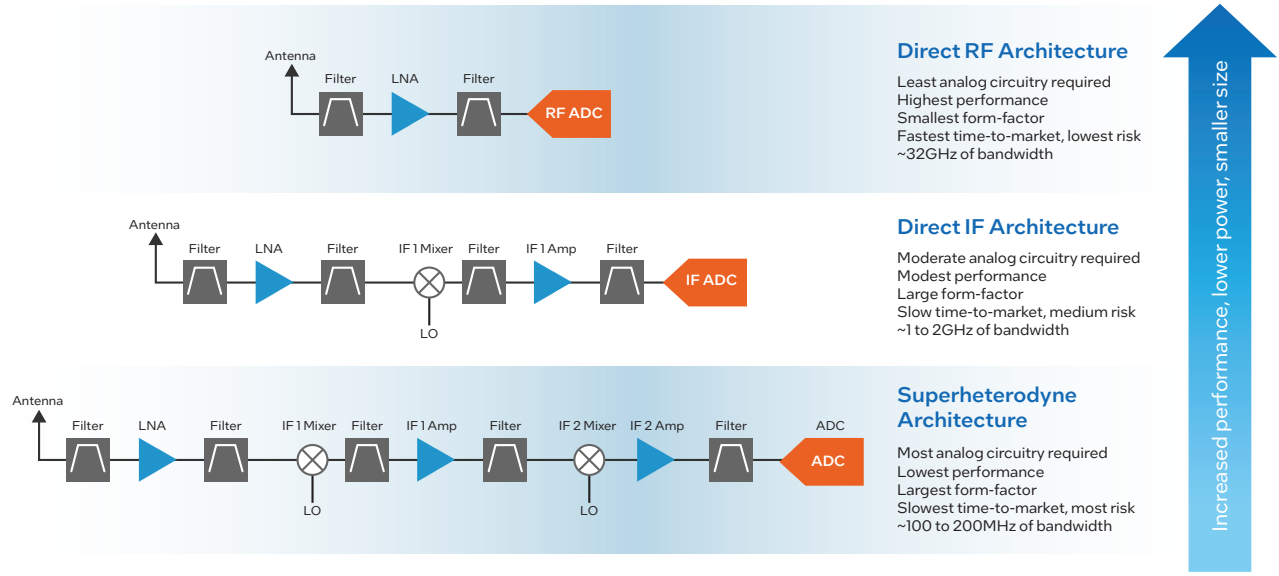

Figure 2. RF front-end design has evolved from fully analog, using a superheterodyne architecture, to the largely digital direct-RF architecture enabled by today's high-speed analog converters and fast digital logic.

The first JESD204 standard appeared in 2006 and has evolved over the years. The original single-lane JESD204 had maximum data rate of 3.125 Gbps. JESD204A, which appeared in 2008, added support for multiple lanes with a maximum data rate of 3.125 Gbps per lane. JESD204B appeared in 2011 and has a maximum transfer rate of 12.5 Gbps per lane, while JESD204C has a maximum transfer rate of 32 Gbps per lane.

The JESD204 standard delivered several advantages compared to parallel connections over PCB traces:

- Reduced PCB area
- Simplified PCB trace routing
- Reduced converter package size
- Comparable I/O power consumption for higher I/O throughput
- Scalable to higher frequencies
- Simplified interface timing

Intel FPGAs and SoC FPGAs have long supported the JESD204 protocols through their high-speed SerDes transceiver ports. However, the JESD204 standards also have disadvantages.

Two of the most significant JESD204 disadvantages are the added latency of the serial connections and the relatively high I/O power consumption needed to drive multiple PCB traces at multi-Gbps data rates. At the maximum 64 Gsps sample rate, a JESD204C connection running at 32 Gbps serial data rate per lane requires 16 lanes of high-speed interconnect between each data converter and the FPGA's transceiver ports to satisfy the required transfer rate. Such an interface consumes a significant amount of power and routing 16 lanes of 32 Gbps signals per discrete converter on a PCB so that all traces have exactly the same length can be challenging.

Further, many military applications cannot tolerate the latency overhead imposed by the JESD204 interface protocol. These kinds of real-time applications need a different sort of high-speed analog converter interface that consumes less power and exhibits much lower latency. Devices in the new Direct-RF Series FPGA portfolio require less interface power and deliver lower much latency because they're based on the massively parallel connectivity and much lower I/O power consumption inherent in Intel's EMIB and AIB die-to-die interconnect technologies.

FPGAs, structured ASICs, and ASICs

The FPGA die in these Direct-RF Series FPGAs are well suited to direct-RF applications. Their ability to implement very wide DSP blocks mates well with the wide interconnect capabilities of EMIB and AIB, enabling direct-RF processing at much lower clock rates, due to programmable logic's massively parallel processing capabilities.

However, the RF converter tiles used in these Direct-RF Series FPGAs are not limited to use with FPGA fabric die. Because they use the EMIB and AIB interconnect standards, these same RF converter tiles can be used with Intel eASIC structured ASICs, which trade off hardware field-programmability for lower power, higher operating speed, and lower unit cost. Intel eASIC devices deliver lower operating power when compared with FPGAs and lower total cost of ownership by delivering faster time to market (TTM) and lower NRE when compared to ASICs. Designs based on Intel eASIC structured ASICs can be completed in roughly half the development time required for a cell-based ASIC, when using a comparable process technology. In addition, it's possible to convert some FPGA-based designs into Intel eASIC structured ASIC designs directly using tools and services provided by Intel.

For the right project, it may make sense to take a project's logic die all the way to the ASIC level. ASICs are fully custom semiconductors that are tailor-made for specific applications. ASICs can deliver the same functions as Intel FPGAs and Intel eASIC structured ASICs, but with even lower power consumption and higher performance. Additional NRE costs and development time are required to instantiate a design into an ASIC. Intel and Intel Foundry Services (IFS) work directly with customers desiring an ASIC solution.

The Art of the Possible

Solving tough engineering challenges such as implementing direct RF, is just the beginning. Intel builds most of the members of the Intel Stratix 10 and Intel Agilex 9 FPGA families, including the new Direct-RF Series FPGA portfolio by assembling various chiplet combinations into a single component using advanced packaging techniques. Pursuing this chiplet-based methodology has helped Intel build many industry-leading capabilities into Intel Agilex 9 FPGAs with higher performance, lower power consumption, PCIe 4.0 and 5.0 interfaces, Compute Express Link (CXL) interfaces, transceiver data rates as fast as 116 Gbps, and integration of high-performance HBM2e DRAM.

Intel is uniquely well positioned to address the toughest application challenges because of the company's technology lead in chiplet-based heterogenous integration. This lead has allowed Intel to quickly develop FPGAs that are more closely targeted for their intended applications.

Figure 3 shows Intel's chiplet library, which includes a wide array of functions developed on a variety of process nodes. These chiplets provide the building blocks for assembling complex, highly capable, finely targeted FPGAs. The left side of Figure 3 shows Intel chiplet within the library including various FPGA fabrics, interconnect chiplets including high-speed SerDes transceivers, PCIe 4.0 and 5.0 ports, and more specialized chiplets that implement specific capabilities such as DSP and networking.

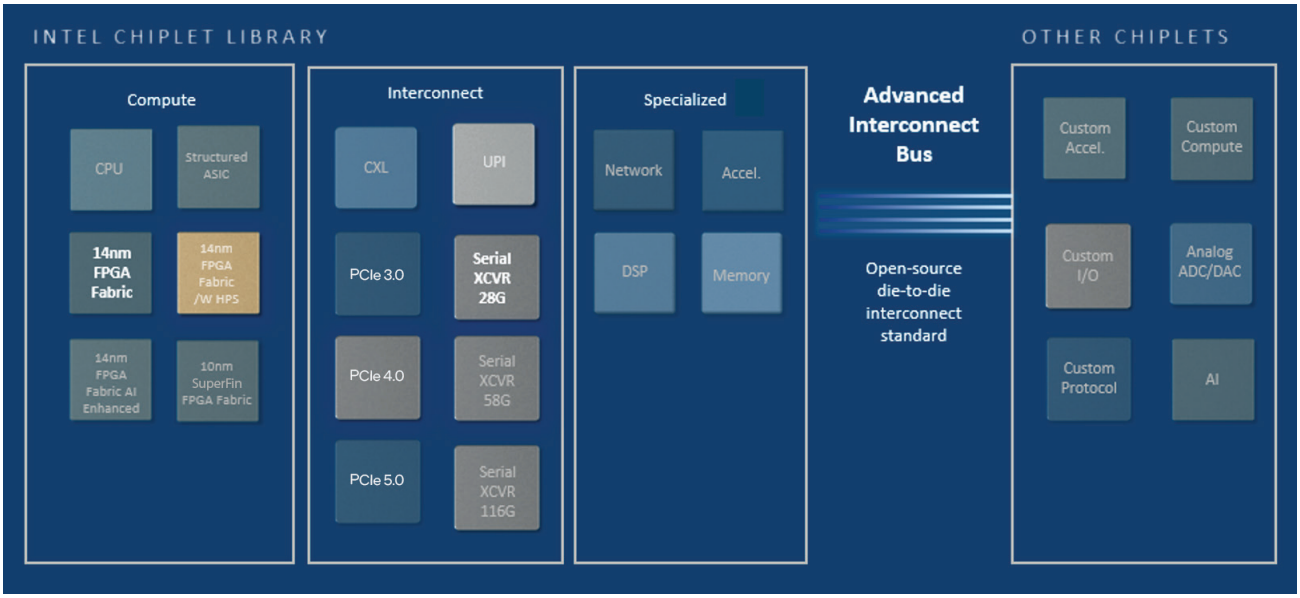

Figure 3. The Intel chiplet library enables heterogeneous assembly of targeted FPGAs

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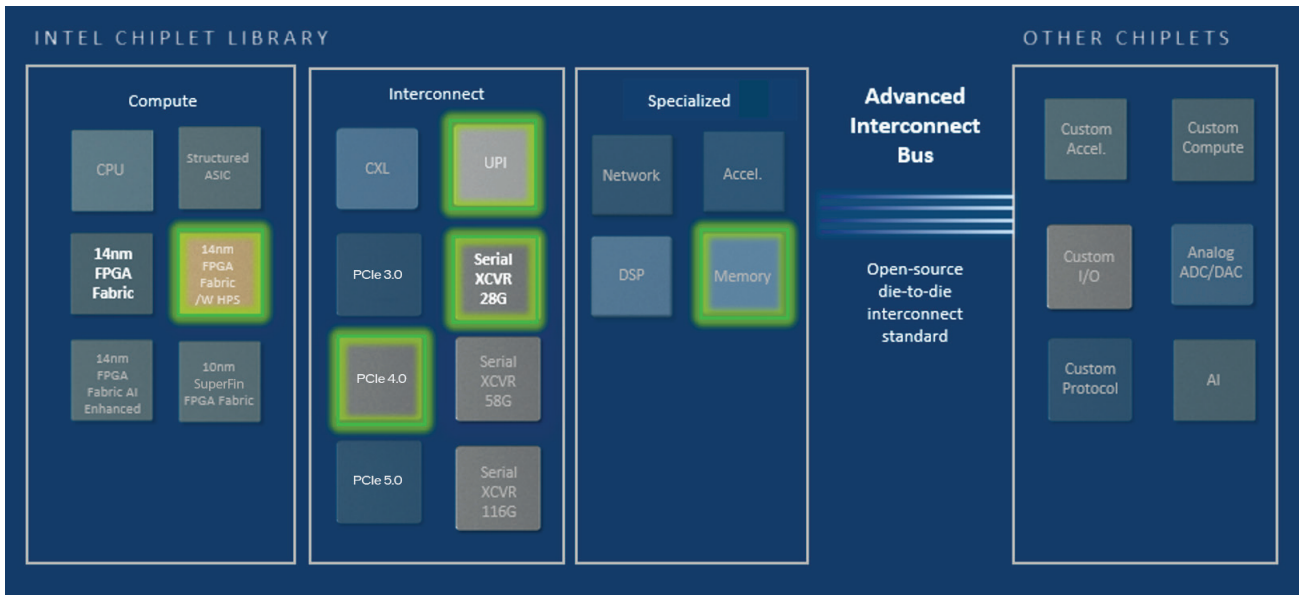
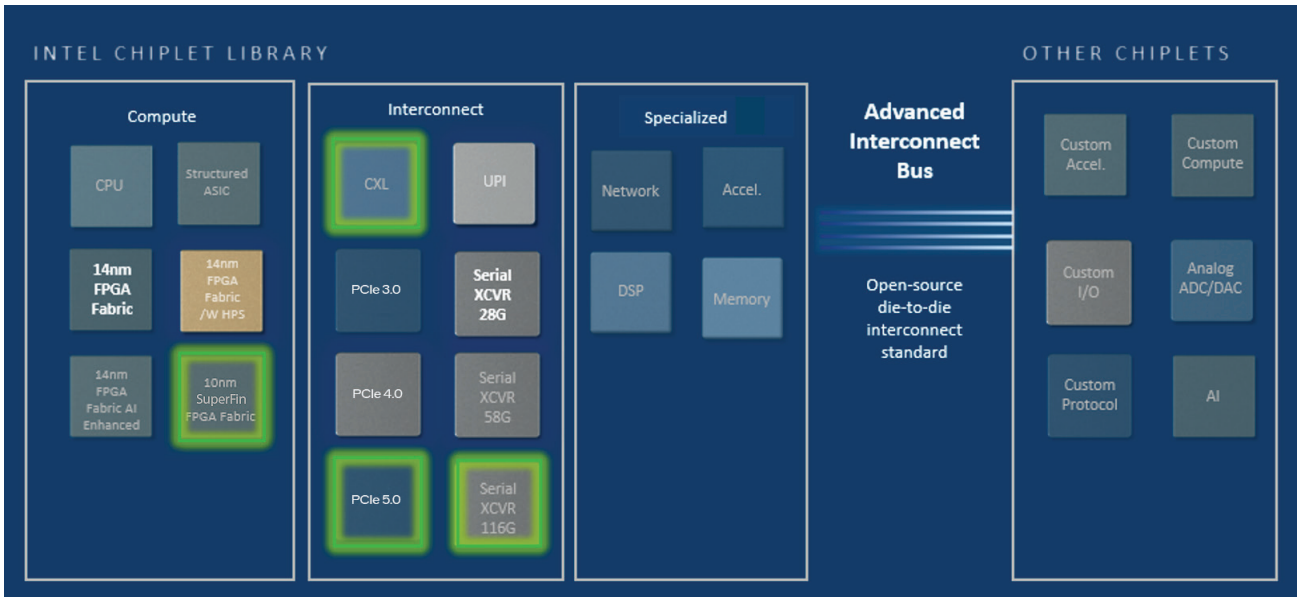
The right side of Figure 3 shows a set of application-specific chiplets used for custom acceleration, custom I/O, custom compute functions, and analog functions such as ADCs and DACs. These custom chiplets can be sourced by any IP or semiconductor vendor, developed on any process node, using any foundry. As long as these chiplets use the AIB protocol, Intel can integrate them into its FPGAs and SoCs using EMIB packaging technology.

For example, Figure 4(a) shows the chiplets that Intel used to add PCIe 4.0 capability to the Intel Stratix 10 DX FPGA family. Thanks to chiplets, EMIB technology, and AIB, Intel became the first vendor to offer FPGAs with PCIe 4.0 capability that was certified by the PCI Special Interest Group. This Intel Stratix 10 FPGA family member incorporates a chiplet that provides the PCIe 4.0 capability, a HBM memory stack (a vertical stack of chiplets) to provide high memory bandwidth, and 58G transceiver chiplets for high-performance serial I/O. Similarly, Figure 4(b) shows the construction of an Intel Agilex 9 FPGA that incorporates a different combination of chiplets paired with an Intel Agilex 9 FPGA logic die, resulting in an advanced FPGA with PCIe 5.0, CXL, and 116G serial transceivers. Finally, Figure 4(c) shows how an analog-enabled Intel FPGA might be constructed from chiplets made by Intel and from chiplets sourced from other semiconductor vendors.

4(a)



4(b)



4(c)

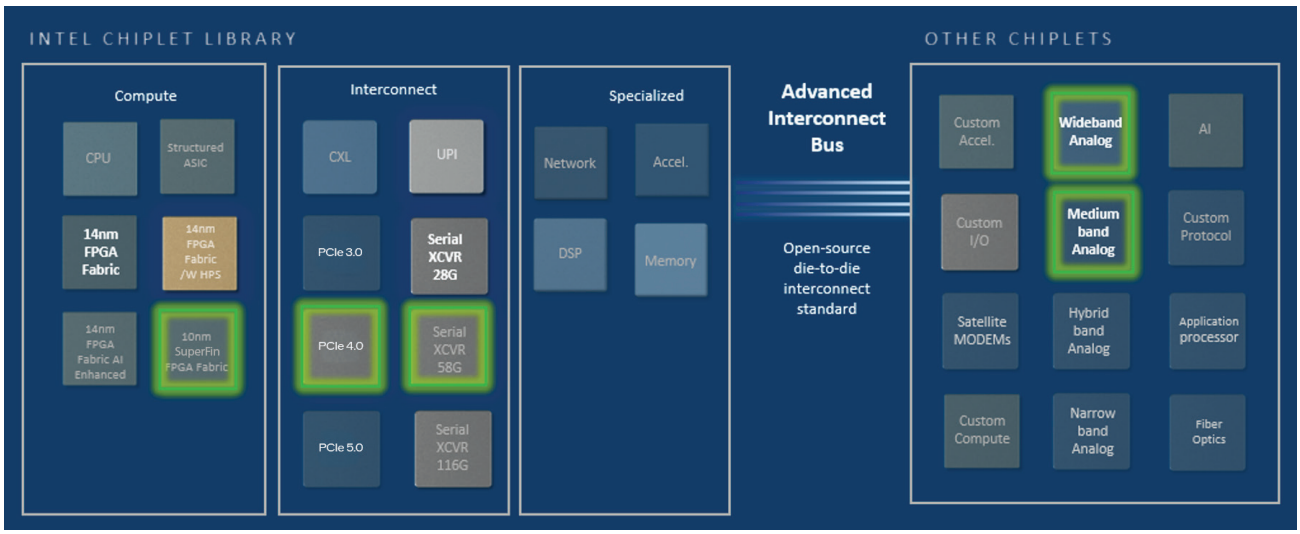


Figure 4. The Intel Stratix 10 DX FPGA family became the first FPGAs to offer PCIe 4.0 capabilities certified by the PCI Special Interest Group, thanks to the use of chiplets, as shown in 4(a). Intel added PCIe 5.0, CXL, and 116G transceivers to Intel Agilex 9 FPGAs using chiplets from the chiplet library, as shown in 4(b). Finally, an analog-enabled Intel FPGA might use analog chiplets from other semiconductor vendors, as shown in Figure 4(c).

Figures 4(a), 4(b), and 4(c) illustrate how chiplet-based design and manufacturing allow Intel to introduce new technology rapidly, by building on a firm foundation of existing chiplets, and then mixing and matching those chiplets using any combination of IP, process node, and foundry to achieve the required functionality.

Currently, there are more than twenty chiplets in the Intel chiplet library. These chiplets encompass a broad range of functionality, built on several different process nodes from multiple foundries, and sourced from different developers. Functions in the library already include FPGA fabric die from two Intel FPGA families, high-speed SerDes transceivers, optical I/O, analog data converters, application-specific computing, and five chiplets from Defense Industrial Base suppliers.

Over time, this chiplet library will continue to grow. Intel can integrate these chiplets with FPGA, structured ASIC, or full-custom ASIC die. This capability provides system designers with a range of design options that cover different levels of flexibility and different levels of optimization for cost, power, and performance for many applications including direct RF, and beyond.

Conclusion

As the only semiconductor vendor to offer FPGAs, structured ASICs, and ASICs, Intel is uniquely positioned to provide a range of solutions for teams developing high-performance RF-band equipment. Years of experience with advanced packaging technologies, including EMIB and AIB, and a resilient supply chain bolster Intel's trusted leadership position.

Further, Intel is continuing to work with leading makers of cutting-edge analog RF converters to develop ADC and DAC tiles that are compatible with Intel's EMIB, AIB, and multichip packaging technologies. The new analog-enabled Direct-RF Series FPGA portfolio provides concrete evidence that these technologies are ready and able to tackle the toughest problems on the analog/digital edge.

Chiplets can be based on many types of technologies, from high-speed analog conversion to in-line accelerators, to whatever you can imagine. In addition, a resilient supply chain with advanced technologies and manufacturing capabilities allows Intel to deliver solutions that provide unique value. If you have an engineering challenge with unique performance and SWAP requirements that might benefit from this sort of advanced technology, let's talk.

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