CAUTION: The IP described in this document is scheduled for product obsolescence and discontinued support as described in PDN1403. Therefore, Altera does not recommend use of this IP in new designs. For more information about Altera's current IP offering, refer to Altera's Intellectual Property website.
# Altera Corporation MegaCore Version 9.1

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1. About This MegaCore Function

Release Information

Table 1–1 provides information about this release of the Altera® RLDRAM II Controller MegaCore® function.

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Version</td>
<td>9.1</td>
</tr>
<tr>
<td>Release Date</td>
<td>November 2009</td>
</tr>
<tr>
<td>Ordering Code</td>
<td>IP-RLDRAMII</td>
</tr>
<tr>
<td>Product ID</td>
<td>00AC</td>
</tr>
<tr>
<td>Vendor ID</td>
<td>6AF7</td>
</tr>
</tbody>
</table>

For more information about this release, refer to the MegaCore IP Library Release Notes and Errata.

Altera verifies that the current version of the Quartus® II software compiles the previous version of each MegaCore function. The MegaCore IP Library Release Notes and Errata report any exceptions to this verification. Altera does not verify compilation with MegaCore function versions older than one release.

Device Family Support

MegaCore functions provide either full or preliminary support for target Altera device families:

- **Full support** means the MegaCore function meets all functional and timing requirements for the device family and may be used in production designs.
- **Preliminary support** means the MegaCore function meets all functional requirements, but may still be undergoing timing analysis for the device family; it may be used in production designs with caution.
Table 1–2 shows the level of support offered by the RLDRAM II Controller MegaCore function to each Altera device family.

<table>
<thead>
<tr>
<th>Device Family</th>
<th>Support</th>
</tr>
</thead>
<tbody>
<tr>
<td>HardCopy® II</td>
<td>Preliminary</td>
</tr>
<tr>
<td>Stratix® II</td>
<td>Full</td>
</tr>
<tr>
<td>Stratix II GX</td>
<td>Full</td>
</tr>
<tr>
<td>Other device families</td>
<td>No support</td>
</tr>
</tbody>
</table>

**Features**

- Common I/O (CIO) and separate I/O (SIO) device support
- Memory burst length 2, 4, and 8-beat support
- Nonmultiplexed addressing
- Datapath generation
- Data strobe signal (DQS) and non-DQS capture modes
- Automatic constraint generation
- Easy-to-use IP Toolbench interface
- IP functional simulation models for use in Altera-supported VHDL and Verilog HDL simulators
- Support for OpenCore Plus evaluation

**General Description**

The RLDRAM II controller MegaCore function handles the complex aspects of using RLDRAM II—initializing the memory devices and translating read and write requests from the local interface into all the necessary RLDRAM II command signals.

The RLDRAM II controller is optimized for Altera Stratix II devices and has preliminary support for Stratix II GX and HardCopy II devices. The advanced features available in these devices allow you to interface directly to RLDRAM II devices.

Figure 1–1 on page 1–3 shows a system-level diagram including the example design that the RLDRAM II Controller MegaCore function creates for you.
About This MegaCore Function

Figure 1–1. RLDAM II Controller System-Level Diagram

IP Toolbench generates the following items:

- A testbench, which instantiates the example design
- A synthesizable example design which instantiates the following modules:
  - RLDAM II controller:
    - Encrypted control logic, which takes transaction requests from the local interface and issues writes, reads, and refreshes to the memory interface
    - A clear-text datapath
  - Example driver—generates write, read and refresh requests and outputs a pass_fail signal to indicate that the tests are passing or failing
  - System phase-locked loop (PLL)—generates the RLDAM II controller clocks
  - Delay locked loop (DLL)—instantiated in DQS mode and generates the DQS delay control signal for the dedicated DQS delay circuitry

Note to Figure 1–1:
(1) Non-DQS mode only.
Performance and Resource Utilization

- Optional feedback clock PLL—instantiated in non-DQS mode and generates a capture clock for the datapath read capture and logic path

OpenCore Plus Evaluation

With Altera’s free OpenCore Plus evaluation feature, you can perform the following actions:

- Simulate the behavior of a megafunction (Altera MegaCore function or AMPPSM megafunction) within your system
- Verify the functionality of your design, as well as evaluate its size and speed quickly and easily
- Generate time-limited device programming files for designs that include MegaCore functions
- Program a device and verify your design in hardware

You only need to obtain a license for the megafunction when you are completely satisfied with its functionality and performance, and want to take your design to production.

For more information on OpenCore Plus hardware evaluation using the RLDRAM II controller, refer to “OpenCore Plus Time-Out Behavior” on page 2–12 and AN 320: OpenCore Plus Evaluation of Megafonctions.

Table 1–3 shows typical expected performance for the RLDRAM II Controller MegaCore function, with the Quartus II software.

<table>
<thead>
<tr>
<th>Device</th>
<th>Capture Mode</th>
<th>f_{MAX} (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stratix II (EP2S60F1020C3)</td>
<td>Non-DQS</td>
<td>200</td>
</tr>
<tr>
<td></td>
<td>DQS</td>
<td>300</td>
</tr>
<tr>
<td>Stratix II GX (EP2SGX30CF780C3)</td>
<td>Non-DQS</td>
<td>200</td>
</tr>
<tr>
<td></td>
<td>DQS</td>
<td>300</td>
</tr>
</tbody>
</table>
Stratix II and Stratix II GX devices support RLDRAM at up to 300 MHz. Table 1–4 shows the clock frequency support for Stratix II and Stratix GX device families, with the Quartus II software.

<table>
<thead>
<tr>
<th>Speed Grade</th>
<th>Frequency (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>−3</td>
<td>300</td>
</tr>
<tr>
<td>−4</td>
<td>250</td>
</tr>
<tr>
<td>−5</td>
<td>200</td>
</tr>
</tbody>
</table>

Table 1–5 shows typical sizes in combinational adaptive look-up tables (ALUTs) and logic registers for the RLDRAM II controller.

<table>
<thead>
<tr>
<th>Device</th>
<th>Memory Width (Bits)</th>
<th>Combinational ALUTs</th>
<th>Logic Registers</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stratix II and Stratix II GX</td>
<td>9</td>
<td>127</td>
<td>169</td>
</tr>
<tr>
<td></td>
<td>18</td>
<td>130</td>
<td>209</td>
</tr>
<tr>
<td></td>
<td>36</td>
<td>151</td>
<td>287</td>
</tr>
<tr>
<td></td>
<td>72</td>
<td>185</td>
<td>444</td>
</tr>
</tbody>
</table>

Notes to Table 1–5:
(1) These sizes are a guide only and vary with different choices of parameters.
2. Functional Description

Figure 2–1 shows the RLDRAM II Controller MegaCore function block diagram.

**Notes to Figure 2–1:**
(1) You can edit the rldramii_prefix in IP Toolbench.
(2) The default signal is <signal>_0. When you specify additional address and command busses, both <signal>_0 and <signal>_1 are present.
(3) Non-DQS mode only.
(4) DQS mode only.
The RLDRAM II controller comprises the following two blocks:

- Control logic (encrypted)
- Datapath (clear text)

The control logic performs the following actions:

- Generates initialization sequence using the RLDRAM II initialization values set in IP Toolbench
- Generates write, read, or refresh accesses when requested at the local interface
- Generates datapath control signals that ensure that the write data is output on the memory rldramii_dq[] (CIO devices) or rldramii_d[] (SIO devices) bus during the correct clock cycles

The datapath performs the following actions:

- Interfaces to common I/O (CIO) or separate I/O (SIO) RLDRAM II devices
- Generates RLDRAM II clocks
- Places RLDRAM II commands onto the memory command bus using one of the following system PLL clocks on either the rising or falling edge:
  - System clock
  - Write clock
  - Dedicated clock
- Places write data onto the rldramii_dq[] or rldramii_d[] bus during the correct clock cycles
- Captures the read data using dedicated data strobe signal (DQS) delay circuitry during DQS mode or an external capture clock in non-DQS mode

Control Logic

The control logic is responsible for controlling transactions at the memory interface. The control logic accepts read, write, and refresh requests and executes them immediately as RLDRAM II transactions.

In addition to reads, writes, and refreshes the control logic is also responsible for controlling initialization of the RLDRAM II devices.

For more information on reads, writes, refreshes, and initialization, see “Interfaces” on page 2–16.
Table 2–1 shows the RLDRAM II control signals generated by the control logic for each operation.

<table>
<thead>
<tr>
<th>Operation</th>
<th>Acronym</th>
<th>rldramii_cs_n_0</th>
<th>rldramii_we_n_0</th>
<th>rldramii_ref_n_0</th>
<th>rldramii_a_0[20:0]</th>
<th>rldramii_ba_0[2:0]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Idle</td>
<td>NOP</td>
<td>High</td>
<td>Don't care</td>
<td>Don't care</td>
<td>Don't care</td>
<td>Don't care</td>
</tr>
<tr>
<td>Mode Register Set</td>
<td>MRS</td>
<td>Low</td>
<td>Low</td>
<td>Low</td>
<td>See your RLDRAM data sheet</td>
<td>Don't care</td>
</tr>
<tr>
<td>Read</td>
<td>READ</td>
<td>Low</td>
<td>High</td>
<td>High</td>
<td>Address</td>
<td>Bank address</td>
</tr>
<tr>
<td>Write</td>
<td>WRITE</td>
<td>Low</td>
<td>Low</td>
<td>High</td>
<td>Address</td>
<td>Bank address</td>
</tr>
<tr>
<td>Auto Refresh</td>
<td>AREF</td>
<td>Low</td>
<td>High</td>
<td>Low</td>
<td>Don't care</td>
<td>Bank address</td>
</tr>
</tbody>
</table>

**Datapath**

Figure 2–2 on page 2–4 shows the datapath block diagram.
Block Description

Figure 2–2. Datapath Block Diagram

Note (1)

The default signal is \(<signal>_0. When you specify additional address and command busses, both \(<signal>_0\) and \(<signal>_1\) are present.

The datapath performs the following functions:

- Interfaces to CIO or SIO RLDRAM II devices
- Outputs write data to the RLDRAM II interface
- Captures RLDRAM II read data and data valid (QVLD) signals with:
  - In DQS mode, a delayed \(rldramii_qk[]\) generated by the dedicated DQS delay circuitry
  - In non-DQS mode, an external capture clock

Note to Figure 2–2:
(1) The default signal is \(<signal>_0. When you specify additional address and command busses, both \(<signal>_0\) and \(<signal>_1\) are present.
Functional Description

- Generates the RLDRAM II clocks
- Generates addresses and commands on:
  - System, dedicated, or write clock
  - Rising or falling edge
- Inserts pipeline registers in address and command and write data path
- Inserts pipeline registers in read data and QVLD path

The datapath provides the interface between the read and write data busses of the datapath interface and the double-clocked, bidirectional data bus of the memory interface. The datapath data busses are twice the width of the memory data bus, because the memory interface transfers data on both the rising and falling edges of the clock.

IP Toolbench generates a clear-text VHDL or Verilog HDL datapath, which matches your custom variation. If you are designing your own controller, Altera recommends that you use this module as your datapath.

Figure 2–3 shows the write control signals timing relationship when writing to the datapath.

---

**Figure 2–3. Datapath Write Control Signal Timing**

---

Memory Clock Generator

The memory clock generator generates memory clocks. There can be up to four memory clocks and they are generated with an `altddio_out` megafunction.

Address & Command Output Registers

The address and command output registers can have the following options:

- System, write, or dedicated clock clocking for the output registers.
- Rising or falling edge clocking
Pipeline Registers

IP Toolbench can insert pipeline registers into the datapath to help meet timing at higher frequencies. IP Toolbench offers the following pipeline options:

- Insert address and command and write data pipeline registers. The pipeline depth is the same for the write-data path and the address and command path. The write data and address and command pipeline registers are clocked off the system clock.
- Insert read data and QVLD pipeline registers. The pipeline depth is the same for the read-data path and the QVLD path. The read data and QVLD pipeline registers are clocked off the clock that captures the read data—the delayed rldramii_qk[] signal in DQS mode; the external capture clock in non-DQS mode.

DQS Group

The datapath instantiates one or more DQS groups, which generates write data, rldramii_dq[] (CIO devices), or rldramii_d[] (SIO devices) and captures read data rldramii_dq[] (CIO devices), or rldramii_q[] (SIO devices). The IP Toolbench DQ per DQS (CIO devices) or Q per DQS (SIO devices) parameter determines the DQS group width. For example, if DQ per DQS is 9 bits, the control_wdata[] and control_rdata[] signals are 18-bits wide. To build larger widths, the datapath instantiates multiple DQS group modules to increase the data-bus width in increments of DQ per DQS (or Q per DQS) bits.

The datapath generates the DM output, rldramii_dm[], in the DM group module. It generates the DM output in the same way as the write data.

The datapath captures the QVLD input, rldramii_qvld[], in the QVLD group module. The rldramii_qvld[] signal is captured in the same way that the DQS group module captures the read data. In DQS mode, the delayed rldramii_qk[] captures rldramii_qvld[]; in non-DQS mode, the external clock captures rldramii_qvld[].

Figure 2–4 on page 2–7 shows the Stratix II series and HardCopy II devices DQS group block diagram (DQS mode, CIO devices).
**Figure 2–4. DQS Group Block Diagram—DQS Mode, CIO Devices**  
*Note (1), (2), (3)*

**Notes to Figure 2–4:**
1. This figure shows the logic for one DQ output only.
2. All clocks are $clk$, unless marked otherwise.
3. Bus width $W$ is dependent on the DQ per DQS parameter.
4. Invert combout of the I/O element (IOE) for the $dqs$ pin before feeding into $inclock$ of the IOE for the DQ pin. This inversion is automatic if you use an altdq megafuction for the DQ pins.

---

Figure 2–5 on page 2–8 shows the Stratix II series and HardCopy II devices DQS group block diagram (DQS mode, SIO devices).
Notes to Figure 2–4:
(1) This figure shows the logic for one Q output and one D input only.
(2) All clocks are clk, unless marked otherwise.
(3) Bus width W is dependent on the Q per DQS parameter.
(4) Invert combout of the I/O element (IOE) for the dqs pin before feeding in to inclock of the IOE for the Q pin. 
This inversion is automatic if you use an altdq megafunction for the Q pins.

Datapath Example

Figure 2–6 shows an example datapath. The example RLDRAM II controller and memory configuration has the following parameters:

- DQS mode
- Two 18-bit CIO RLDRAM II devices. Each RLDRAM II device has two rldramii_qk[] data strobes, each associated with 9-bits of data
- 36-bit RLDRAM II interface, which requires a 72-bit datapath interface
Figure 2–6 shows the following points, which are applicable for all interface configurations:

- Each DQS `rldramii_dq[i]` byte group is captured by the delayed version of its associated `rldramii_qk[i]` data strobe:
**Block Description**

- `rldramii_dq[8:0]` is captured by the delayed `rldramii_qk[0]`
- `rldramii_dq[17:9]` is captured by the delayed `rldramii_qk[1]`
- `rldramii_dq[26:18]` is captured by the delayed `rldramii_qk[2]`
- `rldramii_dq[35:27]` is captured by the delayed `rldramii_qk[3]`

- QVLD is always captured by the delayed version of `rldramii_qk[0]` for the associated RLDRAM II device. In Figure 2–6 there are four `rldramii_qk[]` signals. Only `rldramii_qk[0]` per RLDRAM II device captures the associated QVLD signal:
  - `rldramii_qvld[0]` is captured by the delayed `rldramii_qk[0]`
  - `rldramii_qvld[1]` is captured by the delayed `rldramii_qk[2]`

- After the capture registers all captured read data is clocked off the undelayed `rldramii_qk[]` signal that captures the QVLD signal for a particular RLDRAM II device:
  - All RLDRAM II 0 captured data is clocked off the undelayed `rldramii_qk[0]`
  - All RLDRAM II 1 captured data is clocked off the undelayed `rldramii_qk[2]`

- Only one `capture_clk[]` per attached RLDRAM II device is output from the datapath:
  - RLDRAM II 0 capture data is associated with `capture_clk[0]`, which is the delayed `rldramii_qk[0]`
  - RLDRAM II 1 capture data is associated with `capture_clk[1]`, which is the delayed `rldramii_qk[2]`

**Read Data Capture Clock Association**

Figure 2–7 shows the read data and data strobes at the memory interface for the example datapath in Figure 2–6. Figure 2–8 shows how the `capture_clk[]` associates with the captured read data, `control_rdata[]` at the datapath interface.
Figure 2–7. Memory Interface

```
RLDRAM II
Device 1
rldramii_dq[35:27]
  M  N  O  P
rldramii_qk[3]
  I  J  K  L
rldramii_dq[26:18]
  rldramii_qk[2]
  rldramii_dq[35:27]
  RLDRAM II
  Device 0
  rldramii_dq[17:9]
  E  F  G  H
  rldramii_qk[1]
  rldramii_dq[8:0]
  A  B  C  D
  rldramii_qk[0]
  rldramii_qk[]{3}
  rldramii_qk[]{2}
  rldramii_qk[]{1}
  rldramii_qk[]{0}
```

- Data associated with rldramii_qk[]{3} rising edge
- Data associated with rldramii_qk[]{0} falling edge

Figure 2–8 shows that any read data captured on the rising edge of the delayed rldramii_qk[]{] signal is located in the lower half-bit locations of control_rdata[]. Any read data captured on the falling edge of the delayed rldramii_qk[]{] signal is located in the upper half-bit locations.
of control_rdata[], which means different bit ranges of the control_rdata[] are associated with different capture_clk[] signals.

Figure 2–8 is a specific example but the mapping and clock association applies to any RLDRAM II controller interface and memory configuration.

OpenCore Plus Time-Out Behavior

OpenCore Plus hardware evaluation can support the following two modes of operation:

- Untethered—the design runs for a limited time
- Tethered—requires a connection between your board and the host computer. If tethered mode is supported by all megafunctions in a design, the device can operate for a longer time or indefinitely

All megafunctions in a device time out simultaneously when the most restrictive evaluation time is reached. If there is more than one megafunction in a design, a specific megafunction’s time-out behavior may be masked by the time-out behavior of the other megafunctions.

For MegaCore functions, the untethered time out is 1 hour; the tethered time out value is indefinite.

Your design stops working after the hardware evaluation time expires and the controller issues no read commands at the memory interface.

For more information on OpenCore Plus hardware evaluation, see “OpenCore Plus Evaluation” on page 1–4 and AN 320: OpenCore Plus Evaluation of Megafunctions.

Device-Level Configuration

This section describes the following topics:

- “PLL Configuration” on page 2–12
- “Example Design” on page 2–14
- “Constraints” on page 2–16

PLL Configuration

IP Toolbench creates up to two example PLLs in your project directory, which you can parameterize to meet your exact requirements. IP Toolbench generates the example PLLs with an input to output clock ratio of 1:1 and a clock frequency you entered in IP Toolbench. In addition IP Toolbench sets the correct phase outputs on the PLLs’ clocks. You can
edit the PLLs to meet your requirements with the altpll MegaWizard™ Plug-In. IP Toolbench overwrites your PLLs in your project directory unless you turn off Update example design system PLL.

The external clocks are generated using standard I/O pins in double data rate I/O (DDIO) mode (using the altddio_out megafunction). This generation matches the way in which the write data is generated and allows better control of the skew between the clock and the data to meet the timing requirements of the RLDRAM II device.

The PLL has the following outputs:

- Output c0 drives the system clock that clocks most of the controller including the control logic and datapath.
- Output c1 drives the write clock that lags the system clock.
- Output c2 optionally drives the address and command clock.
- Output c3 drives the DQS DLL clock.

The recommended configuration for implementing the RLDRAM II controller in Stratix II series and HardCopy II devices is to use a single enhanced PLL to produce all the required clock signals. No external clock buffer is required as the Altera device can generate clock signals for the RLDRAM II devices.

Figure 2–9 on page 2–14 shows the recommended PLL configuration.
Notes to Figure 2–9:
(1) Non-DQS mode only.
(2) You can connect the addr_cmd_clk RLDRAM II controller input to clk, write_clk or to the dedicated PLL output C2.

Example Design

IP Toolbench creates an example design that shows you how to instantiate and connect up the RLDRAM II controller to an example driver. The example design is a working system that can be compiled and used for both static timing checks and board tests. It also instantiates an example PLL that generates all the required clocks for the controller. In DQS mode, a DLL is instantiated that controls the DQS capture delay phase. In non-DQS mode, the example design instantiates a feedback PLL. The output of the feedback PLL is a phase-shifted rldramii_qk[] data strobe, which captures the read data.

The example driver is a self-checking test generator for the RLDRAM II controller. It uses a state machine to write data patterns to all memory banks. It then reads back the data and checks that the data matches. If any read data fails the comparison, the pnf_per_byte output transitions low for one cycle and the pnfPersist permanent output transitions low and stays low.

Figure 2–10 shows a testbench and an example design.
Table 2–2 describes the files that are associated with the example design and the testbench.

### Table 2–2. Example Design & Testbench Files

<table>
<thead>
<tr>
<th>Filename</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>&lt;top-level name&gt;_tb.v or .vhd (1)</code></td>
<td>Testbench for the example design.</td>
</tr>
<tr>
<td><code>&lt;top-level name&gt;.vhd or .v (1)</code></td>
<td>Example design.</td>
</tr>
<tr>
<td><code>rldramii_pll_&lt;device name&gt;.vhd or .v</code></td>
<td>Example PLL, which you should configure to match your frequency.</td>
</tr>
<tr>
<td><code>rldramii_fbpll_&lt;device name&gt;.vhd or .v</code></td>
<td>Feedback PLL.</td>
</tr>
<tr>
<td><code>&lt;variation name&gt;_example_driver.v or .vhd (2)</code></td>
<td>Example driver.</td>
</tr>
<tr>
<td><code>&lt;variation name&gt;.v or .vhd (2)</code></td>
<td>RLDRAM II controller.</td>
</tr>
</tbody>
</table>

**Notes to Table 2–2:**

(1) `<top-level name>` is the name of the Quartus II project top-level entity.

(2) `<variation name>` is the variation name.

The testbench instantiates an RLDRAM II model and generates a reference clock for the PLL.

Altara does not provide a memory simulation model. You must download one or use your own.
For more details on how to run the simulation script, see “Simulate the Example Design” on page 3–11.

Constraints

The constraints scripts set the following constraints:

- Sets IO standards:
  - 1.5 or 1.8-V HSTL voltage selection
  - Address and command—HSTL Class I
  - Data CIO mode—HSTL Class II
  - Data SIO mode—HSTL Class I

- Sets output capacitance

- Places data pins as per selection in pin placement constraints floor plan. Allows automatic placement for DQS and non-DQS modes

- Places all DM pins

- Sets up correct output enable groups

- Sets `rldramii_a_0`, `rldramii_ba_0`, `rldramii_cs_n_0`, `rldramii_ref_n_0` and `rldrainii_we_n_0` as fast output registers (see note 1 in Table 2–5)

- Sets `rldramii_ck[]` non-global signal in DQS capture mode

- Add **Hold Relationship** and **Setup Relationship** to all I/O ports.

Interfaces

This section describes the following RLDRAM II commands:

- Initialization
- Writes
- Reads
- Refreshes

Initialization

The control logic initializes the RLDRAM II devices. During initialization the mode register is set and each bank is refreshed in turn. IP Toolbench sets the following RLDRAM II initialization features:

- On-die termination (ODT)
- Impedance matching resistor
- DLL enable
- RLDRAM II configuration

Figure 2–11 shows the initialization sequence.
The mode register set (MRS) command configures the RLDRAM II devices. In the ten-cycle MRS sequence, the first nine MRS commands are dummy commands and all address bits are held at zero, to reset the RLDRAM II DLL; the final MRS command configures the memory. The RLDRAM II configuration data (CFG) is output on the `rldramii_a_0[ ]` bus during the final MRS command. The following memory parameters are setup during the final MRS command cycle:

- RLDRAM II termination
- Impedance matching resistor
- DLL enable/disable
- RLDRAM II configuration

**Writes**

When you assert `local_write_req`, the control logic issues the write transaction immediately at the memory interface. The control logic then requests write data by asserting `local_wdata_req`, so that the RLDRAM II `tWL` period is satisfied during write transactions. This functionality means that the write request is decoupled from the write data.

**Figure 2–12** shows three write requests at the local and SIO RLDRAM II interface. In this example, the memory burst length is set to eight beats. The RLDRAM II device is setup with a `tRC` of six-clock cycles (configuration two).
Figure 2–12 shows the transactions at the local interface are separated by the correct number of clock cycles for the target RLDRAM II device configuration. If transaction requests are supplied to the RLDRAM II controller with the incorrect spacing the controller executes these transactions as requested, which can result in incorrect behavior.

Figure 2–13 shows an example of a write following a read at a CIO RLDRAM II interface. In this example, the memory burst length is set to two beats. The RLDRAM II device is setup with a $t_{RC}$ of six-clock cycles (configuration two).

For more information about bus turnaround timing calculations with CIO devices, refer to AN 325: Interfacing RLDRAM II with Stratix II, Stratix & Stratix GX Devices.
Reads

When you assert local_read_req, the control logic issues the read transaction immediately at the memory interface.

In DQS mode the read data, rldramii_dq[] (CIO devices) or rldramii_q[] (SIO devices), and the QVLD signals, rldramii_qvld[], are captured using the delayed rldramii_qk[] data strobes that have been phase shifted using the dedicated DQS delay circuitry.

In non-DQS mode the read data, rldramii_dq[] or rldramii_q[], and the QVLD signals, rldramii_qvld[], are captured using an external capture clock.
During reads, the local interface indicates that read data is valid by asserting the `local_rdata_valid[]` signal. All captured read data is clocked off the clock that captures the RLDRAM II read data. In DQS mode, this clock is the delayed DQS signal, `capture_clk[]`, sourced from the dedicated DQS delay circuitry. In non-DQS mode this clock is the external capture clock, `non_dqs_capture_clk`.

Figure 2–14 shows an example of a read at an SIO RLDRAM II interface. In this example, the memory burst length is set to eight beats. The RLDRAM II device is setup with a $t_{RC}$ of six-clock cycles (configuration two).

Figure 2–15 shows an example of a read following a write at a CIO RLDRAM II interface. In this example, the memory burst length is set to eight beats. The RLDRAM II device is setup with a $t_{RC}$ of six-clock cycles (configuration two).

For more information about bus turnaround timing calculations with CIO devices, refer to AN 325: Interfacing RLDRAM II with Stratix II, Stratix & Stratix GX Devices.
You must issue refreshes to the RLDRAM II devices at periodic intervals. When a refresh is required, assert `local_refresh_req` and the RLDRAM II controller issues the refresh command immediately to the requested bank address on `local_bank_addr[]` input. You must correctly insert the refresh request and ensure that the tRC timing parameter is not violated. You can issue single or ganged refreshes. For ganged refreshes assert `local_refresh_req` for X clock cycles, where X is the number of refreshes that you require.

Figure 2–16 shows a single refresh command:
Table 2–3 shows the system signals.

<table>
<thead>
<tr>
<th>Name</th>
<th>Width (Bits)</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>clk</td>
<td>1</td>
<td>Input</td>
<td>System clock for the control logic and datapath.</td>
</tr>
<tr>
<td>write_clk</td>
<td>1</td>
<td>Input</td>
<td>Shifted clock that center aligns write data to the memory.</td>
</tr>
</tbody>
</table>
## Functional Description

### addr_cmd_clk

- **Name:** addr_cmd_clk
- **Width (Bits):** 1
- **Direction:** Input
- **Description:** Address and command output register clock. The `addr_cmd_clk` clock frequency must be the same as the system clock, `clk`, and the write clock, `write_clk`, frequencies.

In addition, when there is a separate address and command clock phase, no timing paths related to this clock should be cut, to ensure that any paths using a separate clock for address and command are timing analysed.

### dqs_delay_ctrl[]

- **Name:** dqs_delay_ctrl[]
- **Width (Bits):** 6
- **Direction:** Input
- **Description:** Delay bus for DLL to shift DQS inputs. DQS mode only.

### non_dqs_capture_clk

- **Name:** non_dqs_capture_clk
- **Width (Bits):** 1
- **Direction:** Input
- **Description:** Optional clock that captures read data and clocks read data logic. Non-DQS mode only.

### reset_clk_n

- **Name:** reset_clk_n
- **Width (Bits):** 1
- **Direction:** Input
- **Description:** Reset input for logic on the system clock domain. The `reset_clk_n` can be asserted asynchronously but must be deasserted synchronous to the rising edge of the system clock.

### reset_addr_cmd_clk_n

- **Name:** reset_addr_cmd_clk_n
- **Width (Bits):** 1
- **Direction:** Input
- **Description:** Reset input for logic on the address and command clock domain. The `reset_addr_cmd_clk_n` can be asserted asynchronously but must be deasserted synchronous to the rising edge of the address and command clock.
### Table 2–3. System Signals  (Part 2 of 3)

<table>
<thead>
<tr>
<th>Name</th>
<th>Width (Bits)</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>addr_cmd_clk</td>
<td>1</td>
<td>Input</td>
<td>Address and command output register clock. The <code>addr_cmd_clk</code> clock frequency must be the same as the system clock, <code>clk</code>, and the write clock, <code>write_clk</code>, frequencies. In addition, when there is a separate address and command clock phase, no timing paths related to this clock should be cut, to ensure that any paths using a separate clock for address and command are timing analysed.</td>
</tr>
<tr>
<td>dqs_delay_ctrl[]</td>
<td>6</td>
<td>Input</td>
<td>Delay bus for DLL to shift DQS inputs. DQS mode only.</td>
</tr>
<tr>
<td>non_dqs_capture_clk</td>
<td>1</td>
<td>Input</td>
<td>Optional clock that captures read data and clocks read data logic. Non-DQS mode only.</td>
</tr>
<tr>
<td>reset_clk_n</td>
<td>1</td>
<td>Input</td>
<td>Reset input for logic on the system clock domain. The <code>reset_clk_n</code> can be asserted asynchronously but must be deasserted synchronous to the rising edge of the system clock.</td>
</tr>
<tr>
<td>reset_addr_cmd_clk_n</td>
<td>1</td>
<td>Input</td>
<td>Reset input for logic on the address and command clock domain. The <code>reset_addr_cmd_clk_n</code> can be asserted asynchronously but must be deasserted synchronous to the rising edge of the address and command clock.</td>
</tr>
</tbody>
</table>
reset_read_clk_n[

DQS mode: the number of RLDRAM II devices attached to the memory interface

Non-DQS mode: 1

Input Reset input for logic on the capture clock domain. In DQS mode, the capture clock domain is capture_clk[]. In non-DQS mode, it is non_dqs_capture_clk. In DQS mode, each reset_read_clk_n[] is associated with the corresponding capture_clk[] clock domain. The reset_read_clk_n[] can be asserted asynchronously but must be deasserted synchronous to the rising edge of the capture clock.

capture_clk[]

The number of RLDRAM II devices attached to memory interface

Output Undelayed DQS clock used by capture circuitry to capture RLDRAM II read data. There is one capture_clk[] per attached RLDRAM II device. DQS mode only.

Table 2–4 shows the local interface signals.

<table>
<thead>
<tr>
<th>Name</th>
<th>Width (Bits)</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>local_addr[]</td>
<td>Device dependant</td>
<td>Input</td>
<td>RLDRAM II address. IP Toolbench refers to the memory.dat file and selects the address width appropriate to the device.</td>
</tr>
<tr>
<td>local_bank_addr[]</td>
<td>3</td>
<td>–</td>
<td>RLDRAM II bank address.</td>
</tr>
<tr>
<td>local_dm[]</td>
<td>The number of RLDRAM II devices attached to the memory interface × 2</td>
<td>Input</td>
<td>Optional local data mask (DM). Twice the width of the memory rldramii_dm[] bus. When all high, all writes are masked.</td>
</tr>
<tr>
<td>local_read_req</td>
<td>1</td>
<td>Input</td>
<td>Read request signal.</td>
</tr>
<tr>
<td>local_refresh_req</td>
<td>1</td>
<td>Input</td>
<td>User controlled refresh request. This allows complete control over when refreshes are issued to the memory. The refresh is issued to the bank address on local_bank_addr[].</td>
</tr>
</tbody>
</table>
Table 2–4. Local Interface Signals (Part 2 of 2)

<table>
<thead>
<tr>
<th>Name</th>
<th>Width (Bits)</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>local_wdata[]</td>
<td>Data-bus width × 2</td>
<td>Input</td>
<td>Write data bus. The local interface must request local_wdata[] over multiple clock cycles to construct the write data for any requested write bursts. If the memory burst length is set to two beats, the write data is requested in a single clock cycle at the local interface.</td>
</tr>
<tr>
<td>local_write_req</td>
<td>1</td>
<td>Input</td>
<td>Write request signal.</td>
</tr>
<tr>
<td>local_init_done</td>
<td>1</td>
<td>Output</td>
<td>Memory initialization complete signal which is asserted when the controller has completed its initialization of the memory. Reads and writes should not be requested until local_init_done is asserted.</td>
</tr>
<tr>
<td>local_rdata[]</td>
<td>Data-bus width × 2</td>
<td>Output</td>
<td>Read data bus. The controller returns local_rdata[] over multiple clock cycles for any requested read transactions. If the memory burst length is set to two beats, the read data is returned in a single clock cycle at the local interface.</td>
</tr>
<tr>
<td>local_rdata_valid[]</td>
<td>The number of RLDRAM II devices attached to memory interface</td>
<td>Output</td>
<td>Read data valid signal, which indicates that valid data is present on the read data bus. The local_rdata_valid[] signal is aligned with the local read data, local_rdata[]. There is only one local_rdata_valid[] per attached RLDRAM II device.</td>
</tr>
<tr>
<td>local_wdata_req</td>
<td>1</td>
<td>Output</td>
<td>Write data request signal. When the local interface asserts local_wdata_req, all the write data for the burst should be available in contiguous clock cycles.</td>
</tr>
</tbody>
</table>

Table 2–5 shows the memory interface signals.

Table 2–5. Memory Interface Signals (Part 1 of 2)

<table>
<thead>
<tr>
<th>Name</th>
<th>Width (Bits)</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>rldramii_dq[]</td>
<td>Data-bus width</td>
<td>Bidirectional</td>
<td>Memory data bus. CIO devices only.</td>
</tr>
<tr>
<td>rldramii_qk[]</td>
<td>1 to 9</td>
<td>Bidirectional</td>
<td>In DQS mode, the memory data strobe signal that captures read data into the Altera device; in non-DQS mode, the RLDRAM II controller does not use rldramii_qk[].</td>
</tr>
<tr>
<td>rldramii_q[]</td>
<td>Data-bus width</td>
<td>Input</td>
<td>Memory read data bus. SIO devices only.</td>
</tr>
<tr>
<td>Name</td>
<td>Width (Bits)</td>
<td>Direction</td>
<td>Description</td>
</tr>
<tr>
<td>---------------------</td>
<td>------------------------------------------------------------------------------</td>
<td>-----------</td>
<td>--------------------------------------------------</td>
</tr>
<tr>
<td>rldramii_qvld[]</td>
<td>The number of RLDRAM II devices attached to memory interface</td>
<td>Input</td>
<td>Read data valid flag.</td>
</tr>
<tr>
<td>rldramii_a_0[]</td>
<td>local_addr[]</td>
<td>Output</td>
<td>Memory address signals.</td>
</tr>
<tr>
<td>rldramii_a_1[]</td>
<td>(1)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>rldramii_a_0[]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>rldramii_a_1[]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>rldramii_a_0[]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>rldramii_a_1[]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>rldramii_a_0[]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>rldramii_a_1[]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>rldramii_hi_0[]</td>
<td>3</td>
<td>Output</td>
<td>Memory bank address signals.</td>
</tr>
<tr>
<td>rldramii_hi_1[]</td>
<td>(1)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>rldramii_hi_0[]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>rldramii_hi_1[]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>rldramii_clk[],</td>
<td>1 to 3 (with dedicated PLL clocks) or 1 to 8 otherwise</td>
<td>Output</td>
<td>Memory command output clock.</td>
</tr>
<tr>
<td>rldramii_clk_n[]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>rldramii_cs_n_0</td>
<td>1</td>
<td>Output</td>
<td>Memory chip select signal.</td>
</tr>
<tr>
<td>rldramii_cs_n_1</td>
<td>(1)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>rldramii_d[]</td>
<td>Data-bus width</td>
<td>Output</td>
<td>Memory write data bus. SIO devices only.</td>
</tr>
<tr>
<td>rldramii_dm[]</td>
<td>The number of RLDRAM II devices attached to memory interface</td>
<td>Output</td>
<td>Memory DM (optional).</td>
</tr>
<tr>
<td>rldramii_ref_n_0</td>
<td>1</td>
<td>Output</td>
<td>Memory refresh request signal.</td>
</tr>
<tr>
<td>rldramii_ref_n_1</td>
<td>(1)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>rldramii_ref_n_0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>rldramii_ref_n_1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>rldramii_we_n_0</td>
<td>1</td>
<td>Output</td>
<td>Memory write enable signal.</td>
</tr>
<tr>
<td>rldramii_we_n_1</td>
<td>(1)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>rldramii_we_n_0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>rldramii_we_n_1</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note to Table 2–5:
(1) The default signal is <signal>_0. When you specify additional address and command busses, both <signal>_0 and <signal>_1 are present.
Table 2–6 shows the datapath interface signals.

<table>
<thead>
<tr>
<th>Name</th>
<th>Width (Bits)</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>control_a[]</td>
<td>local_addr[]</td>
<td>Input</td>
<td>Address bits.</td>
</tr>
<tr>
<td>control.ba[]</td>
<td>3</td>
<td>Input</td>
<td>Bank address bits.</td>
</tr>
<tr>
<td>control_cs_n</td>
<td>1</td>
<td>Input</td>
<td>Chip select signal.</td>
</tr>
<tr>
<td>control_dm[]</td>
<td>The number of RLDRAM II devices attached to the memory interface × 2</td>
<td>Input</td>
<td>The DM bus, which has valid data in the same clock cycles that control_wdata_valid is asserted.</td>
</tr>
<tr>
<td>control_doing_wr</td>
<td>1</td>
<td>Input</td>
<td>Control_doing_wr is asserted when the controller is writing to the RLDRAM II devices and controls the output enables on rldramii_dq[] or rldramii_d[].</td>
</tr>
<tr>
<td>control_ref_n</td>
<td>1</td>
<td>Input</td>
<td>Refresh signal.</td>
</tr>
<tr>
<td>control_wdata[]</td>
<td>Data-bus width × 2</td>
<td>Input</td>
<td>The write data bus, which has valid data in the same clock cycles that control_wdata_valid is asserted.</td>
</tr>
<tr>
<td>control_wdata_valid</td>
<td>1</td>
<td>Input</td>
<td>Enables the write data bus and DM enable registers so that they are only updated when valid data and enables are available.</td>
</tr>
<tr>
<td>control_we_n</td>
<td>1</td>
<td>Input</td>
<td>Write enable signal.</td>
</tr>
<tr>
<td>control_qvld[]</td>
<td>The number of RLDRAM II devices attached to the memory interface</td>
<td>Output</td>
<td>The read data valid flag. There is only one QVLD flag per RLDRAM II device. The control_qvld[] signal is aligned with the valid control_rdata[] and is asserted during this period. The control_qvld[] signal has the same functionality as local_rdata_valid[].</td>
</tr>
<tr>
<td>control_rdata[]</td>
<td>Data-bus width × 2</td>
<td>Output</td>
<td>The captured read data (same as local_rdata[]).</td>
</tr>
</tbody>
</table>
# Memory

Table 2–7 shows the memory type parameters.

## Table 2–7. Memory Type Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Range</th>
<th>Units</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RLDRAM II device</td>
<td>Part number</td>
<td>–</td>
<td>A part number for a particular memory device. Choosing an entry sets many of the parameters in the wizard to the correct value for the specified part. You can add your own devices to this list by editing the <code>memory_types.dat</code> file in the <code>constraints</code> directory.</td>
</tr>
<tr>
<td>Clock speed</td>
<td>100 to 400 MHz</td>
<td>MHz</td>
<td>The memory controller clock frequency. The constraints script and the datapath use this clock speed. It must be set to the value that you intend to use. The first time you use IP Toolbench or if you turn on <strong>Update example design system PLL,</strong> it uses this value for the IP Toolbench-generated PLL's input and output clocks.</td>
</tr>
<tr>
<td>Interface voltage</td>
<td>1.5 or 1.8 V</td>
<td>V</td>
<td>The RLDRAM II interface voltage.</td>
</tr>
<tr>
<td>DQ per DQS</td>
<td>8, 9, 16, 18 Bits</td>
<td></td>
<td>Number of DQ bits per DQS input pin. CIO devices only.</td>
</tr>
<tr>
<td>Q per DQS</td>
<td>8, 9, 16, 18 Bits</td>
<td></td>
<td>Number of Q bits per DQS input pin. SIO devices only.</td>
</tr>
<tr>
<td>Data-bus width</td>
<td>Device dependent</td>
<td>Bits</td>
<td>The width of the memory interface.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>For more information about supported interface data widths, refer to <strong>AN 325: Interfacing RLDRAM II with Stratix II, Stratix &amp; Stratix GX Devices.</strong></td>
</tr>
</tbody>
</table>

Table 2–8 shows the memory initialization options.

## Table 2–8. Memory Initialization Options

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Range</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory configuration</td>
<td>1, 2, or 3.</td>
<td>Refer to your RLDRAM II data sheet.</td>
</tr>
<tr>
<td>Burst length</td>
<td>2, 4, or 8</td>
<td>Number of beats in the burst at the memory interface. The number of beats at the local interface is half this value.</td>
</tr>
<tr>
<td>Manually enter initialization clock cycles</td>
<td>On or off</td>
<td>The wizard takes the number of initialization clock cycles from the <code>memory.dat</code> file in the <code>constraints</code> directory. The number is calculated from the initialization entry time and the clock speed. You can manually enter a number for the initialization clock cycles if you turn on <strong>Manually enter initialization clock cycles.</strong></td>
</tr>
<tr>
<td>Number of initialization clock cycles</td>
<td>16 to 80,000</td>
<td>You can manually enter a number for the initialization clock cycles if you turn on <strong>Manually enter initialization clock cycles.</strong></td>
</tr>
<tr>
<td>Enable on-die termination</td>
<td>On or off</td>
<td>Refer to your RLDRAM II data sheet.</td>
</tr>
</tbody>
</table>
Parameters

**Table 2–9. Memory Interface Parameters**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Range</th>
<th>Units</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of address and command busses from FPGA to memory for multiple devices</td>
<td>1 or 2</td>
<td>–</td>
<td>Depends on the number of devices. If you connect only one device there can be only one address and command bus. (1)</td>
</tr>
<tr>
<td>Generate DM pins</td>
<td>On or off</td>
<td>–</td>
<td>Adds DM pins and logic to the design.</td>
</tr>
<tr>
<td>Use dedicated PLL outputs</td>
<td>On or off</td>
<td>–</td>
<td>Turn on to use dedicated PLL outputs to generate the clocks, which is recommended for HardCopy II devices. When turned off altddio outputs generate the clock outputs.</td>
</tr>
<tr>
<td>Number of clock pairs from FPGA to memory</td>
<td>1 to 8</td>
<td>–</td>
<td>The number of RLDRAM II clock output pairs generated in the datapath. When you turn on Use dedicated clock outputs, only values of 1 to 3 are valid.</td>
</tr>
</tbody>
</table>

**Note to Table 2–9:**
(1) The default signal is `<signal>_0`. When you specify additional address and command busses, both `<signal>_0` and `<signal>_1` are present.
Functional Description

Timing

Table 2–10 shows the pipeline options.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Range</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of address and command and write data pipeline registers</td>
<td>0, 1, 2 or 3</td>
<td>When you choose 1, 2, or 3 the wizard inserts 1, 2, or 3 pipeline registers between the memory controller and the command and address output registers and the write data output registers. These registers may help to achieve the required performance at higher frequencies.</td>
</tr>
<tr>
<td>Number of read data pipeline registers</td>
<td>0, 1, 2 or 3</td>
<td>When you choose 1, 2, or 3 the wizard inserts 1, 2, or 3 pipeline registers between the read capture registers and the memory controller. These registers may help to achieve the required performance at higher frequencies.</td>
</tr>
</tbody>
</table>

Table 2–11 shows the clocking modes.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Range</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Address and command clock</td>
<td>System, write, or dedicated</td>
<td>The clock for the address and command output registers. For system_clk choose System; for write_clk, choose Write, and for a separate clock, choose Dedicated. If you choose Dedicated for the clock, ensure the clock phase allows the Quartus II software to meet the setup time on the address and command output registers.</td>
</tr>
<tr>
<td>Address and command clock edge</td>
<td>Falling or rising</td>
<td>The clock edge on which the addresses and commands are output.</td>
</tr>
<tr>
<td>Dedicated address and command clock PLL phase offset</td>
<td>± 180°</td>
<td>Sets the dedicated address and command clock PLL phase for better timing.</td>
</tr>
<tr>
<td>Enable DQS mode</td>
<td>On or off</td>
<td>Turn on for DQS mode; otherwise the controller is in non-DQS mode (Stratix II and Stratix II GX devices only). HardCopy II devices allow DQS mode only.</td>
</tr>
<tr>
<td>Use migratable byte groups</td>
<td>On or off</td>
<td>When turned on, you can migrate the design to a migration device. When turned off the wizard allows much greater flexibility in the placement of byte groups. You can only turn on this option when Enable DQS mode is turned off.</td>
</tr>
<tr>
<td>Feedback PLL phase offset</td>
<td>± 180°</td>
<td>Sets the feedback clock PLL phase for read capture (non-DQS mode only).</td>
</tr>
</tbody>
</table>
Table 2–12 shows the pin loading parameters.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Range (pF)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pin loading on FPGA DQ/DQS pins</td>
<td>0 to 100</td>
<td>Enter the pin loading to match your board and memory devices.</td>
</tr>
<tr>
<td>Pin loading on FPGA address and command pins</td>
<td>0 to 100</td>
<td>Enter the pin loading to match your board and memory devices.</td>
</tr>
<tr>
<td>Pin loading on FPGA clock pins</td>
<td>0 to 100</td>
<td>Enter the pin loading to match your board and memory devices.</td>
</tr>
</tbody>
</table>

Project Settings

Table 2–13 shows the example design settings.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Automatically apply RLDAM II controller-specific constraints to the</td>
<td>When this option is turned on, the next time you compile, the Quartus II software automatically runs the add constraints script. Turn off this option if you do not want the script to run automatically.</td>
</tr>
<tr>
<td>Quartus II project</td>
<td></td>
</tr>
<tr>
<td>Update the example design file that instantiates the RLDAM II controller</td>
<td>When this option is turned on, IP Toolbench parses and updates the example design file. It only updates sections that are between the following markers: &lt;&lt;START MEGAWIZARD INSERT &lt;tagname&gt; &lt;&lt;END MEGAWIZARD INSERT &lt;tagname&gt; \</td>
</tr>
<tr>
<td>Update example design system PLL</td>
<td>When this option is turned on, IP Toolbench automatically overwrites the PLL. Turn off this option, if you do not want the wizard to overwrite the PLL.</td>
</tr>
</tbody>
</table>

If you edit the example design file, ensure that your changes are outside of the markers or remove the markers. Once you remove the markers, you must keep the file updated, because IP Toolbench can no longer update the file.
Table 2–14 shows the variation path parameters.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Enable hierarchy control</td>
<td>The constraints script analyzes your design, to automatically extract the hierarchy to your variation. To prevent the constraints script analyzing your design, turn on <strong>Enable Hierarchy Control</strong>, and enter the correct hierarchy path to your datapath.</td>
</tr>
<tr>
<td>Hierarchy path to RLDRAM II controller datapath</td>
<td>The hierarchy path is the path to your RLDRAM II controller datapath, minus the top-level name. The hierarchy entered in the wizard must match your design, because the constraints scripts rely on this path for correct operation.</td>
</tr>
</tbody>
</table>

Table 2–15 shows the device pin prefixes parameter.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Prefix all RLDRAM II pins on the device with</td>
<td>This string prefixes the pin names for the FPGA pins that are connected to the RLDRAM II controller.</td>
</tr>
</tbody>
</table>

**MegaCore Verification**

MegaCore verification involves simulation testing and hardware testing.

**Simulation Environment**

Altera has carried out extensive functional tests using industry-standard models to ensure the functionality of the RLDRAM II controller. In addition, Altera has carried out a wide variety of gate-level tests on the RLDRAM II controller to verify the post-compilation functionality of the controller.

**Hardware Testing**

Table 2–16 shows the Altera development board on which Altera hardware tested the RLDRAM II controller.

<table>
<thead>
<tr>
<th>Development Board</th>
<th>Altera Device</th>
<th>Memory Device</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stratix II Memory Demonstration Board 1</td>
<td>EP2S60F1020C3</td>
<td>Micron 18-bit CIO and SIO RLDRAM II devices</td>
</tr>
</tbody>
</table>
Design Flow

To evaluate the RLDRAM II Controller MegaCore function using the OpenCore Plus feature, include these steps in your design flow:

1. Obtain and install the RLDRAM II Controller MegaCore Function.

The RLDRAM II Controller is part of the MegaCore IP Library, which is distributed with the Quartus II software and downloadable from the Altera website, www.altera.com.

For system requirements and installation instructions, refer to Altera Software Installation and Licensing.

Figure 3–1 shows the directory structure after you install the RLDRAM II Controller, where <path> is the installation directory. The default installation directory on Windows is c:\altera\<version>; on Linux it is /opt/altera<version>.

**Figure 3–1. RLDRAM II Controller Directory Structure**

- `<path>`
  - Installation directory.
- `ip`
  - Contains the Altera MegaCore IP Library and third-party IP cores.
- `altera`
  - Contains the Altera MegaCore IP Library.
- `common`
  - Contains shared components.
- `rldram_ii_controller`
  - Contains the RLDRAM II Controller MegaCore function files and documentation.
- `constraints`
  - Contains scripts that generate an instance-specific Tcl script for each instance of the RLDRAM II Controller in various Altera devices.
- `dat`
  - Contains a data file for each Altera device combination that is used by the Tcl script to generate the instance-specific Tcl script.
- `doc`
  - Contains the documentation for the RLDRAM II Controller MegaCore function.
- `lib`
  - Contains encrypted lower-level design files and other support files.

2. Create a custom variation of the RLDRAM II Controller MegaCore function using IP Toolbench.
IP Toolbench is a toolbar from which you quickly and easily view documentation, specify parameters, and generate all of the files necessary for integrating the parameterized MegaCore function into your design.

3. Implement the rest of your design using the design entry method of your choice.

4. Use the IP Toolbench-generated IP functional simulation model to verify the operation of your design.

For more information on IP functional simulation models, refer to the Simulating Altera IP in Third-Party Simulation Tools chapter in volume 3 of the Quartus II Handbook.

5. Edit the PLL.

6. Use the Quartus II software to add constraints to the example design and compile the example design.

7. Perform gate-level timing simulation, or if you have a suitable development board, you can generate an OpenCore Plus time-limited programming file, which you can use to verify the operation of the example design in hardware.

8. Either obtain a license for the RLDRAM II controller MegaCore function or replace the encrypted RLDRAM II controller control logic with your own logic and use the clear-text datapath.

   If you obtain a license for the RLDRAM II controller, you must set up licensing.

9. Generate a programming file for the Altera device(s) on your board.

10. Program the Altera device(s) with the completed design.

This walkthrough explains how to create a RLDRAM II controller using the Altera RLDRAM II controller IP Toolbench and the Quartus II software on a PC. When you are finished generating a custom variation of the RLDRAM II controller MegaCore function, you can incorporate it into your overall project.

This walkthrough requires the following steps:

- “Create a New Quartus II Project” on page 3–3
- “Launch IP Toolbench” on page 3–4
Create a New Quartus II Project

You need to create a new Quartus II project with the New Project Wizard, which specifies the working directory for the project, assigns the project name, and designates the name of the top-level design entity. To create a new project follow these steps:

1. Choose Programs > Altera > Quartus II <version> (Windows Start menu) to run the Quartus II software. Alternatively, you can use the Quartus II Web Edition software.

2. Choose New Project Wizard (File menu).

3. Click Next in the New Project Wizard Introduction page (the introduction page does not display if you turned it off previously).

4. In the New Project Wizard: Directory, Name, Top-Level Entity page, enter the following information:
   a. Specify the working directory for your project. For example, this walkthrough uses the c:\altera\projects\rldram_project directory.
   b. Specify the name of the project. This walkthrough uses project for the project name.

   The Quartus II software automatically specifies a top-level design entity that has the same name as the project. Do not change it.

5. Click Next to close this page and display the New Project Wizard: Add Files page.

   When you specify a directory that does not already exist, a message asks if the specified directory should be created. Click Yes to create the directory.

6. If you installed the MegaCore IP Library in a different directory from where you installed the Quartus II software, you must add the user libraries:
   a. Click User Libraries.
b. Type `<path>\ip` into the Library name box, where `<path>` is the directory in which you installed the RLDRAM II controller.

c. Click Add to add the path to the Quartus II project.

d. Click OK to save the library path in the project.

7. Click Next to close this page and display the New Project Wizard: Family & Device Settings page.


9. The remaining pages in the New Project Wizard are optional. Click Finish to complete the Quartus II project.

You have finished creating your new Quartus II project.

Launch IP Toolbench

To launch IP Toolbench in the Quartus II software, follow these steps:


   ![Refer to Quartus II Help for more information on how to use the MegaWizard Plug-In Manager.](image)

2. Specify that you want to create a new custom megafunction variation and click Next.

3. Expand the Interfaces > Memory Controllers directory, then click RLDRAM II Controller v9.1.

4. Select the output file type for your design; the wizard supports VHDL and Verilog HDL.

5. The MegaWizard Plug-In Manager shows the project path that you specified in the New Project Wizard. Append a variation name for the MegaCore function output files `<project path>\<variation name>`.

   ![The `<variation name>` must be a different name from the project name and the top-level design entity name.](image)

6. Click Next to launch IP Toolbench.
Step 1: Parameterize

To parameterize your MegaCore function, follow these steps:

For more information on parameters, refer to "Parameters" on page 2–28.

1. Click Step 1: Parameterize in IP Toolbench.

2. Choose the memory type.
   a. Choose the memory device.
      - You can add your own memory devices to this list by editing the memory_types.dat file in the constraints directory.
   b. Enter the clock speed.
   c. Choose the interface voltage.
   d. Choose the data bus width.
   e. Choose the DQ per DQS (CIO devices), or the Q per DQS (SIO devices).

3. Choose the memory initialization options.

4. Choose your memory interface parameters.

5. Click the Timing tab.
   For more information on timing parameters, refer to "Timing" on page 2–31.

6. Enter the datapath pipeline options.

7. Choose the clocking modes.

8. Turn on the appropriate capture mode—DQS or non-DQS capture mode. If you turn off Enable DQS mode (non-DQS capture mode), you can turn on Use migratable bytegroups.

9. Click the Project Settings tab.
   For more information on project settings, refer to "Project Settings" on page 2–32.
10. Altera recommends that you turn on **Automatically apply RLDRAM II controller-specific constraints to the Quartus II project** so that the Quartus II software automatically applies the constraints script when you compile the example design.

You must turn on this option, the first time you run IP Toolbench.

11. Ensure **Update the example design file that instantiates the RLDRAM II controller variation** is turned on, for IP Toolbench to automatically update the example design file.

You must turn on this option, the first time you run IP Toolbench.

12. Turn off **Update example design system PLL**, if you have edited the PLL and you do not want the wizard to regenerate the PLL when you regenerate the variation.

You must turn on this option, the first time you run IP Toolbench.

13. The constraints script automatically detects the hierarchy of your design. The constraints script analyzes and elaborates your design to automatically extract the hierarchy to your variation. To prevent the constraints script analyzing and elaborating your design, turn on **Enable Hierarchy Control**, and enter the correct hierarchy path to your datapath. **Figure 3–2** shows the following example hierarchy:

```
my_system:my_system_inst|my_sub_system:my_sub_system_inst|
my_rldramii:my_rldramii_inst|datapath:datapath_inst|
```
14. IP Toolbench uses a prefix (for example, rldramii_) for the names of all memory interface pins. Enter a prefix for all memory interface pins associated with this custom variation.

15. Enter the pin loading for the FPGA pins.

   ![You must enter suitable values for the pin loading, because the values affect timing.]

16. Click Finish.

**Step 2: Constraints**

To choose the constraints for your device, follow these steps:

1. Click **Step 2: Constraints** in IP Toolbench.

2. Choose the positions on the device for each of the RLDRAM II byte groups. To place a byte group, select the byte group in the drop-down box at your chosen position.

   ![The floorplan matches the orientation of the Quartus II floorplanner. The layout represents the die as viewed from above. A byte group consists of data (DQ) pins for CIO devices; or data (Q) pins for SIO devices, and a data strobe signal (DQS) pin. The number of data pins per byte group matches your choice of DQ (or Q) per DQS.]

Step 3: Set Up Simulation

An IP functional simulation model is a cycle-accurate VHDL or Verilog HDL model produced by the Quartus II software. The model allows for fast functional simulation of IP using industry-standard VHDL and Verilog HDL simulators.

You may only use these simulation model output files for simulation purposes and expressly not for synthesis or any other purposes. Using these models for synthesis will create a nonfunctional design.

To generate an IP functional simulation model for your MegaCore function, follow these steps:

1. Click Step 3: Set Up Simulation in IP Toolbench.
2. Turn on Generate Simulation Model.
3. Choose the language in the Language list.
4. Some third-party synthesis tools can use a netlist that contains only the structure of the MegaCore function, but not detailed logic, to optimize performance of the design that contains the MegaCore function. If your synthesis tool supports this feature, turn on Generate netlist.
5. Click OK.

Step 4: Generate

To generate your MegaCore function, click Step 4: Generate in IP Toolbench.
Table 3–1 describes the generated files and other files that may be in your project directory. The names and types of files specified in the IP Toolbench report vary based on whether you created your design with VHDL or Verilog HDL.

<table>
<thead>
<tr>
<th>Filename</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt;variation name&gt;.vhd, or .v</td>
<td>A MegaCore function variation file, which defines a VHDL or Verilog HDL description of the custom MegaCore function. Instantiate the entity defined by this file inside of your design. Include this file when compiling your design in the Quartus II software.</td>
</tr>
<tr>
<td>&lt;variation name&gt;.cmp</td>
<td>A VHDL component declaration file for the MegaCore function variation. Add the contents of this file to any VHDL architecture that instantiates the MegaCore function.</td>
</tr>
<tr>
<td>&lt;variation name&gt;.bsf</td>
<td>Quartus II symbol file for the MegaCore function variation. You can use this file in the Quartus II block diagram editor.</td>
</tr>
<tr>
<td>&lt;variation name&gt;.sdc</td>
<td>A Synopsys Design Constraints (SDC) file. Use this SDC file with the DDR timing wizard (DTW)-generated SDC file when using TimeQuest. You must copy the contents of this file into the DTW-generated SDC file, so the example design has the correct timing constraints when using TimeQuest.</td>
</tr>
<tr>
<td>altera_vhdl_support.vhd</td>
<td>A VHDL package that contains functions for the generated entities. This file may be shared between MegaCore functions.</td>
</tr>
<tr>
<td>&lt;variation name&gt;_example_driver.vhd or .v</td>
<td>Example driver.</td>
</tr>
<tr>
<td>&lt;top-level name&gt;.vhd or .v</td>
<td>Example design file.</td>
</tr>
<tr>
<td>add_constraints_for_&lt;variation name&gt;.tcl</td>
<td>Add constraints script.</td>
</tr>
<tr>
<td>rldramii_pll_&lt;device name&gt;.vhd or .v</td>
<td>System PLL.</td>
</tr>
<tr>
<td>rldramii_fbpll_&lt;device name&gt;.vhd or .v</td>
<td>Feedback PLL.</td>
</tr>
<tr>
<td>&lt;variation name&gt;_auk_rldramii_addr_cmd_reg.vhd or .v</td>
<td>Address and command output registers.</td>
</tr>
<tr>
<td>&lt;variation name&gt;_auk_rldramii_clk_gen.vhd or .v</td>
<td>Memory clock generator.</td>
</tr>
<tr>
<td>&lt;variation name&gt;_auk_rldramii_controller_ipfs_wrapper.vhd or .v</td>
<td>A file that instantiates the controller.</td>
</tr>
<tr>
<td>&lt;variation name&gt;_auk_rldramii_controller_ipfs_wrapper.vo or .vo</td>
<td>VHDL or Verilog HDL IP functional simulation model.</td>
</tr>
<tr>
<td>&lt;variation name&gt;_auk_rldramii_datapath.vhd or .v</td>
<td>Datapath.</td>
</tr>
</tbody>
</table>
1. After you review the generation report, click **Exit** to close IP Toolbench.

The Quartus II IP File (.qip) is a file generated by the MegaWizard interface, and contains information about the generated IP core. You are prompted to add this .qip file to the current Quartus II project at the time of file generation. In most cases, the .qip file contains all of the necessary assignments and information required to process the core or system in the Quartus II compiler. Generally, a single .qip file is generated for each MegaCore function or system in the Quartus II compiler.

Now, simulate the example design (refer to “Simulate the Example Design” on page 3–11), edit the PLL(s), and compile (refer to “Compile the Example Design” on page 3–14).
Simulate the Example Design

This section describes the following simulation techniques:

- Simulate with IP Functional Simulation Models
- Simulating in Third-Party Simulation Tools Using NativeLink

Simulate with IP Functional Simulation Models

You can simulate the example design using the IP Toolbench-generated IP functional simulation models. IP Toolbench generates a VHDL or Verilog HDL testbench for your example design, which is in the testbench directory in your project directory.

For more information on the testbench, refer to “Example Design” on page 2–14.

You can use the IP functional simulation model with any Altera-supported VHDL or Verilog HDL simulator. To simulate the example design with the ModelSim® simulator, follow these steps:

1. Obtain a memory model that matches your chosen parameters and save it to the <directory name>/testbench directory. For example, you can download a RLDRAM II model from the Micron web site at www.micron.com.

   Before running the simulation you may also need to edit the testbench to match the chosen RLDRAM II model.

2. Start the ModelSim-Altera simulator.

3. Change your working directory to your IP Toolbench-generated file directory <directory name>/testbench/modelsim.

4. To simulate with an IP functional simulation model simulation, type the following command:

   ```
   source <variation name>_vsm.tcl
   ```

   Before running the simulation, you may have to edit the set memory model parameter in the <variation name>_vsm.tcl file to match the selected RLDRAM II model.

5. For a gate-level timing simulation (VHDL or Verilog HDL ModelSim output from the Quartus II software), type the following commands:

   ```
   set use_gate_model 1
   ```
Simulating in Third-Party Simulation Tools Using NativeLink

You can perform a simulation in a third-party simulation tool from within the Quartus II software, using NativeLink.

For more information on NativeLink, refer to the Simulating Altera IP in Third-Party Simulation Tools chapter in volume 3 of the Quartus II Handbook.

To set up simulation in the Quartus II software using NativeLink, follow these steps:

1. Create a custom variation with an IP functional simulation model.
2. Obtain and copy an RLDRAM II model to a suitable location, for example, the testbench directory.
   Before running the simulation you may also need to edit the testbench to match the chosen RLDRAM II model.
3. Check that the absolute path to your third-party simulator executable is set. On the Tools menu click Options and select EDA Tools Options.
4. On the Processing menu, point to Start and click Start Analysis & Elaboration.
5. On the Assignments menu click Settings, expand EDA Tool Settings and select Simulation. Select a simulator under Tool Name and in NativeLink Settings, select Compile Test Bench and click Test Benches.
6. Click New.
7. Enter a name for the Test bench name.
8. Enter the name of the automatically generated testbench, <project name>_tb, in Test bench entity.
9. Enter the name of the top-level instance in Instance.
10. Change Run for to 80 μs.

source <variation name>_vsim.tcl
11. Add the testbench files. In the **File name** field browse to the location of the RLDRAM II model and the testbench, `<project name>_tb`, click **OK** and click **Add**.

12. Click **OK**.

13. Click **OK**.

14. On the Tools menu point to **EDA Simulation Tool** and click **Run EDA RTL Simulation**.

### Edit the PLL

The IP Toolbench-generated example design includes a PLL, which has an input to output clock ratio of 1:1 and a clock frequency that you entered in IP Toolbench. In addition, IP Toolbench correctly sets all the phase offsets of all the relevant clock outputs for your design. You can edit the PLL input clock to make it conform to your system requirements. If you re-run IP Toolbench and wish to save your PLL edits, turn off **Update example design system PLL**.

If you turn off **Enable DQS mode**, IP Toolbench generates a second PLL—the feedback PLL. You need not edit the feedback PLL.

For more information on the PLL, refer to “PLL Configuration” on page 2–12.

To edit the example PLL, follow these steps:

1. Choose **MegaWizard Plug-In Manager** (Tools menu).

2. Select **Edit an existing custom megafunction variation** and click **Next**.

3. In your Quartus II project directory, for VHDL choose `rldramii_pll_<device name>.vhd`; for Verilog HDL choose `rldramii_pll_<device name>.v`.

4. Click **Next**.

5. Edit the PLL parameters in the **altpll** MegaWizard Plug-In.

For more information on the **altpll** megafunction, refer to the Quartus II Help or click **Documentation** in the **ALTPLL** MegaWizard Plug-In.
Compile the Example Design

Before the Quartus II software compiles the example design it runs the IP Toolbench-generated Tcl constraints script, `auto_add_rldramii_constraints.tcl`, which calls the `add_constraints_for_<variation name>.tcl` script for each variation in your design. The `add_constraints_for_<variation name>.tcl` script checks for any previously added constraints, removes them, and then adds constraints for that variation.

The constraints script analyzes and elaborates your design, to automatically extract the hierarchy to your variation. To prevent the constraints script analyzing and elaborating your design, turn on **Enable Hierarchy Control** in the wizard, and enter the correct hierarchy path to your datapath (refer to step 13 on page 3–6).

When the constraints script runs, it creates another script, `remove_constraints_for_<variation name>.tcl`, which you can use to remove the constraints from your design.

To compile the example instance, follow these steps:

1. Choose **Start Compilation** (Processing menu), which runs the add constraints scripts, compiles the example design, and performs timing analysis.

2. View the Timing Analyzer to verify your design meets timing.

If the compilation does not reach the frequency requirements, follow these steps:

1. Choose **Settings** (Assignments menu).

2. Expand **Analysis and Synthesis Settings** in the category list.

3. Select **Speed** in Optimization Technique.

4. Expand **Fitter Settings**.

5. Turn on **Optimize Hold Timing** and select **All Paths**.

6. Turn on **Fast-corner timing**.

7. Click **OK**.

8. Re-compile the example design by choosing **Start Compilation** (Processing menu).
To achieve a higher frequency, increase the number of address and command and write data pipeline registers, or increase the number read data pipeline registers, refer to step 6 on page 3–5.

To view the constraints in the Quartus II Assignment Editor, choose Assignment Editor (Assignments menu).

If you have “?” characters in the Quartus II Assignment Editor, the Quartus II software cannot find the entity to which it is applying the constraints, probably because of a hierarchy mismatch. Either edit the constraints script, or enter the correct hierarchy path in the Project Settings tab (refer to step 13 on page 3–6).

For more information on constraints, refer to “Constraints” on page 2–16.

Program a Device

After you have compiled the example design, you can perform gate-level simulation (refer to “Simulate the Example Design” on page 3–11) or program your targeted Altera device to verify the example design in hardware.

With Altera's free OpenCore Plus evaluation feature, you can evaluate the RLDRAM II Controller MegaCore function before you obtain a license. OpenCore Plus evaluation allows you to generate an IP functional simulation model, and produce a time-limited programming file.

For more information on OpenCore Plus hardware evaluation using the RLDRAM II Controller MegaCore function, refer to “OpenCore Plus Evaluation” on page 1–4, “OpenCore Plus Time-Out Behavior” on page 2–12, and AN 320: OpenCore Plus Evaluation of Megafunctions.

Implement Your Design

In the MegaWizard flow, to implement your design based on the example design, replace the example driver in the example design with your own logic.

A FIFO buffer is not implemented in the core; you must implement a FIFO buffer.

Set Up Licensing

You need to obtain a license for the MegaCore function only when you are completely satisfied with its functionality and performance, and want to take your design to production.
After you obtain a license for RLDRAM II controller, you can request a license file from the Altera web site at www.altera.com/licensing and install it on your computer. When you request a license file, Altera emails you a `license.dat` file. If you do not have Internet access, contact your local Altera representative.
Additional Information

Revision History

The table below displays the revision history for the chapters in this user guide.

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Changes Made</th>
</tr>
</thead>
<tbody>
<tr>
<td>November 2009</td>
<td>9.1</td>
<td>Updated the release information.</td>
</tr>
<tr>
<td>March 2009</td>
<td>9.0</td>
<td>Updated the release information.</td>
</tr>
<tr>
<td>November 2008</td>
<td>8.1</td>
<td>Updated the release information.</td>
</tr>
<tr>
<td>May 2008</td>
<td>8.0</td>
<td>● Added timing assignment information for capture to first level resynchronization registers</td>
</tr>
<tr>
<td>May 2007</td>
<td>7.1</td>
<td>No changes.</td>
</tr>
<tr>
<td>March 2007</td>
<td>7.0</td>
<td>No changes.</td>
</tr>
<tr>
<td>December 2006</td>
<td>6.1</td>
<td>● Added timing assignment information for 18 and 36-bit RLDRAM II devices</td>
</tr>
<tr>
<td>April 2006</td>
<td>1.1.0</td>
<td>● Added timing assignment information for 18 and 36-bit RLDRAM II devices</td>
</tr>
<tr>
<td>October 2005</td>
<td>1.0.0</td>
<td>First published.</td>
</tr>
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</table>

How to Contact Altera

For the most up-to-date information about Altera products, refer to the following table.

<table>
<thead>
<tr>
<th>Information Type</th>
<th>Contact Note (1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technical support</td>
<td><a href="http://www.altera.com/mysupport/">www.altera.com/mysupport/</a></td>
</tr>
<tr>
<td>Technical training</td>
<td><a href="http://www.altera.com/training/">www.altera.com/training/</a></td>
</tr>
<tr>
<td>Technical training services</td>
<td><a href="mailto:custrain@altera.com">custrain@altera.com</a></td>
</tr>
<tr>
<td>Product literature</td>
<td><a href="http://www.altera.com/literature">www.altera.com/literature</a></td>
</tr>
<tr>
<td>FTP site</td>
<td>ftp.altera.com</td>
</tr>
</tbody>
</table>

Note to table:  
(1) You can also contact your local Altera sales office or sales representative.
## Typographic Conventions

This document uses the typographic conventions shown below.

<table>
<thead>
<tr>
<th>Visual Cue</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Bold Type with Initial Capital Letters</strong></td>
<td>Indicates command names, dialog box titles, dialog box options, and other GUI labels. For example, <em>Save As</em> dialog box.</td>
</tr>
<tr>
<td><strong>bold type</strong></td>
<td>Indicates directory names, project names, disk drive names, file names, file name extensions, and software utility names. For example, \qdesigns directory, <em>d</em>: drive, and <em>chiptrip</em>.pdf file.</td>
</tr>
<tr>
<td><strong>Italic Type with Initial Capital Letters</strong></td>
<td>Indicates document titles. For example, <em>AN 519: Stratix IV Design Guidelines</em>.</td>
</tr>
<tr>
<td><strong>Italic type</strong></td>
<td>Indicates variables. For example, <em>n</em> + 1. Variable names are enclosed in angle brackets (&lt; &gt;). For example, <em>&lt;file name&gt;</em> and <em>&lt;project name&gt;</em>.pdf file.</td>
</tr>
<tr>
<td><strong>Initial Capital Letters</strong></td>
<td>Indicates keyboard keys and menu names. For example, <em>Delete</em> key, and the <em>Options</em> menu.</td>
</tr>
<tr>
<td><strong>“Subheading Title”</strong></td>
<td>Quotation marks indicate references to sections within a document and titles of Quartus II Help topics. For example, “Typographic Conventions.”</td>
</tr>
<tr>
<td><strong>Courier type</strong></td>
<td>Indicates signal, port, register, bit, block, and primitive names. For example, <em>data1</em>, <em>tdi</em>, and <em>input</em>. Active-low signals are denoted by suffix <em>n</em>. For example, <em>resetn</em>. Indicates command line commands and anything that must be typed exactly as it appears. For example, <em>c:\qdesigns\tutorial\chiptrip</em>.pdf*. Also, indicates sections of an actual file, such as a Report File, references to parts of files (for example, the AHDL keyword <em>SUBDESIGN</em>), and logic function names (for example, <em>TRI</em>).</td>
</tr>
<tr>
<td>1., 2., 3., and a., b., c., etc.</td>
<td>Numbered steps indicate a list of items when the sequence of the items is important, such as the steps listed in a procedure.</td>
</tr>
<tr>
<td>■ ● </td>
<td>Bullets indicate a list of items when the sequence of the items is not important.</td>
</tr>
<tr>
<td>■</td>
<td>The hand points to information that requires special attention.</td>
</tr>
<tr>
<td>□ □ □</td>
<td>A caution calls attention to a condition or possible situation that can damage or destroy the product or your work.</td>
</tr>
<tr>
<td>□</td>
<td>A warning calls attention to a condition or possible situation that can cause injury.</td>
</tr>
<tr>
<td>↪</td>
<td>The angled arrow instructs you to press Enter.</td>
</tr>
<tr>
<td>▼</td>
<td>The feet direct you to more information about a particular topic.</td>
</tr>
</tbody>
</table>