PowerPlay Early Power Estimator User Guide

For Stratix, Stratix GX & Cyclone FPGAs

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About this User Guide

Revision History

The table below displays the revision history for the chapters in this user guide.

Date	Version	Changes Made
October 2005	2.0	• Changed product name from Power Calculator User Guide to PowerPlay Early Power Estimator User Guide for Stratix Stratix GX & Cyclone FPGAs • Global change from Power Calculator to PowerPlay early power estimator • Updated Chapter 3: Clock Network section • Updated PowerPlay early power estimator graphics
February 2004	1.0	First publication

How to Contact Altera

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Information Type	USA & Canada	All Other Locations
Technical support	www.altera.com/mysupport/	www.altera.com/mysupport/
	(800) 800-EPLD (3753) (7:00 a.m. to 5:00 p.m. Pacific Time)	(408) 544-7000 *(1)* (7:00 a.m. to 5:00 p.m. Pacific Time)
Product literature	www.altera.com	www.altera.com
Altera literature services	literature@altera.com *(1)*	literature@altera.com *(1)*
Non-technical customer service	(800) 767-3753 (7:00 a.m. to 5:00 p.m. Pacific Time)	(408) 544-7000 (7:30 a.m. to 5:30 p.m. Pacific Time)
FTP site	ftp.altera.com	ftp.altera.com

Note to table:
(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

This document uses the typographic conventions shown below.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Command names, dialog box titles, checkbox options, and dialog box options are shown in bold, initial capital letters. Example: **Save As** dialog box.
bold type	External timing parameters, directory names, project names, disk drive names, filenames, filename extensions, and software utility names are shown in bold type. Examples: $\mathbf{f_{MAX}}$, **\qdesigns** directory, **d:** drive, **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Document titles are shown in italic type with initial capital letters. Example: *AN 75: High-Speed Board Design.*
Italic type	Internal timing parameters and variables are shown in italic type. Examples: t_{PIA}, $n + 1$. Variable names are enclosed in angle brackets (< >) and shown in italic type. Example: *<file name>*, *<project name>***.pof** file.
Initial Capital Letters	Keyboard keys and menu names are shown with initial capital letters. Examples: Delete key, the Options menu.
"Subheading Title"	References to sections within a document and titles of on-line help topics are shown in quotation marks. Example: "Typographic Conventions."
`Courier type`	Signal and port names are shown in lowercase Courier type. Examples: `data1`, `tdi`, `input`. Active-low signals are denoted by suffix `n`, e.g., `resetn`. Anything that must be typed exactly as it appears is shown in Courier type. For example: `c:\qdesigns\tutorial\chiptrip.gdf`. Also, sections of an actual file, such as a Report File, references to parts of files (e.g., the AHDL keyword `SUBDESIGN`), as well as logic function names (e.g., `TRI`) are shown in Courier.
1., 2., 3., and a., b., c., etc.	Numbered steps are used in a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ● •	Bullets are used in a list of items when the sequence of the items is not important.
✓	The checkmark indicates a procedure that consists of one step only.
	The hand points to information that requires special attention.
	The caution indicates required information that needs special consideration and understanding and should be read prior to starting or continuing with the procedure or process.
	The warning indicates information that should be read prior to starting or continuing the procedure or processes
↵	The angled arrow indicates you should press the Enter key.
	The feet direct you to more information on a particular topic.

1. About the PowerPlay Early Power Estimator for Stratix, Stratix GX & Cyclone FPGAs

Release Information

Table 1–1 provides information on the version of the PowerPlay early power estimator documented in this user guide.

Table 1–1. PowerPlay Early Power Estimator Versions

Device Family	Early Power Estimator Version
Stratix	3.11 and later
Stratix GX	2.1 and later
Cyclone	2.1 and later

Device Family Support

The *PowerPlay Early Power Estimator User Guide* provides full support for the target Altera device families listed in Table 1–2.

Table 1–2. Device Family Support

Device Family	Support
Stratix	Full
Stratix GX	Full
Cyclone	Full

General Description

As designs grow larger and processes continue to shrink, power becomes an increasing concern. PCB designers need an accurate estimate of the amount of power the device consumes to develop an appropriate power budget, and to design the power supplies, the voltage regulators, the heat sink, and the cooling system. You can estimate a Stratix®, Stratix GX, or Cyclone™ device's power using the Microsoft Excel-based PowerPlay early power estimator available from the Altera web site or the simulation-based power estimation feature in the Quartus® II software. You need to enter the device resources, operating frequency, toggle rates, and other parameters in the PowerPlay early power estimator.

The PowerPlay early power estimator spreadsheets for Stratix, Stratix GX, and Cyclone devices provide a current (I_{CC}) and power (P) estimation based on typical conditions (room temperature and nominal V_{CC}).

This user guide explains how to use the Stratix PowerPlay early power estimator version 3.11, Stratix GX PowerPlay early power estimator version 2.1, and Cyclone PowerPlay early power estimator version 2.1 to estimate device power consumption.

These PowerPlay early estimators are used to estimate power consumption, and not used as a specification. Be sure to verify the actual I_{CC} during device operation, as this measurement is sensitive to the actual device design and the environmental operating conditions.

For more information about available device resources, I/O standard support, and other device features, refer to the appropriate device family handbook.

Features

The features of the PowerPlay early power estimator include:

- Estimate your design's power usage before creating the design, during the design process, or after the design is complete
- Import device resource information from the Quartus II software into the PowerPlay early power estimator with the use of the Quartus II-generated power estimation file
- Perform preliminary thermal analysis of your design

2. Setting Up PowerPlay Early Power Estimator for Stratix, Stratix GX & Cyclone FPGAs

System Requirements

The PowerPlay early power estimator requires:

- Windows NT/2000/XP operating system
- Microsoft Excel 2002 or higher
- Quartus II software 5.0 or higher

Download & Install the PowerPlay Early Power Estimator

The PowerPlay early power estimator for Stratix®, Stratix GX, or Cyclone™ devices are available from the Altera web site (**www.altera.com**). After reading the terms and conditions, click the **I Agree** button, to download the Microsoft Excel file to your hard drive.

By default, the Microsoft Excel 2002 macro security level is set to **High**. When the macro security level is set to **High**, macros are automatically disabled. To change the macro security level in Microsoft Excel 2002, choose **Options** (Tools menu). On the **Security** tab of the **Options** window, click **Macro Security**. On the **Security Level** tab of the **Security** dialog box, chose **Medium**. When the macro security level is set to **Medium**, a pop-up window asks you whether to enable macros or disable macros each time you open a spreadsheet that contains macros. After changing the macro security level, you must close the spreadsheet and re-open it in order to use the macros.

Entering Information into the PowerPlay Early Power Estimator

You can either manually enter power information into the PowerPlay early power estimator or load a power estimation file generated by the Quartus II software 5.0 or higher. You can also clear all the values currently in the PowerPlay early power estimator.

Clearing All Values

You can reset all of the user entered values in the PowerPlay early power estimator by clicking **Reset All Values**.

To use the **Reset All Values** feature, enable macros for the spreadsheet. If you did not enabled macros for the spreadsheet, you need to reset all user-entered values manually.

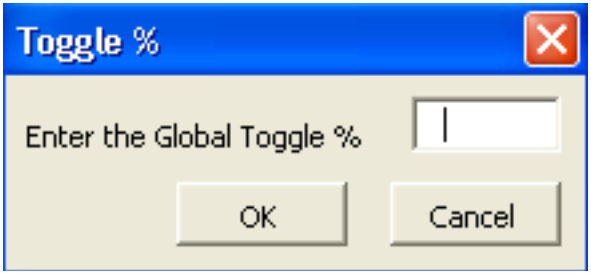
Entering Global Toggle Rate

You can enter a global toggle percentage for the entire design by clicking **Enter Toggle %**. You can manually change any toggle rate from the user-entered value after clicking **Enter Toggle%**. To enter a global toggle rate into the PowerPlay early power estimator, perform the following steps:

1. Click **Enter Toggle %** in the PowerPlay early power estimator.
2. Enter toggle percentage from 1% to 100% into the ***Toggle %*** dialog box (Figure 2–1).
3. Click **OK** to populate all toggle percentage field with the specified value.

If **Toggle %** dialog box is left blank or not specified, the default toggle rate is 12.5%.

Figure 2–1. Toggle % Dialog Box



Manually Entering Information

You can manually enter values into the PowerPlay early power estimator in the appropriate section.

Importing a File

If you already have an existing design or a partially completed design, the power estimation file generated by the Quartus II software contains the device resource information. You can import this device resource information from the Quartus II software power estimation file into the PowerPlay early power estimator. Importing a file saves you time and

effort otherwise spent manually entering information into the PowerPlay early power estimator. You can manually change any of the values after importing a file.

To generate the power estimation file:

1. Compile your design in the Quartus II software.
2. Click **Generate PowerPlay Early Power Estimator File** (Project menu).
3. Browse to a power estimation file generated from the Quartus II software. The file name is:

   <*revision_name*>**_early_pwr.txt**

For more information on generating the power estimation file in the Quartus II software, refer to the *Early Power Estimation* chapter in the *Quartus II Handbook*.

To import data into the PowerPlay early power estimator, perform the following steps:

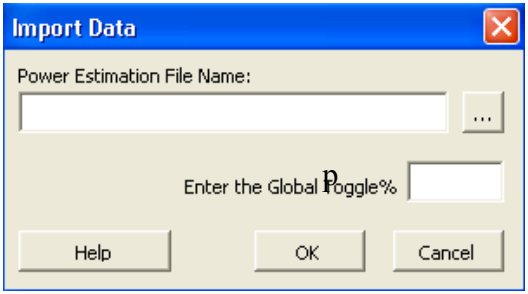
1. Click **Select Import File** in the PowerPlay early power estimator. A **Import Data** dialog box opens (Figure 2–2).
2. Browse to a power estimation file generated from the Quartus II software. The file name is:

   <*revision_name*>**_early_pwr.txt**

3. Enter the global toggle rate. If you leave this box blank, the default global toggle rate is 12.5%.
4. Click **Load Import File OK**.

Clicking **Load Import File OK** clears any user-entered values in the PowerPlay early power estimator and populates the PowerPlay early power estimator with device resource information from the specified power estimation file.

Figure 2–2. Import Data Dialog Box



After running the Import Data macro, you must manually select the appropriate RAM block mode in the **Mode** column of the **RAM Blocks** section.

The f_{MAX} imported into the PowerPlay early power estimator is the same as the f_{MAX} reported in the Quartus II timing analyzer. You can manually edit the f_{MAX} and toggle percentage in the PowerPlay early power estimator to suit your system requirements.

If your design has more than 10 design modules, the Import Data macro instructs you to check the <*project name*>**_early_pwr_errors pwr_est_errors.txt** file for errors. You should verify that the entries in the PowerPlay power estimation file are valid design modules. If they are valid design modules, manually enter these resources into the PowerPlay early power estimator.

You can merge similar design modules into one common row entry. For example, if the f_{MAX} for one logic element (LE) design module is only slightly higher or lower than another, you can enter this information into one row in the PowerPlay early power estimator by entering the higher f_{MAX} and adding the LE resources used. If the design modules are completely different, you can manually enter the additional design modules into another copy of the PowerPlay early power estimator. You can also enter the 10 design modules that use the most resources for an estimation.

Estimating Power

You can estimate power at any point in your design cycle. You can use the PowerPlay early power estimator to estimate the power consumption if you have not begun your design, or if your design is not complete. After completing your design, you can use the simulation-based power estimation feature in Quartus II software or the PowerPlay early power estimator to estimate the power consumption.

For more information on the simulation-based power estimation feature in Quartus II software, refer to the *PowerPlay Early Power Estimator* chapter in the *Quartus II Handbook*.

To use the PowerPlay early power estimator, enter the device resources, operating frequency, toggle rates and other parameters in the PowerPlay early power estimator. If you do not have an existing design, then you must estimate the number of device resources your design uses in order to enter the information into the PowerPlay early power estimator.

Estimating Power Before Starting the FPGA Design

FPGAs provide the convenience of a shorter design cycle and faster time-to-market than ASICs or ASSPs. This means that the board design often takes places during the FPGA design cycle, and the power planning for the device can happen before any of the FPGA design is complete.

Table 2–1 shows the advantages and disadvantages to using the PowerPlay early power estimator before you begin the FPGA design.

Table 2–1. Power Estimation Before FPGA Design Has Begun

Advantages	Disadvantages
Power estimation can be done before any FPGA design is complete	• Accuracy depends on user input and estimate of the device resources • Process can be time consuming

To estimate power usage with the PowerPlay early power estimator if you have not started your FPGA design, perform the following steps:

1. Download the PowerPlay early power estimator from the Altera web site (**www.altera.com**).
2. Select the target device and package from the PowerPlay early power estimator **Device** section.
3. Enter in the requested values for any relevant power consumption section and clock domain. I_{CC} and P values are calculated automatically, and an I_{CC} and P subtotal are given for each section.
4. The PowerPlay early power estimator displays the estimated power usage in the **Total** section.

Estimating Power While Creating the FPGA Design

When the FPGA design is partially complete, you can use the power estimation file (<*project name*>**_pwr_cal.txt**) generated by the Quartus II software to supply information to the PowerPlay early power estimator. After using the Import Data macro to import the power estimation file information into the PowerPlay early power estimator, you can edit the PowerPlay early power estimator to reflect the device resource estimates for the final design.

For more information on generating the power estimation file in the Quartus II software, refer to the *PowerPlay Early Power Estimation* chapter in the *Quartus II Handbook*.

Table 2–2 shows the advantages and disadvantages when using the PowerPlay early power estimator and the FPGA design is partially complete.

Table 2–2. Power Estimation When FPGA Design Is Partially Complete

Advantages	Disadvantages
Accuracy is dependent on user input and estimate of the final design device resources	• Power estimation can be done early in the FPGA design cycle • Provides the flexibility to automatically fill in the PowerPlay early power estimator based on Quartus II software compilation results

Use the following steps to estimate power usage with the PowerPlay early power estimator if your FPGA design is partially complete:

1. Compile the partial FPGA design in the Quartus II software.
2. Generate the power estimation file (<*project name*>**_pwr_cal.txt**) in the Quartus II software by clicking **Generate Power Estimation File** (Project menu).
3. Download the PowerPlay early power estimator from the Altera website (**www.altera.com**).
4. Run the Import Data macro in the PowerPlay early power estimator to automatically populate the PowerPlay early power estimator entries.
5. After running the Import Data macro to populate the PowerPlay early power estimator, you can manually edit the cells to reflect final device resource estimates.

Estimating Power After Completing the FPGA Design

When you complete your FPGA design, estimate the device power consumption using the simulation-based power estimation feature in the Quartus II software. The Quartus II Simulator supports simulation-based power estimation for Stratix, Stratix GX, Cyclone, MAX® 7000AE, MAX 7000B, and MAX 3000A devices.

Table 2–3 shows the advantages and disadvantages when using the simulation-based power estimation feature in Quartus II software when the FPGA design is complete.

Table 2–3. Power Estimation When FPGA Design Is Complete

Advantages	Disadvantages
Provides the most accurate power estimation since the simulation stimuli reflects actual device behavior	Power estimation done later in the FPGA design cycle

For more information on the simulation-based power estimation feature in Quartus II software, refer to the *PowerPlay Early Power Estimator* chapter in the *Quartus II Handbook*.

Altera strongly recommends that you run the PowerPlay early power estimator after your FPGA design is completed.

3. Using PowerPlay Early Power Estimator for Stratix, Stratix GX & Cyclone FPGAs

PowerPlay Early Power Estimator Input Values

The sections in the PowerPlay early power estimator that estimate I_{CC} and power represent an architectural feature of the device, such as the clocktree network, RAM blocks, or digital signal processing (DSP) blocks. The sub-total of the I_{CC} and power consumed by each architectural feature is reported in each section in milli-Amps (mA) and milli-Watts (mW).

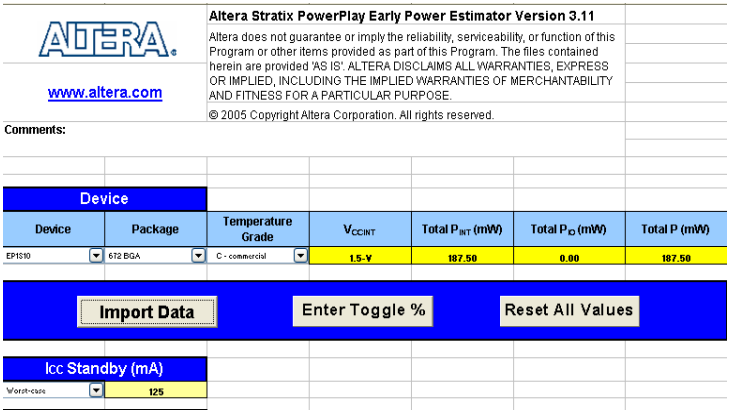
The following sections of this user guide explain what values you need to enter for each section of the PowerPlay early power estimator. Sections in the PowerPlay early power estimator calculate power representing architectural features of the device, such as clocks, RAM blocks, or DSP blocks. Each section also provides an example of how you would enter the relevant information into the PowerPlay early power estimator.

Device

Different Stratix®, Stratix GX, or Cyclone™ devices consume different amounts of power for the same design in a similar condition. The larger the device, the more power it consumes because of the larger die and longer interconnects in the device.

In the **Device** section of the PowerPlay early power estimator, select the target device with the corresponding package and temperature grade used in your design (Figure 3–1). The total power for both the logic array and I/O pins are reported in this section.

Figure 3–1. Stratix PowerPlay Early Power Estimator Device & I_{CC} Standby Section



I_{CC} Standby

I_{CC} standby is the current consumed by the device after it is configured, with no signals driving it and no interconnects toggling. The **I_{CC} Standby** section of the PowerPlay early power estimator has both a typical and worst-case value for each device (see Figure 3–2). The typical value is for a typical process at 25° C. The worst-case value is for a fast process at 85° C.

Do not use the worst-case value as a maximum specification, only as a guideline. Your device's actual I_{CC} standby may vary from what the PowerPlay early power estimator reports.

Clock Network Information

Stratix and Stratix GX devices feature three types of clock networks: global, regional, and fast regional. The **Clock Network** section in the Stratix and Stratix GX PowerPlay early power estimator is divided into these three sections:

- Stratix and Stratix GX devices feature 16 dedicated global clock networks
- 16 regional clock networks (four per device quadrant)
- 8 dedicated fast regional clock networks (at least two per device quadrant)

The Stratix and Stratix GX PowerPlay early power estimator reflect the actual clock resources in the device by providing 16 rows for the global clock network, 16 rows for the regional clock network, and 8 rows for the fast regional clock network.

Cyclone devices have eight global clock networks. They do not have regional clock or fast regional clock networks.

Each row in the **Clock Network** section represents a clock network or a separate clock domain. For each clock network used, you need to enter the clock frequency (f_{MAX}) in MHz and the number of flip-flops fed by the clock. Table 3–1 describes the values that are entered in the **Clock Network** section of the PowerPlay early power estimator.

Table 3–1. Clock Network Section Information (Part 1 of 2)

Column Heading	Description
Clock Network	Enter a name for the clock network in this column. This is an optional value.
f_{MAX} (MHz)	Enter the clock frequency for the clock network. This value is limited by the maximum frequency specification for the device family.
# Flip-Flops	Enter the number of registers driven by the clock network. The number of flip-flops driven by every global clock, regional clock, and fast regional clock signal is reported in the Fan-out column of the Quartus II Compilation Report under **Fitter** > **Resource Section** > **Global & Other Fast Signals** > **Fan-out**. This value is limited by the number of logic elements (LEs) available in the largest device in the family. You should verify that the number of flip-flops entered does not exceed the number of LEs available in your target device because the PowerPlay early power estimator does not verify this.
# DSP Blocks	Enter the number of DSP blocks driven by the clock network. The number of DSP blocks driven by every global clock, regional clock, and fast regional clock signal is reported in the Fan-out column of the Quartus II Compilation Report under **Fitter** > **Resource Section** > **Global & Other Fast Signals** > **Fan-out**. *(1)*
# M512 Blocks	Enter the number of M512 blocks driven by the clock network. The number of M512 blocks is driven by every global clock, regional clock, and fast regional clock signal is reported in the Fan-out column of the Quartus II Compilation Report under **Fitter** > **Resource Section** > **Global & Other Fast Signals** > **Fan-out**. *(1)*
# M4K Blocks	Enter the number of M4K blocks driven by the clock network. The number of M4K blocks is driven by every global clock, regional clock, and fast regional clock signal is reported in the Fan-out column of the Quartus II Compilation Report under **Fitter** > **Resource Section** > **Global & Other Fast Signals** > **Fan-out**. *(1)*
MRAM Blocks	Enter the number of MRAM blocks driven by the clock network. The number of MRAM blocks is driven by every global clock, regional clock, and fast regional clock signal is reported in the Fan-out column of the Quartus II Compilation Report under **Fitter** > **Resource Section** > **Global & Other Fast Signals** > **Fan-out.** *(1)*
I_{CCINT} (mA)	This shows the estimated I_{CCINT}, in mA, based on the f_{MAX} and number of flip-flops you entered. This value is estimated automatically.

Table 3–1. Clock Network Section Information (Part 2 of 2)	
Column Heading	**Description**
P_{INT} (mW)	This shows the estimated P_{INT}, in mW, based on the f_{MAX} and number of flip-flops you entered. This value is estimated automatically.

Note to Table 3–1:

(1) This value is limited by the number of blocks (DSP, M4K, M512, or MRAM) available in the largest device in the family. You should verify that the number of (DSP, M4K, M512, or MRAM) blocks entered does not exceed the number of (DSP, M4K, M512, or MRAM) blocks available in your target device because the PowerPlay early power estimator does not verify this.

Figure 3–2 shows a screen shot of the **Global & Other Fast Signals** report from the Quartus II software Compilation Report. The report shows fan-out for each signal that uses a global clock. The **Timing Analysis** section of the Compilation Report lists the clock signal frequencies. Enter the appropriate information from the Compilation Report into the PowerPlay early power estimator. Figure 3–3 shows the Stratix device PowerPlay early power estimator and the estimated power consumed by the global clock, regional clock, and fast regional clock networks for this design.

Figure 3–2. Global & Other Fast Signals Resource Section in Compilation Report

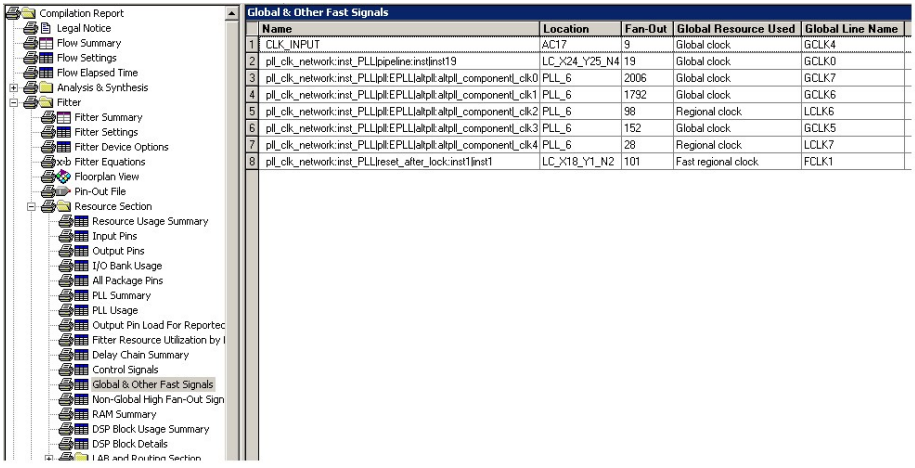


Figure 3–3. Clock Network Section in the Stratix & Stratix GX PowerPlay Early Power Estimator

Clock Network								
Global Clock Network	f_{MAX} (MHz)	# Flipflops	# DSP Blocks	# M512 Blocks	# M4K Blocks	# M-RAM Blocks	I_{CCINT} (mA)	P_{INT} (mW)
1	100	12500	0	0	0	0	243.09	364.64
2	250	0	10	0	0	0	87.19	130.79
3	175	0	0	0	20	0	45.50	68.25
4	308	0	0	80	0	0	295.68	443.52
5	150	0	0	0	0	6	9.00	13.50
						Subtotal	680.47	1020.70
Regional Clock Network	f_{MAX} (MHz)	# Flipflops	# DSP Blocks	# M512 Blocks	# M4K Blocks	# M-RAM Blocks	I_{CCINT} (mA)	P_{INT} (mW)
1	75	10000	0	0	0	0	107.19	160.79
2	225	0	4	0	0	0	35.06	52.58
3	200	0	0	100	0	0	240.00	360.00
4	150	0	0	0	50	0	97.50	146.25
5	300	0	0	0	0	6	18.00	27.00
						Subtotal	497.75	746.63
Fast Regional Clock Network	f_{MAX} (MHz)	# Flipflops	# DSP Blocks	# M512 Blocks	# M4K Blocks	# M-RAM Blocks	I_{CCINT} (mA)	P_{INT} (mW)
1	100	5000	0	0	0	0	101.32	151.98
2	150	0	6	0	0	0	33.83	50.75
3	125	0	0	9	0	0	13.50	20.25
4	80	0	0	0	2	0	2.08	3.12
5	200	0	0	0	0	1	2.00	3.00
						Subtotal	150.73	226.10

Figure 3–4. Clock Network Section in the Cyclone PowerPlay Early Power Estimator

Clock Network					
Global Clock Network	f_{MAX} (MHz)	# Flipflops	# M4K Blocks	I_{CCINT} (mA)	P_{INT} (mW)
1	145	12500	0	271.12	406.69
2	250	0	20	42.52	63.79
3	100	0	15	12.77	19.16
4	80	5000	0	71.89	107.84
5	0	0	0	0.00	0.00
6	0	0	0	0.00	0.00
7	0	0	0	0.00	0.00
8	0	0	0	0.00	0.00
			Subtotal	398.32	597.47

Logic Elements

A design can be considered a combination of several design modules operating at different frequencies and toggle rates. Each design module can have a different amount of LEs with and without carry-chains. For the most accurate power estimation, partition the design into different design modules. You can partition your design by grouping modules by clock frequency, location, hierarchy, or entities.

Each row in the LEs section represents a separate design module. For each design module, you need to enter the clock frequency (f_{MAX}) in MHz, the number of LEs fed by this clock, the number of LEs that use carry chains fed by this clock, and the toggle percentage.

Table 3–2 describes the values that are entered in the LEs section of the PowerPlay early power estimator.

Table 3–2. Logic Elements (LEs) Section Information

Column Heading	Description
Design Module	Enter a name for the design module in this column. This is an optional value.
f_{MAX} (MHz)	This is the frequency of the clock feeding the LEs. This value is limited by the maximum frequency specification for the device family. If you have asynchronous logic that is not fed by a clock or is combinational logic, you should consider this as a design module. Estimate how often this logic toggles based on your design. Using this information, enter an appropriate clock frequency and toggle percentage.
Average Fan-Out	The average fan-out per LE of your design. The Quartus II reports this information in the **Average Fan-Out** row in the **Fitter** > **Resource Section** > **Fitter Resource Usage Summary** section of the Compilation Report. The average fan-out usually ranges from 1 to 5 with a design average of 3.4.
# LEs	The number of LEs used in the whole design is reported in the Quartus II software in the Logic Cells row in the **Fitter** > **Resource Section** > **Fitter Resource Usage Summary** section of the Compilation Report. The number of LEs used in each design entity is found in the **Fitter Resource Utilization by Entity** section of the Compilation Report or the **Hierarchies** tab of the **Project Navigator**. *(1)*
# LEs w/carry	The number of LEs in the design module that use carry chains. The Quartus II software reports the number of LEs using carry chains in the **Logic Cells in Carry Chains** row in the under **Fitter** > **Resource Section** > **Fitter Resource Usage Summary** section of the Compilation Report. *(1)*
Toggle %	The average percentage of LEs toggling on each clock cycle. The toggle percentage ranges from 0 to 100%. Typically, the toggle percentage is 12.5%, which is the toggle percentage of a 16-bit counter. To be more conservative, you can use a higher toggle percentage. For instance, a TFF with its input tied to V_{CC} has a toggle rate of 100% because its output is changing logic states on every clock cycle. Figure 3–5 for an example. Figure 3–6 shows an example of a 4-bit counter. The first TFF with least significant bit (LSB) output `cout0` has a toggle rate of 100% because `cout0` toggles on every clock cycle. The toggle rate for the second TFF with output `cout1` is 50% since `cout1` only toggles on every two clock cycles. Consequently, the toggle rate for the third TFF with output `cout2` and fourth TFF with output `cout3` are 25% and 12.5%, respectively. Therefore, the average toggle percentage for this 4-bit counter is (100 + 50 + 25 + 12.5)/4 = 46.875%.

Notes to Table 3–2:

(1) This value is limited by the largest number of LEs available in the largest device in the family. You must verify that the number of LEs entered does not exceed the number of LEs available in your target device.

Figure 3–5. TFF Example

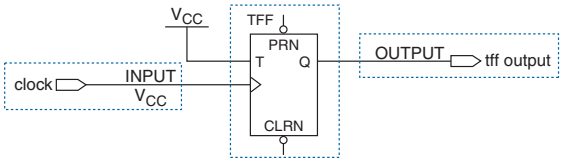


Figure 3–6. 4-Bit Counter Example

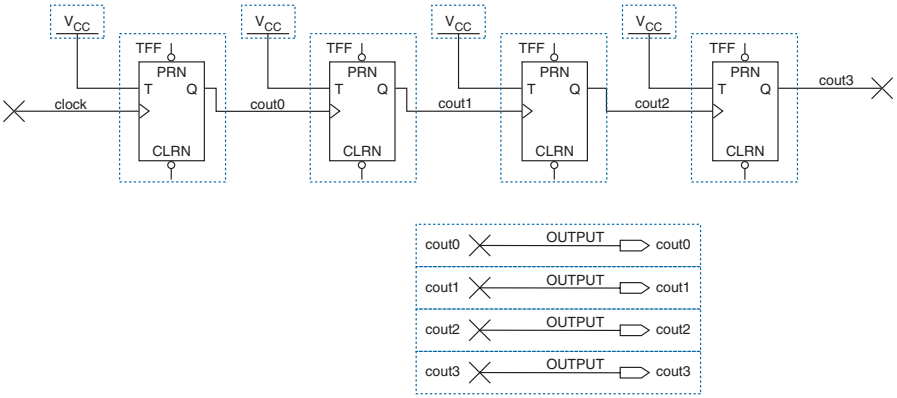
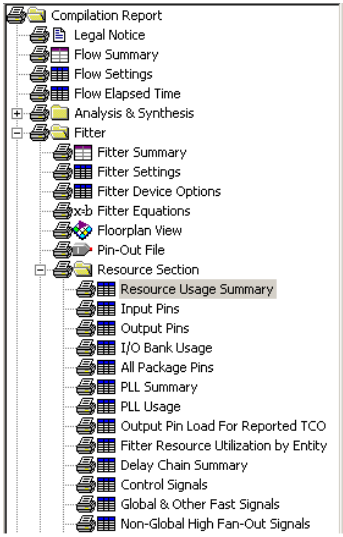


Figure 3–7 shows the **Resource Usage Summary** in the Quartus II software Compilation Report for a design targeting the Stratix device family. The Compilation Report provides the total number of LEs used by the design and the average fan-out. You can view the **Fitter Resource Utilization by Entity** section of the Compilation Report or use the **Hierarchies** tab of the **Project Navigator** to determine how many LEs are in each entity. Using this information from the Compilation Report, you can enter in the appropriate information into the PowerPlay early power estimator. Figure 3–8 shows the Stratix device PowerPlay early power estimator and the estimated power consumed by the LEs in this design.

Figure 3–7. Resource Usage Summary in Compilation Report



Resource Usage Summary

	Resource	Usage
1	Logic cells	5,811 / 25,660 (22 %)
2	Registers	3,847 / 29,162 (13 %)
3	User inserted logic cells	0
4	I/O pins	14 / 597 (2 %)
5	-- Clock pins	1 / 16 (6 %)
6	Global signals	8
7	M512s	141 / 224 (62 %)
8	M4Ks	65 / 138 (47 %)
9	M-RAMs	2 / 2 (100 %)
10	Total memory bits	835,488 / 1,944,576 (42 %)
11	Total RAM block bits	1,560,384 / 1,944,576 (80 %)
12	DSP block 9-bit elements	32 / 80 (40 %)
13	Global clocks	5 / 16 (31 %)
14	Regional clocks	2 / 16 (12 %)
15	Fast regional clocks	1 / 8 (12 %)
16	DIFFIOCLKs	0 / 16 (0 %)
17	SERDES transmitters	0 / 78 (0 %)
18	SERDES receivers	0 / 78 (0 %)
19	Maximum fan-out node	pll_clk_network:inst_PLL|pll:EPLL|altpll:altpll_component|_clk0
20	Maximum fan-out	4054
21	Total fan-out	25216
22	Average fan-out	4.16

Figure 3–8. Logic Elements (LEs) Section in the Stratix PowerPlay Early Power Estimator

Logic Elements (LEs)

Average Fan-out

4.16

Design Module	fMAX (MHz)	# LEs	# LEs w/Carry	Toggle %	ICCINT (mA)	PINT (mW)
1	250	2500	2000	12.50	**86.06**	**129.08**
2	100	1700	1400	12.50	**23.53**	**35.30**
3	50	500	400	12.50	**3.44**	**5.16**
4	20	511	421	12.50	**1.41**	**2.12**
5	10	600	450	12.50	**0.82**	**1.23**
6	0	0	0	0.00	**0.00**	**0.00**
7	0	0	0	0.00	**0.00**	**0.00**
8	0	0	0	0.00	**0.00**	**0.00**
9	0	0	0	0.00	**0.00**	**0.00**
10	0	0	0	0.00	**0.00**	**0.00**
				Subtotal	**115.26**	**172.89**

Digital Signal Processing Blocks

The **Digital Signal Processing (DSP)** section is only found in the Stratix and Stratix GX PowerPlay early power estimator. Stratix and Stratix GX devices have dedicated DSP blocks, which have high-speed parallel processing capabilities that are optimized for DSP applications. DSP blocks are ideal for implementing DSP applications that need high data throughput.

Each row in the **Digital Signal Processing (DSP) Blocks** section represents a DSP design module where the DSP block(s) have the same frequency, number of data outputs, and toggle percentage. If some (or all) DSP blocks in your design have different configurations, you need to enter the information in different rows. For each DSP module, you need to enter the clock frequency (f_{MAX}) in MHz, the number of data outputs per DSP block, the toggle percentage of the data outputs, and the number of DSP blocks with this configuration. Table 3–3 describes the values that are entered in the **Digital Signal Processing (DSP) Blocks** section of the PowerPlay early power estimator.

Table 3–3. Digital Signal Processing (DSP) Blocks Section Information

Column Heading	Description
DSP Module	In this column, you can enter a name for the DSP module. This is an optional value.
f_{MAX} (MHz)	The frequency of the clock feeding the DSP blocks. The maximum clock frequency for DSP blocks is 340 MHz.
# Data Outputs	The number of outputs per DSP block. The number of outputs per DSP block are found in the Quartus II software timing closure floorplan. This number must be an integer value from 0 to 144.
Toggle %	The average percentage of DSP data outputs toggling on each clock cycle. The toggle percentage ranges from 0 to 100%. Typically, the toggle percentage is 12.5%. To be more conservative, you can use a higher toggle percentage.
# DSP blocks	The number of DSP blocks that are configured with the same clock frequency, data outputs, and toggle percentage. This value is limited by the number of DSP blocks available in the largest device in the family. You need to verify that the number of DSP blocks entered does not exceed the number of DSP blocks available in your target device because the PowerPlay early power estimator does not verify this.

Figure 3–9 shows the Stratix device PowerPlay early power estimator and the estimated power consumed by the DSP blocks for a design targeting a Stratix device that uses two DSP blocks clocked by a 250-MHz clock in 36 × 36 mode with a 12.5% toggle rate for the data outputs.

Figure 3–9. Digital Signal Processing Blocks Section in the Stratix PowerPlay Early Power Estimator

Digital Signal Processing (DSP) Blocks

DSP Module	fMAX (MHz)	# Data Outputs	Toggle %	# DSP blocks	ICCINT (mA)	PINT (mW)
1	250	72	12.50	2	32.74	49.10

Phase-Locked Loops

Stratix and Stratix GX devices have two types of phase-locked loops (PLLs): enhanced PLLs and fast PLLs. The **Phase-Locked Loops (PLLs)** section in the Stratix and Stratix GX PowerPlay early power estimator is divided into two sections. Cyclone devices have fast PLLs only.

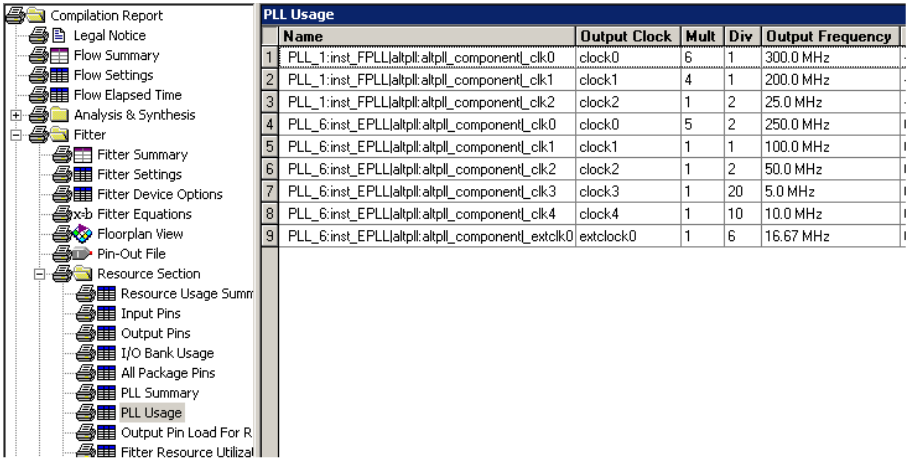
Each row in the PLLs section represents a PLL in the device. For each enhanced PLL or fast PLL used, you need to enter the maximum output clock frequency for that PLL. Table 3–4 describes the values that are entered in the **Phase-Locked Loops (PLLs)** section of the PowerPlay early power estimator.

Table 3–4. Phase-Locked Loops (PLLs) Section Information

Column Heading	Description
PLLs	Enter a name for the PLL in this column. This is an optional value.
f_{MAX} (MHz)	The maximum PLL clock output frequency for this PLL. This value is limited by the maximum PLL output clock frequency specification for the device family.

Figure 3–10 shows an example of the **PLL Usage** summary in the Quartus II software Compilation Report for a design targeting a Stratix device. The Compilation Report provides the output frequency for each PLL clock output. You only need to enter in the maximum output frequency for that PLL into the PowerPlay early power estimator. Figure 3–11 shows the Stratix device PowerPlay early power estimator and the estimated power consumed by the enhanced PLL and the fast PLL used in this example.

Figure 3–10. Phase-Locked Loops (PLLs) Usage in Compilation Report



PLL Usage

	Name	Output Clock	Mult	Div	Output Frequency
1	PLL_1:inst_FPLL|altpll:altpll_component|_clk0	clock0	6	1	300.0 MHz
2	PLL_1:inst_FPLL|altpll:altpll_component|_clk1	clock1	4	1	200.0 MHz
3	PLL_1:inst_FPLL|altpll:altpll_component|_clk2	clock2	1	2	25.0 MHz
4	PLL_6:inst_EPLL|altpll:altpll_component|_clk0	clock0	5	2	250.0 MHz
5	PLL_6:inst_EPLL|altpll:altpll_component|_clk1	clock1	1	1	100.0 MHz
6	PLL_6:inst_EPLL|altpll:altpll_component|_clk2	clock2	1	2	50.0 MHz
7	PLL_6:inst_EPLL|altpll:altpll_component|_clk3	clock3	1	20	5.0 MHz
8	PLL_6:inst_EPLL|altpll:altpll_component|_clk4	clock4	1	10	10.0 MHz
9	PLL_6:inst_EPLL|altpll:altpll_component|_extclk0	extclock0	1	6	16.67 MHz

Figure 3–11. Phase-Locked Loops (PLLs) Section in the Stratix PowerPlay Early Power Estimator

Phase-Locked Loops (PLLs)

Enhanced PLLs	fMAX (MHz)	ICCINT (mA)	PINT (mW)
1	250	98.49	147.73
2	0	0.00	0.00
3	0	0.00	0.00
4	0	0.00	0.00
	Subtotal	98.49	147.73

Fast PLLs	fMAX (MHz)	ICCINT (mA)	PINT (mW)
1	300	59.71	89.57
2	0	0.00	0.00
3	0	0.00	0.00
4	0	0.00	0.00
5	0	0.00	0.00
6	0	0.00	0.00
7	0	0.00	0.00
8	0	0.00	0.00
	Subtotal	59.71	89.57

RAM Blocks

Stratix and Stratix GX device TriMatrix™ memory consists of three types of RAM blocks:

- M512 blocks

- M4K blocks
- M-RAM blocks

Since the power consumption for each type of RAM blocks is different, the **RAM Blocks** section in the Stratix or Stratix GX PowerPlay early power estimator is divided into three parts. Cyclone devices only contain M4K RAM blocks.

Each row in the **RAM Block** section represents a design module where the RAM block(s) have the same frequency, number of data inputs and outputs, toggle percentage and mode. If some (or all) of the RAM blocks in your design have different configurations, enter the information in different rows. For each design module, you need to enter the clock frequency (f_{MAX}) in MHz, the number of data inputs and outputs per RAM block, the toggle percentage of the data inputs and outputs, the number of RAM blocks with this configuration, and the mode of each RAM block.

Table 3–5. RAM Blocks Section Information (Part 1 of 2)

Column Heading	Description
Design Module	Enter a name for the design module in this column. This is an optional value.
f_{MAX} (MHz)	Enter the frequency of the clock feeding the RAM blocks. If two clocks running at different frequencies are feeding the RAM block, enter in the higher of the two frequencies. This value is limited by the maximum frequency specification for each type of RAM block.
# Data Inputs	Enter the number of data inputs per RAM block. If your design consists of many RAM blocks with different numbers of inputs, you can divide your design into a few design modules with the same number of inputs. You can find the number of outputs per RAM block in the timing closure floorplan in the Quartus II software. This value is limited by the maximum number of inputs available for each type of RAM block.
# Data Outputs	Enter the number of data outputs per RAM block. If your design consists of many RAM blocks with different numbers of outputs, you can divide your design into a few design modules with the same number of outputs. You can find the number of outputs per RAM block in the timing closure floorplan in the Quartus II software. This value is limited by the maximum number of outputs available for each type of RAM block.
Address Width	Enter the number of address width per RAM block. If your design consists of many RAM blocks with different numbers of address width, you can divide your design into a few design modules with the same number of address width. You can find the number of address width per RAM block in the timing closure floorplan in the Quartus II software. This value is limited by the maximum number of address width available for each type of RAM block.
Toggle %	Enter the average percentage of RAM data inputs and outputs toggling on each clock cycle. The toggle percentage ranges from 0 to 100%. Typically, the toggle percentage is 12.5%. To be more conservative, you can use a higher toggle percentage.

Table 3–5. RAM Blocks Section Information (Part 2 of 2)

Column Heading	Description
Clock Enable %	Enter the average percentage of RAM clock enabled. The toggle percentage ranges from 0 to 100%. Typically, the toggle percentage is 100%.
# <*type of RAM*> Blocks	Enter the number of M512, M4K or M-RAM blocks that are configured with the same clock frequency, data inputs and outputs, toggle percentage and mode. This value is limited by the number of RAM blocks available in the largest device in the family. Verify that the number of RAM blocks entered does not exceed the number of RAM blocks available in your target device. The PowerPlay early power estimator does not verify this.

Figure 3–12 shows the Stratix device PowerPlay early power estimator and the estimated power consumed by the RAM blocks for a design targeting a Stratix device.

Figure 3–12. RAM Blocks Section in the Stratix PowerPlay Early Power Estimator

RAM Blocks

M512 Blocks

Design Module	f_{MAX} (MHz)	# Data Inputs	# Data Outputs	Address Width	Toggle %	Clock Enable %	# M512 Blocks	I_{CCINT} (mA)	P_{INT} (mW)
1	100	18	18	5	50	100	15	95.91	143.87
2	250	9	9	10	50	100	10	101.60	152.40
							Subtotal	197.51	296.26

M4K Blocks

Design Module	f_{MAX} (MHz)	# Data Inputs	# Data Outputs	Address Width	Toggle %	Clock Enable %	# M4K Blocks	I_{CCINT} (mA)	P_{INT} (mW)
1	175	36	36	7	50	100	20	451.57	677.35
2	200	9	9	13	50	100	15	201.36	302.04
							Subtotal	652.92	979.39

M-RAM Blocks

Design Module	f_{MAX} (MHz)	# Data Inputs	# Data Outputs	Address Width	Toggle %	Clock Enable %	# M-RAM Blocks	I_{CCINT} (mA)	P_{INT} (mW)
1	100	144	144	7	50	100	4	620.11	930.16
2	260	72	72	13	50	100	2	532.40	798.61
							Subtotal	1152.51	1728.77

HSDI

The **HSDI** section is only found in the Stratix device PowerPlay early power estimator. Stratix devices contain dedicated circuitry that supports interfacing with high-speed differential I/O standards at speeds up to 840 megabits per second (Mbps). Stratix devices support the HyperTransport technology, LVDS, LVPECL, and 3.3-V PCML differential I/O standards. The **HSDI** section in the Stratix device PowerPlay early power estimator is divided into two parts: Receiver and Transmitter.

Each row in the **HSDI** section represents a separate receiver or transmitter domain. For each transmitter domain used, you need to enter the data rate (in Mbps), the number of channels in that transmitter

domain, the toggle percentage of the serializer outputs, and the I/O standard used on the output pins. Table 3–6 describes the values that are entered in the HSDI section of the PowerPlay early power estimator.

Table 3–6. HSDI Section Information

Column Heading	Description
Domain	Enter a name for the receiver or transmitter domain in this column. This is an optional value.
Data Rate (Mbps)	Enter the maximum data rate in Mbps of the receiver or transmitter channels for each receiver and transmitter domain. Stratix device SERDES circuitry can transmit and receive data up to 840 Mbps per channel. Therefore, the data rate must be a decimal number from 0 to 840 Mbps.
# of Channels	Enter the number of receiver and transmitter channels running at the above data rate. Since each fast PLL in Stratix devices can support up to 20 high-speed differential channels, this number must be an integer value from 0 to 20.
VCCIO	Select the V_{CCIO} used by the receiver channels from the list. The V_{CCIO} available for the receiver channels are 2.5 V and 3.3 V.
Toggle %	Enter the average percentage of serializer outputs toggling at each high-speed clock cycle. The toggle % ranges from 0 to 100%. Typically, the toggle % is 25%. To be more conservative, you can use a higher toggle percentage.
I/O Standard	Select the differential I/O standards used by the transmitter channels from the list. The differential I/O standards available for the transmitter channels are HyperTransport technology, LVDS, LVPECL, and 3.3-V PCML.

Figure 3–13 shows the Stratix PowerPlay early power estimator and the estimated power consumed by the HSDI for a design targeting a Stratix device that has 20 LVDS receiver and transmitter channels operating at 840 Mbps with data outputs toggling at 25%.

The power of the receiver and transmitter PLLs used by the SERDES is included in the HSDI section. Therefore, you do not need to estimate the receiver and transmitter PLL power in the PLL section.

Figure 3–13. HSDI Section in the Stratix PowerPlay Early Power Estimator

High-Speed Digital Interface (HSDI)								
Receiver								
Rx Domain	Data Rate (Mbps)	# of Channels	V_{CCIO}	I_{CCINT} (mA)	I_{CCIO} (mA)	P_{INT} (mW)	P_{IO} (mW)	
1	840	20	3.3	170.90	4.00	256.34	13.20	
2	0	0	2.5	0.00	0.00	0.00	0.00	
3	0	0	2.5	0.00	0.00	0.00	0.00	
4	0	0	2.5	0.00	0.00	0.00	0.00	
			Subtotal	170.90	4.00	256.34	13.20	
Transmitter								
Tx Domain	Data Rate (Mbps)	# of Channels	Toggle %	I/O Standard	I_{CCINT} (mA)	I_{CCIO} (mA)	P_{INT} (mW)	P_{IO} (mW)
1	840	20	25.00	LVDS	232.59	143.07	348.88	472.12
2	0	0	12.50	LVDS	0.00	0.00	0.00	0.00
3	0	0	12.50	LVDS	0.00	0.00	0.00	0.00
4	0	0	12.50	HyperTransport™	0.00	0.00	0.00	0.00
				Subtotal	232.59	143.07	348.88	472.12

Dedicated Source-Synchronous Circuitry

The **Dedicated Source-Synchronous Circuitry** section is only found in the Stratix GX device PowerPlay early power estimator. The dedicated source-synchronous circuitry in Stratix GX devices support a source-synchronous high-speed interface and differential data rates up to 1 gigabit per second (Gbps). Stratix GX devices support the HyperTransport technology, LVDS, LVPECL, and 3.3 V PCML differential I/O standards. Each Stratix GX receiver channel features a dynamic phase alignment (DPA) block. If you are using the DPA feature, choose DPA **On**: If you are not using the DPA feature, choose **Bypass** from the DPA **On**/**Bypass** drop-down menu. The dedicated source-synchronous circuitry section in the Stratix GX PowerPlay early power estimator is divided into two parts; Receiver and Transmitter.

Each row represents a separate receiver or transmitter domain. For each receiver domain used, you need to enter the data rate (Mbps), the number of channels in that receiver domain, and if DPA is on or bypassed. For each transmitter domain used, you need to enter the data rate (Mbps), the number of channels in that transmitter domain, the toggle percentage of

the serializer outputs, and the I/O standard used on the output pins. Table 3–7 describes the values that are entered in the dedicated source-synchronous circuitry section of the PowerPlay early power estimator.

Table 3–7. Dedicated Source-Synchronous Circuitry Section Information

Column Heading	Description
Domain	Enter a name for the receiver or transmitter domain in this column. This is an optional value.
Data Rate (Mbps)	Enter the maximum data rate in Mbps of the receiver or transmitter channels for every receiver and transmitter domain. If the design bypasses the DPA circuitry, Stratix GX SERDES circuitry can receive data at rates up to 840 Mbps. If the design uses DPA circuitry, Stratix GX SERDES circuitry can receive data at rates up to 1,000 Mbps (1 Gbps). Stratix GX SERDES circuitry can transmit data up to 1,000 Mbps (1 Gbps). Therefore, the data rate must be a decimal number from 0 to 1,000 Mbps.
# of Channels	Enter the number of receiver and transmitter channels running at the specified data rate. For transmitters and receivers with DPA bypassed, each fast PLL in Stratix GX devices can support up to 20 high-speed differential channels. For receivers with DPA on, the number of receiver channels can be up to 23. Therefore, the receiver number of channels must be an integer value from 0 to 23, while the number of transmitter channels must be an integer value from 0 to 20.
DPA On/Bypass	Choose On from the DPA **On/Bypass** drop-down menu if you are using the DPA feature; Choose **Bypass** from the DPA **On/Bypass** drop-down menu if you are not using the DPA feature.
Toggle %	Enter the toggle %, which is the average percentage of serializer outputs toggling at each high speed clock cycle. The toggle % ranges from 0 to 100%. Typically, the toggle % is 25%. To be more conservative, you can use a higher toggle percentage.
I/O Standard	Select the differential I/O standards used by the transmitter channels from the list. The differential I/O standards available for the transmitter channels are HyperTransport technology, LVDS, LVPECL, and 3.3-V PCML.

Figure 3–14 shows the Stratix GX PowerPlay early power estimator and the estimated power consumed by the dedicated source-synchronous circuitry for a design targeting a Stratix GX device that has 10 LVDS receiver (with DPA on) and transmitter channels operating at 1 Gbps with data output toggling at 25%.

The power of the receiver and transmitter PLLs used by the dedicated source synchronous circuitry is included in the dedicated source-synchronous circuitry section. You do not need to estimate the receiver and transmitter PLL power in the PLL section.

Figure 3–14. Dedicated Source-Synchronous Circuitry Section in the Stratix GX PowerPlay Early Power Estimator

Dedicated Source-Synchronous Circuitry								
Receiver								
Rx Domain	Data Rate (Mbps)	# of Channels	DPA On/Bypass	I_{CCINT} (mA)	I_{CCIO} (mA)	P_{INT} (mW)	P_{IO} (mW)	
1	1000	10	On	459.50	4.00	689.25	13.20	
2	0	0	Bypass	0.00	0.00	0.00	0.00	
3	0	0	On	0.00	0.00	0.00	0.00	
4	0	0	Bypass	0.00	0.00	0.00	0.00	
			Subtotal	459.50	4.00	689.25	13.20	
Transmitter								
Tx Domain	Data Rate (Mbps)	# of Channels	Toggle %	I/O Standard	I_{CCINT} (mA)	I_{CCIO} (mA)	P_{INT} (mW)	P_{IO} (mW)
1	1000	10	25.00	LVDS	261.70	107.75	392.55	355.56
2	0	0	0.00	LVPECL	0.00	0.00	0.00	0.00
3	0	0	0.00	PCML	0.00	0.00	0.00	0.00
4	0	0	0.00	HyperTransport	0.00	0.00	0.00	0.00
				Subtotal	261.70	107.75	392.55	355.56

General I/O Power

Stratix, Stratix GX, and Cyclone devices feature programmable I/O pins that support a wide range of industry I/O standards, permitting increased design flexibility. The **General I/O Power** section in the PowerPlay early power estimator enables you to estimate the I/O pin power consumption based on their I/O standards.

For I/O standards that recommend termination resistors (for example, SSTL and HSTL), the PowerPlay early power estimator assumes you are using external termination resistors.

The I_{CC} and power reported is for external termination. If you are not using external termination resistors, you should choose the LVTTL I/O standard with the same V_{CCIO} and similar drive strength as the terminated I/O standard. For example, if you are using SSTL-2 class II and are only doing a point-to-point connection and are not using termination resistors, you should select **2.5_LVTTL/LVCMOS_16** as your I/O standard.

The current consumed by the V_{REF} pins is minimal (less than 10 µA). Therefore, this information is not included in the PowerPlay early power estimator, since it s negligible when compared to the power consumed by the general-purpose I/O pins.

Each row in the **General I/O Power** section represents a design module where the I/O pins have the same frequency, toggle percentage, average capacitive load, I/O standard, and data rate. Enter the clock frequency (f_{MAX}) in MHz, the number of output and bidirectional pins with this configuration, toggle percentage of the pins, the average capacitance of

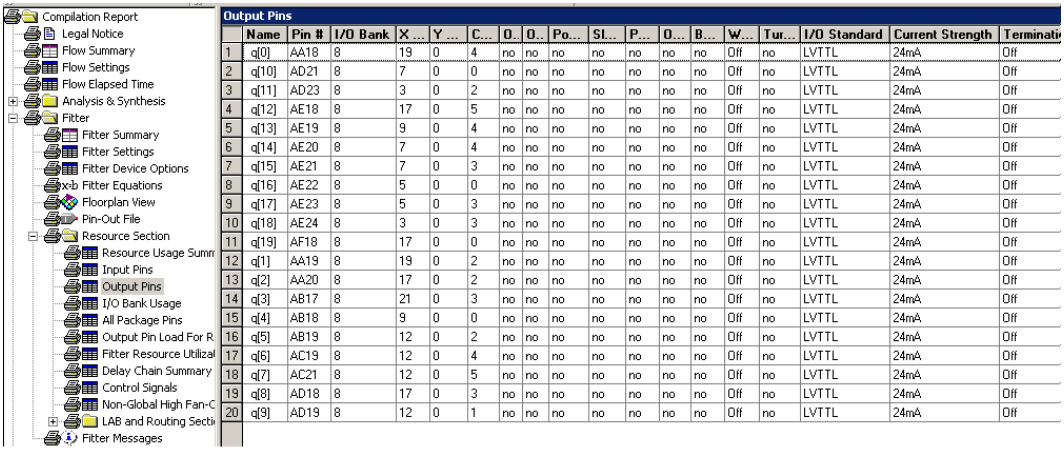
the load, and choose the I/O standard used and I/O data rate for each design module. Table 3–8 describes the values that are entered in the **General I/O Power** section of the PowerPlay early power estimator.

Table 3–8. General I/O Power Section Information

Column Heading	Description
Design Module	Enter a name for the design module in this column. This is an optional value.
f_{MAX} (MHz)	Enter the clock frequency for this design module. This is the frequency of the clock used to feed the I/O registers or the registers that feed the I/O pins. This value is limited by the maximum I/O pin frequency specification for the device family.
# Outputs & Bidirectional Pins	Enter the number of output and bidirectional pins used in this design module. A differential pair of pins should be considered as one pin.
Toggle %	Enter the average percentage of output and bidirectional pins toggling on each clock cycle. The toggle percentage ranges from 0 to 100%. Typically, the toggle percentage is 12.5%. To be more conservative, you can use a higher toggle percentage.
Avg. Capacitive Load (pF)	Enter the average capacitive load in pico-Farads (pF) for the output and bidirectional pins in this clock domain.
I/O Standard	Select the I/O standard used for the output or bidirectional pins in this clock domain from the list. The calculated I/O power varies based on the I/O standard. For I/O standards that recommend termination (for example, SSTL and HSTL), the PowerPlay early power estimator assumes you are using external termination resistors. If you are not using external termination resistors, you should choose the LVTTL I/O standard with the same voltage and similar drive strength as the terminated I/O standard. There are up and down scroll bars to view all the I/O standards in the drop-down list.
I/O Data Rate	Select the I/O data rate (either single data rate (SDR) or double data rate (DDR)) from the list.

Figure 3–15 shows an example of the **Output Pins** report in the Quartus II software Compilation Report for a design targeting a Stratix device. The Compilation Report lists the I/O standard used on each pin. In this example, there are 20 3.3-V LVTTL output pins with 24-mA drive strength operating at single-data rate with an average load of 10 pF. These pins are fed by registers that use a 100-MHz clock and toggle an average of 12.5%. Figure 3–16 shows the Stratix PowerPlay early power estimator and the estimated power consumed by the I/O pins used in this example.

Figure 3–15. Output Pins Report in Compilation Report



Compilation Report
- Legal Notice
- Flow Summary
- Flow Settings
- Flow Elapsed Time
- Analysis & Synthesis
- Fitter
  - Fitter Summary
  - Fitter Settings
  - Fitter Device Options
  - Fitter Equations
  - Floorplan View
  - Pin-Out File
  - Resource Section
    - Resource Usage Summ
    - Input Pins
    - Output Pins
    - I/O Bank Usage
    - All Package Pins
    - Output Pin Load For R
    - Fitter Resource Utilizat
    - Delay Chain Summary
    - Control Signals
    - Non-Global High Fan-C
    - LAB and Routing Secti
  - Fitter Messages

Output Pins

	Name	Pin #	I/O Bank	X ...	Y ...	C...	O..	O...	Po...	Sl...	P...	O...	B...	W...	Tur...	I/O Standard	Current Strength	Terminati
1	q[0]	AA18	8	19	0	4	no	no	no	no	no	no	no	Off	no	LVTTL	24mA	Off
2	q[10]	AD21	8	7	0	0	no	no	no	no	no	no	no	Off	no	LVTTL	24mA	Off
3	q[11]	AD23	8	3	0	2	no	no	no	no	no	no	no	Off	no	LVTTL	24mA	Off
4	q[12]	AE18	8	17	0	5	no	no	no	no	no	no	no	Off	no	LVTTL	24mA	Off
5	q[13]	AE19	8	9	0	4	no	no	no	no	no	no	no	Off	no	LVTTL	24mA	Off
6	q[14]	AE20	8	7	0	4	no	no	no	no	no	no	no	Off	no	LVTTL	24mA	Off
7	q[15]	AE21	8	7	0	3	no	no	no	no	no	no	no	Off	no	LVTTL	24mA	Off
8	q[16]	AE22	8	5	0	0	no	no	no	no	no	no	no	Off	no	LVTTL	24mA	Off
9	q[17]	AE23	8	5	0	3	no	no	no	no	no	no	no	Off	no	LVTTL	24mA	Off
10	q[18]	AE24	8	3	0	3	no	no	no	no	no	no	no	Off	no	LVTTL	24mA	Off
11	q[19]	AF18	8	17	0	0	no	no	no	no	no	no	no	Off	no	LVTTL	24mA	Off
12	q[1]	AA19	8	19	0	2	no	no	no	no	no	no	no	Off	no	LVTTL	24mA	Off
13	q[2]	AA20	8	17	0	2	no	no	no	no	no	no	no	Off	no	LVTTL	24mA	Off
14	q[3]	AB17	8	21	0	3	no	no	no	no	no	no	no	Off	no	LVTTL	24mA	Off
15	q[4]	AB18	8	9	0	0	no	no	no	no	no	no	no	Off	no	LVTTL	24mA	Off
16	q[5]	AB19	8	12	0	2	no	no	no	no	no	no	no	Off	no	LVTTL	24mA	Off
17	q[6]	AC19	8	12	0	4	no	no	no	no	no	no	no	Off	no	LVTTL	24mA	Off
18	q[7]	AC21	8	12	0	5	no	no	no	no	no	no	no	Off	no	LVTTL	24mA	Off
19	q[8]	AD18	8	17	0	3	no	no	no	no	no	no	no	Off	no	LVTTL	24mA	Off
20	q[9]	AD19	8	12	0	1	no	no	no	no	no	no	no	Off	no	LVTTL	24mA	Off

Figure 3–16. General I/O Power Section in the Stratix PowerPlay Early Power Estimator

General I/O Power

Design Module	fMAX (MHz)	# Outputs & Bidirectional Pins	Toggle %	Avg. Capacitive Load (pF)	I/O Standard	I/O Data Rate	ICCIO (mA)	PIO (mW)	ICCVTT (mA)
1	100	20	12.50	10	3.3_LVTTL/LVCMOS_24	SDR	14.63	48.26	0

High-Speed Transceiver Blocks

The **High-Speed Transceiver Blocks** section is only found in the Stratix GX device PowerPlay early power estimator. Stratix GX devices contain transceivers that can receive and transmit data at rates up to 3.125 Gbps. Each transceiver block contains four channels, a transmit PLL, four receive PLLs, and other control circuitry. The Stratix GX transceiver blocks are located in I/O bank five. The total power consumed by the transceiver blocks is reported as $P_{TRANSCEIVER}$, which is separate from P_{INT} and P_{IO}. The **High-Speed Transceiver Blocks** section in the Stratix GX PowerPlay early power estimator is divided into receiver and transmitter sections.

Each row represents a separate transceiver block. For each transceiver block used on the receiving side, you need to enter the data rate (Gbps) and the number of channels used. For each transceiver block used on the transmitting side, you need to enter the data rate (Gbps), the number of channels used, the toggle percentage of the serializer outputs, the maximum output differential voltage (V_{OD}), and the pre-emphasis

settings of the programmed V_{OD}. Table 3–9 describes the values that are entered in the **High-Speed Transceiver Blocks** section of the PowerPlay early power estimator.

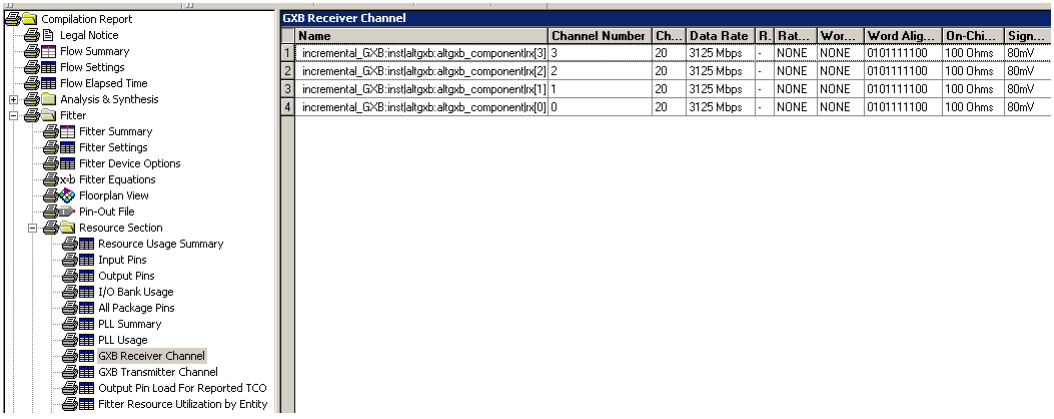
Table 3–9. High-Speed Transceiver Blocks Section Information

Column Heading	Description
Transceiver Block	Enter a name for the transceiver block in this column. This is an optional value.
Data Rate (Gbps)	Enter the maximum data rate (in Gbps) for the receiver and transmitter channels in the targeted transceiver block. The data rate must be a decimal number from 0 to 3.125 Gbps.
# of Channels	Enter the number of receiver and transmitter channels running at the above data rate. Since each transceiver block in Stratix GX devices can support up to four high speed transceiver channels, this value must be an integer value from 0 to 4
Toggle %	Enter the toggle percentage, which is the average percentage of serializer outputs toggling at each high-speed clock cycle. The toggle percentage ranges from 0 to 100%. Typically, the toggle percentage is 25%. To be more conservative, you can use a higher toggle percentage.
V_{OD} (mV)	The output differential voltage (V_{OD}) of the transmitter channels in mV. The V_{OD} values are selected from a list. The V_{OD} values for each Transmitter channel is obtained from the Quartus II software **Compilation Report** under **Fitter** > **Resource Section** > **GXB Transmitter Channel** > **Output Buffer Differential Voltage**.
Pre-emphasis Setting (%)	The pre-emphasis percentage levels of the transmitter channels are selected from a list. The pre-emphasis levels can be set at 0%, 5%, 10%, 15%, 20%, or 25%. The pre-emphasis setting for each Transmitter channel is obtained from the Quartus II **Compilation Report** under **Fitter** > **Resource Section** > **GXB Transmitter Channel** > **Output Buffer Pre-emphasis**.

Figures 3–17 and 3–18 show the GXB Receive Channel and GXB Transmit Channel reports in the Quartus II software Compilation Report for a design targeting a Stratix GX device. This example uses a transceiver block that supports four receive and transmit channels operating at 3.125 Gbps with data output toggling at 25%, a V_{OD} of 1,000 mV, and a pre-emphasis level of 10%. Figure 3–17 shows the Stratix GX PowerPlay early power estimator and the estimated power consumed by the transceiver blocks used in this example.

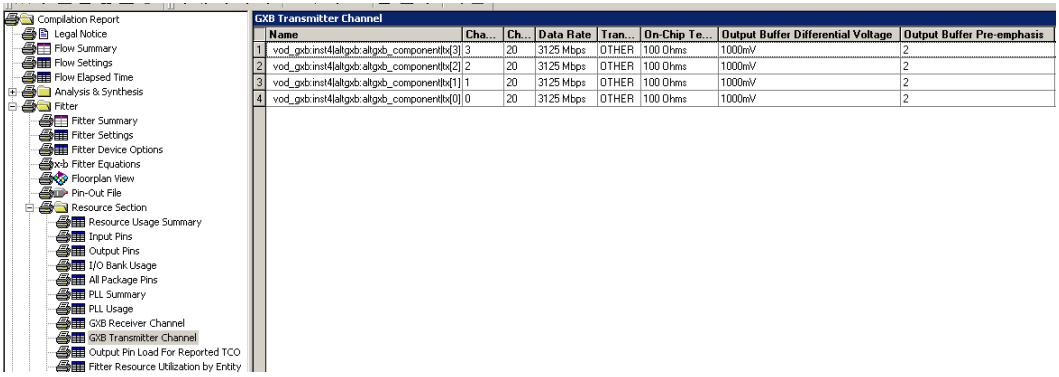
The **High-Speed Transceiver Block** section of the PowerPlay early power estimator includes the receiver and transmitter PLL power used in the transceiver blocks. You do not need to estimate the receiver and transmitter PLL power in the PLL section separately.

Figure 3–17. Stratix GX Transceiver Receiver Channel Report in the Compilation Report



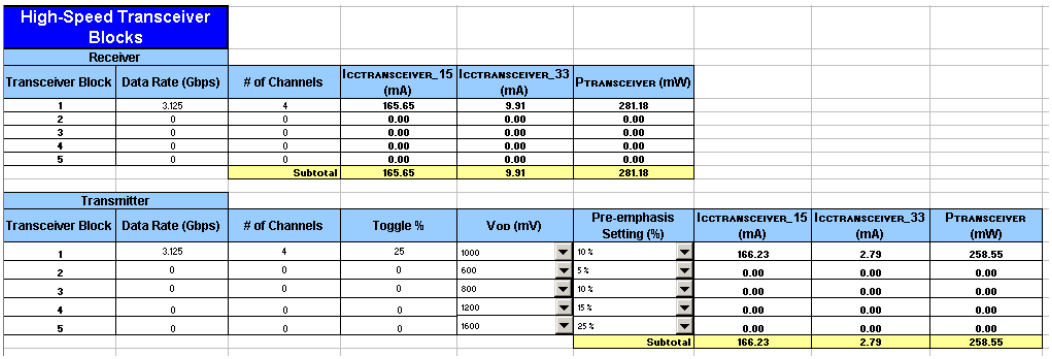
	Name	Channel Number	Ch...	Data Rate	R...	Rat...	Wor...	Word Alig...	On-Chi...	Sign...
1	incremental_GXB:inst|altgxb:altgxb_component|rx[3]	3	20	3125 Mbps	-	NONE	NONE	0101111100	100 Ohms	80mV
2	incremental_GXB:inst|altgxb:altgxb_component|rx[2]	2	20	3125 Mbps	-	NONE	NONE	0101111100	100 Ohms	80mV
3	incremental_GXB:inst|altgxb:altgxb_component|rx[1]	1	20	3125 Mbps	-	NONE	NONE	0101111100	100 Ohms	80mV
4	incremental_GXB:inst|altgxb:altgxb_component|rx[0]	0	20	3125 Mbps	-	NONE	NONE	0101111100	100 Ohms	80mV

Figure 3–18. Stratix GX Transceiver Transmitter Channel Report in the Compilation Report



	Name	Cha...	Ch...	Data Rate	Tran...	On-Chip Te...	Output Buffer Differential Voltage	Output Buffer Pre-emphasis
1	vod_gxb:inst4|altgxb:altgxb_component|tx[3]	3	20	3125 Mbps	OTHER	100 Ohms	1000mV	2
2	vod_gxb:inst4|altgxb:altgxb_component|tx[2]	2	20	3125 Mbps	OTHER	100 Ohms	1000mV	2
3	vod_gxb:inst4|altgxb:altgxb_component|tx[1]	1	20	3125 Mbps	OTHER	100 Ohms	1000mV	2
4	vod_gxb:inst4|altgxb:altgxb_component|tx[0]	0	20	3125 Mbps	OTHER	100 Ohms	1000mV	2

Figure 3–19. High-Speed Transceiver Block Section in the Stratix GX PowerPlay Early Power Estimator



High-Speed Transceiver Blocks

Receiver

Transceiver Block	Data Rate (Gbps)	# of Channels	ICCTRANSCEIVER_15 (mA)	ICCTRANSCEIVER_33 (mA)	PTRANSCEIVER (mW)
1	3.125	4	165.65	9.91	281.18
2	0	0	0.00	0.00	0.00
3	0	0	0.00	0.00	0.00
4	0	0	0.00	0.00	0.00
5	0	0	0.00	0.00	0.00
		Subtotal	165.65	9.91	281.18

Transmitter

Transceiver Block	Data Rate (Gbps)	# of Channels	Toggle %	VOD (mV)	Pre-emphasis Setting (%)	ICCTRANSCEIVER_15 (mA)	ICCTRANSCEIVER_33 (mA)	PTRANSCEIVER (mW)
1	3.125	4	25	1000	10 %	166.23	2.79	258.55
2	0	0	0	600	5 %	0.00	0.00	0.00
3	0	0	0	800	10 %	0.00	0.00	0.00
4	0	0	0	1200	15 %	0.00	0.00	0.00
5	0	0	0	1600	25 %	0.00	0.00	0.00
					Subtotal	166.23	2.79	258.55

Power-Up I_{CC}

Power-up I_{CC} is and estimation of the current required to successfully power-up the device and is observed on the V_{CCINT} power supply. For Stratix and Stratix GX devices, the PowerPlay early power estimator provides both the typical and maximum power-up I_{CC}. For Cyclone devices, the PowerPlay early power estimator provides the maximum power-up I_{CC}.

The power-up I_{CC} current is not added to the total current (I_{CCINT}) because it is only observed when the device is powering up. The power-up current is independent of the current consumption during device user-mode. If the power-up I_{CC} is greater than the total I_{CCINT}, you should select a regulator that supports the maximum power-up I_{CC} requirement.

For more information on power-up I_{CC}, refer to the *DC & Switching Characteristics* chapter of the appropriate device family handbook.

Total

The **Total** section displays the total current and power estimation for the internal logic array (Internal V_{CCINT}), the I/O interface (I/O (V_{CCIO})), the transceiver (Transceiver (V_{CC})), if applicable, and the total power consumption for the whole design. The total I_{CCINT} and P_{INT} are the summation of all the subtotals of the I_{CCINT} and P_{INT} calculated in each section. The total I_{CCIO} and P_{IO} are the summation of all the subtotals of the I_{CCIO} and P_{IO} calculated in the relevant sections. For the Stratix GX PowerPlay early power estimator, the total power consumed by the high-speed transceiver blocks is listed separately as $P_{TRANSCEIVER}$. The

total P_{INT}, total P_{IO}, $P_{TRANSCEIVER}$ (for Stratix GX devices only), and total PowerPlay early power estimator are also displayed in the **Device** section at the top of the PowerPlay early power estimator.

Thermal Analysis

In the **Thermal Analysis** section, enter the device's ambient temperature (T_a) in degrees Celsius. T_j is the maximum recommended operating junction temperature based on the temperature grade of the device you choose. The required junction-to-ambient thermal resistance (θ_{JA}) is the minimum θ_{JA} for the ambient temperature you entered and the amount of power your design consumes. The required θ_{JA} must be greater than the θ_{JA} for the chosen device and package.

Based on the device and package you selected in the **Device** section, the PowerPlay early power estimator determines the junction-to-case thermal resistance (θ_{JC}) and θ_{JA} at still air and air flow rates of 100, 200, and 400 LFpM. These numbers are obtained from the *Altera Device Package Information Data Sheet*.

The maximum allowable power (P_{MAX}) is calculated based on the device package chosen and the ambient temperature using the following equation:

$$(T_j - T_a) / \theta_{JA} = P_{MAX}$$

The P_{MAX} is reported for still air and air flow rates of 100, 200, and 400 LFpM. If the calculated power of your design is greater than the P_{MAX} for the chosen device and package, you need to take the appropriate thermal measures by adding a heat sink or cooling fan on your board.

If you are not using a heat sink, refer to the **Without Heat Sink** section of the PowerPlay early power estimator, which displays whether your selected device package θ_{JA} is less than the required θ_{JA} of your design at still air or with airflow. "Good" indicates that the package θ_{JA} is less than the minimum required θ_{JA} for your design. A blank result indicates that the package θ_{JA} is more than the minimum required θ_{JA}. "No Value" indicates that you have not completely entered the required information.

If you need to use a heat sink, you need to enter the case-to-heat sink thermal resistance (θ_{CS}) and heat sink-to-ambient thermal resistance (θ_{SA}) at still air and airflow rates of 100, 200, and 400 LFpM. The heat sink manufacturer should specify these values. The results in the **With Heat Sink** section tells you whether your device package θ_{JA} is less than the required θ_{JA} at still air or with airflow when using a heat sink. A blank

result indicates that the package θ_{JA} is more than the minimum required θ_{JA}. "No Value" indicates that you have not entered all of the required information.

Figure 3–20 shows the **Thermal Analysis** section in the Stratix PowerPlay early power estimator.

For more information on device thermal analysis, refer to *AN 185: Thermal Management Using Heat Sinks*.

Figure 3–20. Thermal Analysis Section in the Stratix PowerPlay Early Power Estimator

Thermal Analysis

Tj (Degrees C)	Ta (Degrees C)	Required θJA
85	40	10.82

Thermal Resistance Values for Chosen Device & Package

	θJA			
θJC	Still Air	100 LFpM	200 LFpM	400 LFpM
0.25	10.5	8.5	7.1	6

Maximum Allowable Power (Pmax) for Chosen Device & Package

	Still Air	100 LFpM	200 LFpM	400 LFpM
Pmax (W)	4.29	5.29	6.34	7.50

The tables below show possible package & airflow combinations.
Based on the thermal characteristics of the device and the heat sink, the following values will be returned to indicate if the thermal requirements have been met.
- **A result of "Good" means the package theta JA is less than the minimum required theta JA.**
- **A blank result means the package theta JA exceeds the minimum required theta JA.**
- **A result of "No Value" means unable to compare because user data missing.**

Without Heat Sink

	Airflow			
Package	Still Air	100 LFpM	200 LFpM	400 LFpM
780 FineLine BGA	Good	Good	Good	Good

With Heat Sink

Specify the thermal characteristics of the heat sink with or without airflow in the white boxes.
Refer to AN 185 for heat sink vendor references.

Required θJA	Package θJC	Required θCA
10.82	0.25	10.57

θCS	θSA Still Air	θSA 100 LFpM	θSA 200 LFpM	θSA 400 LFpM
0.00	0.00	0.00	0.00	0.00

	Airflow			
Package	Still Air	100 LFpM	200 LFpM	400 LFpM
780 FineLine BGA	No Value	No Value	No Value	No Value