## Contents

### Chapter 1. About This Kit
- Introduction ................................................................. 1–1
- Kit Features ................................................................. 1–1

### Chapter 2. Getting Started
- Introduction ................................................................. 2–1
- Before You Begin ......................................................... 2–1
  - Check the Kit Contents ............................................... 2–1
  - Inspect the Board ....................................................... 2–2
  - Hardware Requirements ............................................. 2–2
  - Software Requirements .............................................. 2–3
  - References ............................................................... 2–3

### Chapter 3. Software Installation
- Introduction ................................................................. 3–1
- Installing the DSP Development Kit CD-ROM ..................... 3–1
- Installing the Altera Complete Design Suite DVD ............... 3–2
- Installing MathWorks MATLAB/Simulink CD-ROM ............ 3–3
- Installing the USB-Blaster Driver .................................. 3–3
- Licensing Considerations ............................................. 3–4

### Chapter 4. DSP Development Kit Hardware Setup
- Introduction ................................................................. 4–1
- Requirements ............................................................... 4–1
- Powering up the Board ................................................ 4–1
- Configuring the FPGA .................................................. 4–6

### Chapter 5. Factory Designs
- Understanding the Factory Design .................................. 5–1
- Exercising the A/D and D/A Converter Performance Test ........ 5–2
- Configuring the Board .................................................. 5–2
- Collecting Data Using the SignalTap II Logic Analyzer ....... 5–3
- Analyzing the Data in the MATLAB Software .................... 5–4
- Conclusion ................................................................. 5–6

### Appendix A. Programming the Flash Device
- Overview ................................................................. A–1
- Creating a Flash File ................................................... A–1
- Parallel Flash Loader Instantiation ................................ A–3
- Programming the Flash Device ...................................... A–3
- Restoring the Factory Design to the Flash Device ............. A–5

### Additional Information
- Revision History ......................................................... About–1
- How to Contact Altera ................................................ About–1
- Typographic Conventions ........................................... About–2
1. About This Kit

Introduction

Welcome to the Altera® DSP Development Kit, Cyclone® III Edition. This kit provides a platform for experimenting with Digital Signal Processing (DSP) using Altera’s design environment and intellectual property. Included are a Data Conversion high-speed mezzanine card (HSMC), a full-featured field-programmable gate array (FPGA) development board, hardware and software development tools, documentation, and accessories needed to begin DSP development.

Kit Features

The DSP Development Kit, Cyclone III Edition contains the following:

■ A Data Conversion HSMC—a prototyping platform that allows you to develop high-performance DSP designs. Key features of the Data Conversion HSMC include two high-speed analog-to-digital (A/D) converters, a dual digital-to-analog (D/A) converter and a Stereo Audio coder/decoder (CODEC).

For detailed information about the components and interfaces included on the Data Conversion HSMC, and about their locations on the board, refer to the Data Conversion HSMC Reference Manual.

■ A Cyclone III Development Board—a hardware platform with integrated USB-Blaster™ and EP3C120 FPGA to support the Data Conversion HSMC. The board also provides power for the Data Conversion HSMC.

For information about setting up and powering up the Cyclone III development board, refer to the Cyclone III Development Kit User Guide. For detailed information about the components and interfaces included on the Cyclone III development board and about their locations on the board, refer to the Cyclone III Development Board Reference Manual.

■ Quartus® II Web Edition Software—The Quartus II software (available on the DVD) integrates in nearly any design environment, with interfaces to industry-standard EDA tools. The kit includes:
  ■ Quartus II Web Edition Software
  ■ MegaCore® IP Library
  ■ Nios® II Embedded Design Suite
  ■ ModelSim®—Altera Web Edition
  ■ DSP Builder
  ■ Free Quartus II Web Edition software license, Windows platform only
For more information, refer to the Altera website at www.altera.com/products/software/products/quartus2web/sof-quarwebmain.html.

- **DSP Development Kit, Cyclone III Edition CD-ROM**—This CD-ROM includes several designs for exercising the Data Conversion HSMC. In addition, the following documentation is included:
  - Design files for the boards included in the kit
  - *Data Conversion HSMC Reference Manual*
  - *Cyclone III Development Board Reference Manual*

- **MathWorks MATLAB/Simulink CD-ROM**—This CD-ROM contains third-party tools that are used in conjunction with DSP Builder as part of Altera’s DSP development flow. MATLAB is a high-level technical computing language environment for algorithm development, data visualization, data analysis, and numerical computation. Simulink provides an interactive graphical environment and a customizable set of block libraries that let you accurately design, simulate, implement, and test signal processing systems.

  A 30-day license for MATLAB/Simulink software is included as part of the DSP Development Kit, Cyclone II Edition. To obtain the personal license password and for more information, visit MathWorks at: www.mathworks.com/products/connections/trials/altera.shtml
Introduction

This user guide familiarizes you with the contents of the kit and guides you through the DSP Development Kit, Cyclone III Edition setup. Using this guide, you can do the following:

■ Inspect the contents of the kit
■ Install the Altera Development Suite Tools
■ Set up licensing
■ Install the DSP Development Kit, Cyclone III Edition CD-ROM
■ Set up, power up, and verify correct operation of the kit hardware
■ Configure the Cyclone III FPGA
■ Find and use the tutorials
■ Set up and run included application examples and demonstrations


Before You Begin

Before using the kit or installing the software, check the kit contents and inspect the board to verify that you received all of the items listed in this section. If any of the items are missing, contact Altera before you proceed.

Check the Kit Contents

The DSP Development Kit, Cyclone III Edition contains the following items:

■ Data Conversion HSMC
■ Cyclone III development board with an EP3C120F780C7N Cyclone III device
■ Altera Complete Design Suite DVD containing:
  ■ Quartus II Web Edition Software
  ■ MegaCore IP Library
  ■ Nios II Embedded Software Design Tools
  ■ ModelSim-Altera Web Edition simulation package
  ■ DSP Builder
- DSP Development Kit, Cyclone III Edition CD-ROM, which includes:
  - Reference designs for DSP application
  - Design examples
  - Data Conversion HSMC Reference Manual
  - DSP Development Kit, Cyclone III Edition Getting Started User Guide (this document)
  - Device data sheets and tutorials
  - Schematic and board design files
- MathWorks MATLAB/Simulink CD-ROM
- SLP-50 anti-aliasing filter from Mini-Circuits
- SMA cables for interconnecting the devices on board
- USB cable for downloading designs
- Power supply and adapters for North America, Europe, the United Kingdom, and Japan

To ensure that you have the most up-to-date information about this product, go to the Altera website at www.altera.com/products/devkits/altera/kit-cyc3-dsp.html.

Inspect the Board

Place the board on an anti-static surface and inspect it to ensure that it has not been damaged during shipment.

Without proper anti-static handling, the Cyclone III development board can be damaged.

Verify that all components are on the board and appear intact.

In typical applications with the Cyclone III development board, a heatsink is not necessary. However, under extreme conditions the board may require additional cooling to stay within operating temperature guidelines. You may wish to perform power consumption and thermal modeling to determine whether your application requires additional cooling.

For more information about power consumption and thermal modeling, refer to AN 358: Thermal Management for FPGAs.

Hardware Requirements

The Quartus II software has some minimum system requirements. Otherwise, the Cyclone III development kit provides all of the hardware needed to use the board.

For Quartus II requirements, refer to the Quartus II Installation & Licensing for Windows Manual.
Software Requirements

This kit requires the following software:

- Windows XP operating system
- Quartus II Web Edition (refer to the readme.txt file on the CD-ROM for specific version requirements)
- MathWorks MATLAB and Simulink DSP system design and modeling tools provided on the MathWorks MATLAB and Simulink Evaluation CD-ROM. This software is required to create hardware description language (HDL) designs that use blocks from DSP Builder.

Although it is already available on the DVD included in the kit, you can also download the Quartus II software from the Altera website at: www.altera.com/products/software/quartus-ii/subscription-edition/qts-se-index.html.

Refer to the Quartus II Installation & Licensing for Windows Manual for more information about the Quartus II system software requirements, especially heeding the following:

- A web browser, Microsoft Internet Explorer version 5.0 or later or Firefox version 2.0 or later. You must have a web browser to register the Quartus II software and request license files. Refer to “Licensing Considerations” on page 3–4.
- Version 2.0 or later of the .NET framework.

If you receive an Application Error message when launching the demo application, install version 2.0 or later versions of the .NET framework. Some Windows versions do not have runtime DLL for the .NET application. The .NET framework application can be downloaded from the following location: www.microsoft.com/download.

References

For other related information, refer to the following websites:

- For additional HSMCs available for purchase: www.altera.com/products/devkits/kit-daughter_boards.jsp
- For the Cyclone III device documentation: www.altera.com/literature/lit-cyc3.jsp
- For the Cyclone III reference designs: www.altera.com/endmarkets/refdesigns/device/cyclone3/cyclone3-index.jsp
- For eStore if you want to purchase devices: www.altera.com/buy/devices/buy-devices.html
- For Cyclone III OrCAD symbols: www.altera.com/support/software/download/pcb/pcb-pcb_index.html
3. Software Installation

Introduction

The instructions in this section explain how to install the following:

- DSP Development Kit, Cyclone III Edition CD-ROM
- Altera Complete Design Suite DVD, including:
  - Quartus II Web Edition Software
  - MegaCore functions from the MegaCore IP Library
  - Nios II Embedded Design Suite
  - ModelSim-Altera Web Edition
  - DSP Builder
- MathWorks MATLAB/Simulink Software CD-ROM

Before starting the installation, verify that you have complied with the conditions described in “Software Requirements” on page 2–3.

Installing the DSP Development Kit CD-ROM

The DSP Development Kit, Cyclone III Edition CD-ROM contains the following items:

- Reference designs for DSP application
- Design examples
- Data Conversion HSMC Reference Manual
- DSP Development Kit, Cyclone III Edition Getting Started User Guide (this document)
- Device datasheets and tutorials
- Schematic and board design files

To install the Cyclone III Development Kit CD-ROM, perform the following steps:

1. Insert the Cyclone III Development Kit CD-ROM into the CD-ROM drive.
   
   The CD-ROM should start an auto-install process. If it does not, browse to the CD-ROM drive and double-click on the setup.exe file.

2. Follow the on-screen instructions to complete the installation process.

The installation program copies the DSP Development Kit, Cyclone III Edition files to the computer hard disk and creates a Programs > Altera > DSP Development Kit, Cyclone III Edition <version#> Windows Start menu shortcut. Use this shortcut to launch the development kit graphical user interface (GUI).
When the installation is complete, the DSP Development Kit, Cyclone III Edition installation program creates the directory structure shown in Figure 3–1, where <path> is the DSP Development Kit, Cyclone III Edition installation directory.

![Figure 3–1. DSP Development Kit, Cyclone III Edition Installed Directory Structure](image)

Table 3–1 lists the file directory names and a description of their contents. The default Windows installation directory is C:\altera\<version#>\kits.

<table>
<thead>
<tr>
<th>Directory Name</th>
<th>Description of Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>board_design_files</td>
<td>Contains schematic, layout, assembly, and bill of material board design files. Use these files as a starting point for a new prototype board design.</td>
</tr>
<tr>
<td>demos</td>
<td>Contains unsupported demonstration files for various use with the development board and/or HSMC.</td>
</tr>
<tr>
<td>documents</td>
<td>Contains the development kit documentation.</td>
</tr>
<tr>
<td>examples</td>
<td>Contains the sample design files for the DSP Development Kit, Cyclone III Edition.</td>
</tr>
<tr>
<td>factory_recovery</td>
<td>Contains programming files for use with the development kit board to return it to the factory default status.</td>
</tr>
</tbody>
</table>

**Installing the Altera Complete Design Suite DVD**

The Quartus II software is the primary FPGA development tool used, along with the MATLAB software, to create the reference designs used in this development kit. Additionally, you may want to install the Nios II Embedded Design Suite found in the Altera Complete Design Suite DVD. The Nios II soft-core embedded processor runs on Altera FPGAs. Some of the reference designs included in this development kit use the Nios II processor.

To install the Altera Complete Design Suite DVD, which includes the Quartus II software, perform the following steps:

1. Insert the Altera Complete Design Suite DVD into the DVD drive.
2. Click **Install free package** on the startup screen. Follow the on-screen instructions and accept all default settings.
3. Next, you can install the DSP Builder software by clicking the **Install** button for the software, which is located in the **Install additional software** section on the startup screen.
If you plan to use the DSP Builder, install the MathWorks MATLAB and Simulink CD-ROM first. Also, because the MathWorks software trial licence is valid only for 30 days, only install the MathWorks MATLAB/Simulink CD-ROM when you are ready to use the DSP Builder, the Simulink software for DSP development, or the factory designs in Chapter 5, Factory Designs.

4. After installing the DSP Builder software, request and install a license to enable it.

For information about obtaining a license file, refer to “Licensing Considerations” on page 3–4.

## Installing MathWorks MATLAB/Simulink CD-ROM

To install MathWorks software, perform the following steps:

1. Before installing, make sure that you have your Personal License Password (PLP) available. To obtain the 30-day evaluation license and for more information, visit MathWorks at [www.mathworks.com/products/connections/trials/altera.shtml](http://www.mathworks.com/products/connections/trials/altera.shtml).

2. If it is running, close the MATLAB/Simulink software.

3. Insert MathWorks MATLAB/Simulink CD-ROM. The MathWorks Installer automatically starts, displaying the **Welcome to The MathWorks Installer** dialog box.

4. In the dialog box, choose **Install** and click **Next**.

5. Enter your name, company name, and PLP in the **License Information** dialog box and click **Next**.

6. Review the software licensing agreement. If you agree with the terms, turn on **Yes** and click **Next**.

7. Select **Typical** or **Custom installation** (for any user-specific selections) and click **Next**.

8. Click **Install**.

9. Click **Finish**.

## Installing the USB-Blaster Driver

The Cyclone III development board includes integrated USB-Blaster circuitry for FPGA programming. However, for the host computer and development board to communicate, you must install the USB-Blaster driver on the host computer.

To download the USB-Blaster driver, go to the Altera support site at [www.altera.com/support/software/drivers/dri-index.html](http://www.altera.com/support/software/drivers/dri-index.html).

Licensing Considerations

Before using the Quartus II software, you must request a license file from the Altera website at www.altera.com/licensing and install it on your computer. When you request a license file, Altera emails you a license.dat file that enables the software.

To license the Quartus II software, you need your network interface card (NIC) ID, a 12-digit hexadecimal number that identifies your computer. Networked (or floating-node) licensing requires a NIC ID or server host ID. When obtaining a license file for network licensing, use the NIC ID from the computer that issues the Quartus II licenses to distributed users over a network. You can find the NIC ID for your card by typing ipconfig/all at a command prompt. Your NIC ID is the number on the physical address line, without the dashes.
4. DSP Development Kit Hardware Setup

Introduction
The instructions in this chapter explain how to attach the Data Conversion HSMC to the Cyclone III development board and configure the FPGA.

Requirements
Before starting the installation, verify that you have complied with the conditions described in “Hardware Requirements” on page 2–2 and have completed the following requirements:

- Quartus II software installed on the host computer
- USB-Blaster driver software installed on the host computer

The Cyclone III development board includes integrated USB-Blaster circuitry for FPGA programming. Host computer and development board cannot communicate without the USB-Blaster driver software installed. For installation information, refer to “Installing the USB-Blaster Driver” on page 3–3.

Powering up the Board
Figure 4–1 shows the Cyclone III development board and its components.
Figure 4–1. Cyclone III Development Board Layout and Components
Figure 4–2 shows the Data Conversion HSMC card layout and components.

**Figure 4–2. Data Conversion HSMC Card Layout and Components**
Figure 4–3 shows the Data Conversion HSMC card connected to the Cyclone III development board.

**Figure 4–3. Data Conversion HSMC Card Connection to the Cyclone III Development Board**

We recommend the standoffs be installed in order to hold the two boards at the proper heights. The shorter standoffs should be installed in the four corners of the Cyclone III development board. Two of the longer standoffs should be installed in the mounting holes near the audio connectors on the Data Conversion HSMC. This minimizes the stress on the HSM connector.

Before powering up, prepare the board by performing the following steps:

1. If other cards are plugged into the HSMC ports, remove them. Figure 4–3 shows a HSMC plugged into both Port A and Port B.

2. Ensure that the POWER switch SW2 is in the OFF (or DOWN) position. Refer to Figure 4–1 on page 4–2 for the location of this switch.

3. Configure the 8-position SW1 DIP switch to the default settings in Table 4–1.
4. Ensure that the 4-position SW3 mini-DIP switches and the two jumpers are set to the default positions shown in Table 4–2.

<table>
<thead>
<tr>
<th>Switch</th>
<th>Name</th>
<th>Function</th>
<th>Default Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>mW/mA</td>
<td>mW</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>V/W</td>
<td>V</td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>RSV0</td>
<td>MAX_reserve0</td>
<td>X</td>
</tr>
<tr>
<td>4</td>
<td>RSV1</td>
<td>MAX_reserve1</td>
<td>X</td>
</tr>
<tr>
<td>5</td>
<td>MAX0</td>
<td>PFL Disable</td>
<td>1</td>
</tr>
<tr>
<td>6</td>
<td>MAX1</td>
<td>MAX_DIP1</td>
<td>X</td>
</tr>
<tr>
<td>7</td>
<td>MAX2</td>
<td>MAX_DIP2</td>
<td>X</td>
</tr>
<tr>
<td>8</td>
<td>MAX3</td>
<td>MAX_DIP3</td>
<td>X</td>
</tr>
</tbody>
</table>

Note to Table 4–1:
(1) X = don’t care

5. Verify that the PGM CONFIG SELECT rotary switch SW5 is set to 0.
   On power up, the development board uses a preloaded configuration to demonstrate that the board is operating correctly.

6. Connect the Data Conversion HSMC to HSMC Port A on the left side of the development board.

7. Verify the jumper configuration is set to the following default settings:
   - J2 ADC_A POWER DOWN removed
   - J3 ADC_A CK SEL jumpers on pins 1-3 and 4-6
   - J6 ADC_B POWER DOWN removed
   - J7 ADC_B CK SEL jumpers on pins 1-3 and 4-6
   - J10 DAC GSET removed
   - J11 DAC MODE removed
   - J13 DAC SLEEP removed
   - J15 DAC_A CLK SEL jumpers on pins 1-3 and 4-6
   - J17 DAC_B CLK SEL jumpers on pins 1-3 and 4-6
   - J23 CLK OUT SEL jumpers on pins 1-3 and 2-4

8. Set the user dip switches on the Cyclone III development board with all of the switches open.
Power up the development board by performing the following steps:

1. Connect the 16-V DC adapter to the development board and to a power source.

> Use only the supplied 16-V power supply. Power regulation circuitry on the board could be damaged by supplies greater than 16 V.

2. Slide the POWER switch to ON. The nearby blue POWER light-emitting diode (LED) lights up.

3. Confirm that user LEDs 0-7 flash in a scrolling, side-to-side pattern. For customized configurations, the pattern depends on the application.

   For information about custom configurations, refer to “Programming the Flash Device” on page A–3.

### Configuring the FPGA

Before configuring the FPGA, ensure that the Quartus II software and the USB-Blaster driver software are installed on the host computer and the development board is powered on.

> For USB-Blaster driver installation information, refer to “Installing the USB-Blaster Driver” on page 3–3.

To configure the Cyclone III FPGA, perform the following steps:

1. Verify that the 4-position SW3 mini-DIP switches and the two jumpers are set to the default positions shown in Table 4–2 on page 4–5.

2. Connect the USB cable to the development board USB port.

3. Cycle the POWER switch OFF then ON.

4. Start the Quartus II software.


6. Click Add File and select `<path>\examples\cycloneIII_3c120_dsp_example_ChA\cycloneIII_3c120_dsp_factory_design_loopback_top.sof`.

7. Turn on the Program/Configure option for the added file.

8. Click Start to download the selected file to the FPGA. The FPGA is configured when the progress bar reaches 100%.
Understanding the Factory Design

In the factory design, two sine waves are generated by two instances of the Altera numerically controlled oscillator (NCO) MegaCore. One of these oscillators is running at 10 times the frequency of the other, but both of them have the same amplitude, each covering 13 bits of dynamic range. The two sine waves output from these blocks are converted from two’s complement binary to unsigned binary format. They are then added together. This combined sine wave signal of 14-bits dynamic range is sent to a 14-bit D/A converter. The analog output of a D/A converter is connected, by means of the included SMA cable, with the analog input of a 14-bit A/D converter. The A/D converter’s digital output is looped back to the Cyclone III device. The A/D is configured by the dip switches to deliver the data in unsigned format. The converted loopback data is captured by an instance of the SignalTap® II logic analyzer in the design for display and analysis.

Figure 5–1 shows a high-level view of the factory design and how it interacts with the D/A and A/D converters on the Data Conversion HSMC in the following sections.

![Factory Design Functional Block Diagram](image)

The design files for the factory design are installed from the DSP Development Kit, Cyclone III Edition CD-ROM in the directory: `<path>kits\cycloneIII_3c120_dsp\examples\cycloneIII_3c120_dsp_example_ChA.`
Exercising the A/D and D/A Converter Performance Test

To test the A/D and D/A converter performance using the factory design, follow these steps:

1. “Configuring the Board” on page 5–2
2. “Collecting Data Using the SignalTap II Logic Analyzer” on page 5–3
3. “Analyzing the Data in the MATLAB Software” on page 5–4

Configuring the Board

The design you use to perform this tutorial exercise uses the Channel A DAC and the Channel A ADC portions of the board. To complete the circuit from end-to-end, install a link between the output of the Channel A DAC and the input to the Channel A ADC. For this link, use one of the SMA cables provided along with the SLP-50 filter. To configure the board, perform the following steps:

1. Attach the filter to the ADC input at J4.
2. Attach the SMA cable from the filter to the DAC output at J12. This connection is shown in Figure 5–1.

The clocks are jumpered according to the instruction in step 7 in “Powering up the Board” on page 4–1. The system should now be powered up.

3. Start the Quartus II software and follow these steps:
   a. On the File menu, click Open Project.
   b. In the Open Project dialog box, browse to the directory: `<path>`\cycloneIII_3c120_dsp\examples\cycloneIII_3c120_dsp_example_ChA
   c. Select cycloneIII_3c120_dsp_factory_design_loopback.qpf, which contains project definitions for reference design, and click Open.
   d. The Signal Tap II file (.stp) provided with the design, sines.stp, is also required. Choose Open (File menu), select Signal Tap II Logic Analyzer Files (*.stp) from the Files of type box, select sines.stp, and click Open.

Figure 5–2 shows sines.stp displayed in the SignalTap II logic analyzer. You can click the “+” sign for the displayed waveform and observe the incoming data stream. Click the “–” sign to collapse the display after you are done so that the analysis shows correctly.
If you modify and recompile the design, specify your new .sof and click **Program Device** in the SignalTap II window to configure the device with your .sof.

### Collecting Data Using the SignalTap II Logic Analyzer

To collect data from the design for analysis, follow these steps.

1. Download the design in the FPGA using the programmer. In the SignalTap window, click this icon ![icon](image) to configure the FPGA.

2. In the **Instance Manager** section of the SignalTap II window, click **Run Analysis** and scroll through the window to observe the following:
   a. Observe the D/A converter output on `da[13..0]`. It shows the combination of the two sine waves, `sin_out[12..0]` and `sin10_out[12..0].`
   b. Observe the A/D converter input of the signal looped back from the D/A on `db[13..0]`. It shows an attenuated combination of two sine waves.

   ![Diagram](image)

   The A/D converter output is attenuated because of losses in the analog circuitry and transformers on the board.
3. On the File menu, select **Create SignalTap II List File** and click **Create/Update**. The Quartus II software generates the file `sines_auto_signaltap_0.txt` in the project directory.

**Analyzing the Data in the MATLAB Software**

To analyze the spectrum content of the data from `sines_auto_signaltap_0.txt` MATLAB, follow these steps:

1. First install MATLAB, which is provided in the kit on an evaluation CD from Mathworks.
2. Start the MATLAB software.
3. Browse to the working directory.
4. To analyze the spectrum of the combined signal output to the D/A converter, perform the following steps:
   a. In the MATLAB Command Window, type the following command:
      ```matlab
      Fir_plot('sines_auto_signaltap_0.txt','a')
      ```
   b. The MATLAB software opens a display window and displays a normalized plot of the DAC CHANNEL A output similar to that shown in Figure 5–3.

   The plotted graph of the peak spur level is below 80 db. A normalized.

**Figure 5–3. Normalized Spectral Plot of 14-bit Output to the Channel A D/A Converter**

![Normalized Spectral Plot](image-url)
5. To analyze the spectrum of the combined signal through the system from the output to the D/A converter back to the input from the A/D converter, perform the following steps:

a. In the MATLAB Command Window, type the following command:
   \[ \text{sines} \_\text{plot('sines\_auto\_signaltap\_0.txt', 'b')} \]

b. The MATLAB software opens a display window and displays a normalized plot of the ADC CHANNEL A input similar to that shown in Figure 5–4. The plot represents the resulting signal with all of the system noise and attenuation.

**Figure 5–4.** Normalized Spectral Plot of 14-bit ADC Channel A Output Data

6. To analyze the final spectrum from the output of the 3-MHz FIR filter, in the MATLAB Command Window, type the following command:
   \[ \text{sines} \_\text{plot('sines\_auto\_signaltap\_0.txt', 'c')} \]

The MATLAB software opens a display window and displays a normalized plot of the output of the 3-MHz FIR filter (Figure 5–5).
Conclusion

This user guide walks you through the software installation process, helps you obtain the license for the DSP Development Kit, Cyclone III Edition and other software and provide information about board setup, configuration, and testing of the Cyclone III DSP development board.
A. Programming the Flash Device

Overview

There is a Common Flash Interface (CFI) type flash memory device on the Cyclone III development board. When you first receive the kit, this CFI flash device arrives programmed with a default factory configuration that was loaded from a Programmer Object File (.pof).

When you power up the board, the CFI flash device configures the FPGA with the default factory configuration using Passive Serial (PS) programming. If the configuration loads correctly, the user LEDs on the board flash sequentially from side to side.

As you develop your own project using the Altera tools, you may wish to program the flash device so that, upon power up, it loads the FPGA with your own design. Or you may wish to restore the default factory configuration to your board.

This appendix describes how to program the flash device. You can load an existing design from a .pof, but if your design exists only as an SRAM Object File (.sof), then you must first convert the .sof to a .pof. Programming the flash device also requires the use of the Altera parallel flash loader (PFL). Using this appendix, you can do the following:

- Create a flash file by converting a .sof to .pof
- Install the PFL
- Use the Quartus II Programmer to write a .pof to the flash device
- Restore the default factory configuration

Creating a Flash File

To create a flash-programmable configuration .pof, perform the following steps:

1. On the File menu in the Quartus II software, click Convert Programming Files.
2. In the Convert Programming Files dialog box, select the parameter values shown in the following table:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Programming file type</td>
<td>Programmer Object File (.pof)</td>
</tr>
<tr>
<td>Configuration device</td>
<td>CFI_512MB</td>
</tr>
<tr>
<td>Mode</td>
<td>1-bit Passive Serial</td>
</tr>
<tr>
<td>File name</td>
<td>&lt;output_file.pof&gt;</td>
</tr>
<tr>
<td>File name example</td>
<td>This is the default file name. Change this to the file name you wish to use for your application. Save the file in &lt;path&gt;\demos\cycloneIII_3c120_dev_pfl.</td>
</tr>
<tr>
<td>Memory Map File</td>
<td>selected (default)</td>
</tr>
</tbody>
</table>
3. Click **Options**. In the **Options** dialog box, enter \(0\times3\text{FE}0000\) and click **OK**. This action sets the option bit base address for the development kit to the required default, \(0\times3\text{FE}0000\). The option bit sector stores the start address for each page of memory and also stores the Page Valid bits. The Page Valid bits indicate whether each page is successfully programmed.

For more information about option bits and Page Mode Implementation of memory, refer to *AN 386: Using the Parallel Flash Loader with the Quartus II Software*.

4. To select the .sof file you want to convert, select the row labeled **SOF Data** in the **Input files to convert** area, click **Add File**, browse to and select the file you wish to convert, and click **OK**. Figure A–1 shows the **Convert Programming Files** dialog box updated with the factory image your\_design\_name.sof.

If you choose to overwrite an existing .pof file, you receive a warning message.

**Figure A–1. Convert Programming Files Settings**

5. Click **Generate**. Generation takes a short time and it is confirmed by a “Generated… pof successfully” message.

You now have a successfully generated .pof that can be programmed to the flash device to automatically configure the FPGA on your Cyclone III development board.
Parallel Flash Loader Instantiation

The development kit includes a PFL megafunction design, `cycloneIII_3c120_dev_pfl`, in the directory `<path>\demos`. The Quartus II software uses the PFL to write programming files to the flash device, which then loads the FPGA on power up.

To write to a flash device, you must first program the PFL into the FPGA by using the Quartus II software as described in “Programming the Flash Device”, steps 1 through 8.

For more information about the PFL megafunction, refer to *AN 386: Using the Parallel Flash Loader with the Quartus II Software*.

Programming the Flash Device

To program the flash device on the development board, you must first create a `.pof` flash file as described in “Creating a Flash File” on page A–1. The following procedure describes how to program the PFL into the FPGA first and use the PFL to write the `.pof` flash file into the flash device.

To download a configuration bit stream into the flash device, perform the following steps:

1. Ensure that the POWER switch SW2 is in the OFF (or DOWN) position.
2. Verify the switch SW3 and jumper settings shown in Table 4–2 on page 4–5.
3. Connect the USB cable to the USB port on the board.
4. Cycle the POWER switch OFF then ON.
5. On the Tools menu in the Quartus II software, click **Programmer**.
6. Click **Add File** and select `<path>\demos\cycloneIII_3C120_dev_pfl\cycloneIII_3C120_dev_pfl.sof`.
7. Turn on the **Program/Configure** option for the added file.
8. Click **Start** to download the selected configuration file to the FPGA (Figure A–2). The FPGA is configured when the progress bar reaches 100%, after which it is ready to access and program the flash device.
9. Click **Auto Detect**. The EP3C120 device and a child CFI_512MB device appear in the list of devices to be programmed.

10. Double-click the `<File><none>` field of the CFI_512MB row. The **Select New Programming File** dialog box appears. Select the desired `.pof`, in this example the `<output_file>.pof` flash file you created earlier, and click **Open**.

11. Turn on **Page_0** and **OPTION_BITS** options in the **Program/Configure** column that correspond to the CFI_512MB device (Figure A–3). This action results in writes only to the flash page zero and the option bit register.

12. Click **Start**. The message window details the flash writing progress to successful completion. Flash writing to one page, as in this case, can take five to six minutes.

You have now successfully programmed the flash device with a configuration for your board. To configure the board from the flash device, power cycle the board as described in “Powering up the Board” on page 4–1.

Powering on the board causes the flash device to load a new configuration into the FPGA device. The Configuration Done LED lights up and the hardware functions associated with the design take effect.
Restoring the Factory Design to the Flash Device

To restore the development board to factory conditions, repeat the steps for writing a new POF to the flash device as described in “Programming the Flash Device” on page A–3, except select the cycloneIII_3c120_dev_factory_recovery.pof file.
Revision History

The following table displays the revision history for this user guide.

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Changes Made</th>
</tr>
</thead>
<tbody>
<tr>
<td>August 2008</td>
<td>1.2</td>
<td>■ Updated directory structure in Figure 3–1.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Deleted Figure 3-1 and Figure 4-4.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Updated Figure 4–2 with Analog devices logo removed.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Updated Figure 4–3.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Converted document to new frame template and made textual and style changes.</td>
</tr>
<tr>
<td>March 2008</td>
<td>1.1</td>
<td>Changes to naming conventions of example designs</td>
</tr>
<tr>
<td>February 2008</td>
<td>1.0</td>
<td>First publication</td>
</tr>
</tbody>
</table>

How to Contact Altera

For the most up-to-date information about Altera products, refer to the following table.

<table>
<thead>
<tr>
<th>Contact Note 1</th>
<th>Contact Method</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technical support</td>
<td>Website</td>
<td><a href="http://www.altera.com/support">www.altera.com/support</a></td>
</tr>
<tr>
<td>Technical training</td>
<td>Website</td>
<td><a href="http://www.altera.com/training">www.altera.com/training</a></td>
</tr>
<tr>
<td></td>
<td>Email</td>
<td><a href="mailto:custrain@altera.com">custrain@altera.com</a></td>
</tr>
<tr>
<td>Product literature</td>
<td>Website</td>
<td><a href="http://www.altera.com/literature">www.altera.com/literature</a></td>
</tr>
<tr>
<td>Non-technical support (General)</td>
<td>Email</td>
<td><a href="mailto:nacomp@altera.com">nacomp@altera.com</a></td>
</tr>
<tr>
<td>(Software Licensing)</td>
<td>Email</td>
<td><a href="mailto:authorization@altera.com">authorization@altera.com</a></td>
</tr>
</tbody>
</table>

Note to Table:
(1) You can also contact your local Altera sales office or sales representative.
Typographic Conventions

This document uses the typographic conventions shown in the following table.

<table>
<thead>
<tr>
<th>Visual Cue</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Bold Type with Initial Capital Letters</strong></td>
<td>Command names, dialog box titles, checkbox options, and dialog box options are shown in bold, initial capital letters. Example: <strong>Save As</strong> dialog box.</td>
</tr>
<tr>
<td><strong>bold type</strong></td>
<td>External timing parameters, directory names, project names, disk drive names, file names, file name extensions, and software utility names are shown in bold type. Examples: <strong>fMAX\qdesigns</strong> directory, <strong>d:</strong> drive, <strong>chiptrip.gdf</strong> file.</td>
</tr>
<tr>
<td><strong>Italic Type with Initial Capital Letters</strong></td>
<td>Document titles are shown in italic type with initial capital letters. Example: <em>AN 75: High-Speed Board Design</em>.</td>
</tr>
<tr>
<td><strong>Italic type</strong></td>
<td>Internal timing parameters and variables are shown in italic type. Examples: <strong>fPA</strong>, ( n + 1 ).</td>
</tr>
<tr>
<td>Variable names are enclosed in angle brackets (&lt;&gt; ) and shown in italic type. Example: &lt;file name&gt;, &lt;project name&gt;.pof file.</td>
<td></td>
</tr>
<tr>
<td><strong>Initial Capital Letters</strong></td>
<td>Keyboard keys and menu names are shown with initial capital letters. Examples: Delete key, the Options menu.</td>
</tr>
<tr>
<td>“Subheading Title”</td>
<td>References to sections within a document and titles of on-line help topics are shown in quotation marks. Example: “Typographic Conventions.”</td>
</tr>
<tr>
<td><strong>Courier type</strong></td>
<td>Signal and port names are shown in lowercase Courier type. Examples: data1, tdi, input. Active-low signals are denoted by suffix n, e.g., resetn.</td>
</tr>
<tr>
<td>Anything that must be typed exactly as it appears is shown in Courier type. For example: c:\qdesigns\tutorial\chiptrip.gdf. Also, sections of an actual file, such as a Report File, references to parts of files (e.g., the AHDL keyword <strong>SUBDESIGN</strong>), as well as logic function names (e.g., <strong>TRI</strong>) are shown in Courier.</td>
<td></td>
</tr>
<tr>
<td>1., 2., 3., and a., b., c., etc.</td>
<td>Numbered steps are used in a list of items when the sequence of the items is important, such as the steps listed in a procedure.</td>
</tr>
<tr>
<td>■ ■</td>
<td>Bullets are used in a list of items when the sequence of the items is not important.</td>
</tr>
<tr>
<td>■ ■</td>
<td>The checkmark indicates a procedure that consists of one step only.</td>
</tr>
<tr>
<td>■ ■</td>
<td>The hand points to information that requires special attention.</td>
</tr>
<tr>
<td>CAUTION</td>
<td>A caution calls attention to a condition or possible situation that can damage or destroy the product or the user's work.</td>
</tr>
<tr>
<td>WARNING</td>
<td>A warning calls attention to a condition or possible situation that can cause injury to the user.</td>
</tr>
<tr>
<td>■ ■</td>
<td>The angled arrow indicates you should press the Enter key.</td>
</tr>
<tr>
<td>■ ■</td>
<td>The feet direct you to more information on a particular topic.</td>
</tr>
</tbody>
</table>