Quartus II Software Version 12.0 SP2 Device Support Release Notes

RN-01075

This document provides late-breaking information about device support in the Altera® Quartus® II software version 12.0 SP2. For information about disk space and system requirements, refer to the **readme.txt** file in your **altera/<*version number*>/quartus** directory.

For information about new features, EDA tool version support, and existing and resolved software issues, refer to the *Quartus II Software Release Notes*.

This document contains the following sections:

Device Support and Pin-Out Status

This section contains information about the device support status in the Quartus II software version 12.0 SP2.

Full Device Support

Full compilation, simulation, timing analysis, and programming support is now available for the new devices listed in Table 1.

Table 1. Devices with Full Support

Device Family	Devices	
Arria® V	5AGXFB3ES	5AGXMB3ES
Cyclone® V	5CGXFC7ES	

Table 1. Devices with Full Support (Continued)

Device Family	Devices	
Stratix® V	5SGSMD3	5SGSMD4
	5SGSMD5	5SGTMC5
	5SGTMC7	5SGXEA3
	5SGXEA4	5SGXEA5
	5SGXEA7	5SGXMA3
	5SGXMA4	5SGXMA5
	5SGXMA7	

Advance Device Support

Compilation, simulation, and timing analysis support is provided for the devices listed in Table 2 that will be released in the near future. The Compiler generates pin-out information for these devices in this release, but does not generate programming files.

Table 2. Devices with Advance Support

Device Family	Devices	
Arria V	5AGXBB1	5AGXBB3
	5AGXBB5	5AGXBB7
	5AGXFB1	5AGXFB3
	5AGXFB5	5AGXFB7
	5AGXMB1	5AGXMB3
	5AGXMB5	5AGXMB7
	5AGTFD3	5AGTFD7
	5AGTMD3	
Cyclone V	5CEBA7	5CEBA9
	5CEFA7	5CEFA9
	5CGXBC7	5CGXBC9
	5CGXFC7	5CGXFC9
	5CGTFD7	5CGTFD9
Stratix V	5SGSED6	5SGSED8
	5SGSMD6	5SGSMD8
	5SGXEA9	5SGXEAB
	5SGXEB5	5SGXEB6
	5SGXEB9	5SGXEBB
	5SGXMA3EH29	5SGXMA9
	5SGXMAB	5SGXMB5
	5SGXMB6	5SGXMB9
	5SGXMBB	

Initial Information Device Support

Compilation, simulation, and timing analysis support is provided for the devices listed in Table 3 that will be released in upcoming versions of the Quartus II software. Programming files and pin-out information are not generated for these devices in this release.

Table 3. Devices with Initial Information Support

Device Family	Devices	
Arria V	5AGTMC3	5AGXBA1
	5AGXBA3	5AGXBA5
	5AGXBA7	5AGXFA5
	5AGXFA7	5AGXMA1
	5AGXMA3	5AGXMA5
	5AGXMA7	
Cyclone V	5CSXFC6	

Memory Recommendations

A full installation of the Quartus II software requires up to 10 GB of available disk space on the drive or partition where you are installing the Altera software.

The Quartus II Stand-Alone Programmer requires a minimum of 1 GB of RAM plus additional memory, based on the size and number of **.sof** files and the size and number of devices being configured.

Altera recommends that your system be configured to provide virtual memory equal to the recommended physical RAM that is required to process your design.

Table 4 lists the memory required to process designs targeted for Altera devices.

Table 4. Memory Recommendations

Family	Device	Recommended Physical RAM	
		32-bit	64-bit
Arria GX	EP1AGX20	512 MB	512 MB
	EP1AGX35, EP1AGX50, EP1AGX60	1.0 GB	1.5 GB
	EP1AGX90	1.5 GB	2.0 GB
Arria II GX	EP2AGX45	1.0 GB	1.5 GB
	EP2AGX65	1.5 GB	2.0 GB
	EP2AGX95, EP2AGX125, EP2AGX190	3.0 GB	4.0 GB
	EP2AGX260	4.0 GB	6.0 GB
Arria II GZ	EP2AGZ225	3.0 GB	4.0 GB
	EP2AGZ300	4.0 GB	6.0 GB
	EP2AGZ350	N/A	8.0 GB

Table 4. Memory Recommendations (Continued)

Family	Device	Recommended Physical RAM	
		32-bit	64-bit
Arria V	5AGXA1, 5AGXA3	N/A	4.0 GB
	5AGXA5, 5AGXA7	N/A	6.0 GB
	5AGXB1, 5AGXB3	N/A	8.0 GB
	5AGXB5, 5AGXB7, 5AGTD7	N/A	12.0 GB
Cyclone	All	512 MB	512 MB
Cyclone II	EP2C5, EP2C8, EP2C15, EP2C20	512 MB	512 MB
	EP2C35, EP2C50	1.0 GB	1.5 GB
	EP2C70	1.5 GB	2.0 GB
Cyclone III	EP3C5, EP3C10, EP3C16, EP3C25, EP3C40	512 MB	512 MB
	EP3C55, EP3C80	768 MB	1.0 GB
	EP3C120	1.5 GB	2.0 GB
Cyclone III LS	EP3CLS70, EP3CLS100	1.5 GB	2.0 GB
	EP3CLS150, EP3CLS200	3.0 GB	4.0 GB
Cyclone IV E	EP4CE6, EP4CE10, EP4CE15, EP4CE22, EP4CE30, EP4CE40	512 MB	512 MB
	EP4CE55, EP4CE75	768 MB	1.0 GB
	EP4CE115	1.0 GB	1.5 GB
Cyclone IV GX	EP4CGX15, EP4CGX22, EP4CGX30	512 MB	512 MB
	EP4CGX50, EP4CGX75	1.0 GB	1.5 GB
	EP4CGX110, EP4CGX150	1.5 GB	2.0 GB
Cyclone V	5CEA7, 5CGXC7, 5CGTD7	3.0 GB	4.0 GB
	5CEA9, 5CGXC9, 5CGTD9, 5CSXC6	N/A	8.0 GB
HardCopy® II	HC210, HC210W	1.5 GB	2.0 GB
	HC220, HC230, HC240	3.0 GB	4.0 GB
HardCopy III	HC325	N/A	8.0 GB
	HC335		12.0 GB
HardCopy IV	HC4E25	N/A	8.0 GB
	HC4GX15		12.0 GB
	HC4E35, HC4GX25		16.0 GB
	HC4GX35		20.0 GB

Table 4. Memory Recommendations (Continued)

Family	Device	Recommended Physical RAM	
		32-bit	64-bit
MAX®	All	512 MB	512 MB
MAX II	All	512 MB	512 MB
MAX V	All	512 MB	512 MB
Stratix	EP1S10, EP1S20	512 MB	512 MB
	EP1S25, EP1S30, EP1S40, EP1S60	1.0 GB	1.5 GB
	EP1S80	1.5 GB	2.0 GB
Stratix GX	EP1SGX10	512 MB	512 MB
	EP1SGX25, EP1SGX40	1.0 GB	1.5 GB
Stratix II	EP2S15	512 MB	512 MB
	EP2S30	1.0 GB	1.5 GB
	EP2S60, EP2S90	1.5 GB	2.0 GB
	EP2S130, EP2S180	3.0 GB	4.0 GB
Stratix II GX	EP2SGX30, EP2SGX60	1.0 GB	1.5 GB
	EP2SGX90	1.5 GB	2.0 GB
	EP2SGX130	3.0 GB	4.0 GB
Stratix III	EP3SL50, EP3SE50, EP3SL70	1.0 GB	1.5 GB
	EP3SE80	1.5 GB	2.0 GB
	EP3SL110, EP3SE110, EP3SL150, EP3SL200	3.0 GB	4.0 GB
	EP3SE260, EP3SL340	4.0 GB	6.0 GB
Stratix IV	EP4SGX70	1.5 GB	2.0 GB
	EP4SE230 EP4SGX110, EP4SGX230, EP4S40G2, EP4S100G2	3.0 GB	4.0 GB
	EP4SGX290	4.0 GB	6.0 GB
	EP4SE360 EP4SGX360, EP4S100G3, EP4S100G4	N/A	8.0 GB
	EP4SGX530, EP4SE530, EP4SE820, EP4S40G5, EP4S100G5	N/A	12.0 GB

Table 4. Memory Recommendations (Continued)

Family	Device	Recommended Physical RAM	
		32-bit	64-bit
Stratix V	5SGXA3, 5SGXA4, 5SGSD3, 5SGSD4, 5SGTC5	N/A	12.0 GB
	5SGXA5, 5SGXB5, 5SGSD5	N/A	16.0 GB
	5SGXA7, 5SGXB6, 5SGSD6, 5SGSD8, 5SGTC7	N/A	20.0 GB
	5SGXA9, 5SGXAB	N/A	24.0 GB
	5SEE9, 5SEEB	N/A	28.0 GB
	5SGXB9, 5SGXBB	N/A	32.0 GB

Timing and Power Models

Table 5 lists a summary of timing and power model status in the current version of the Quartus II software.

Table 5. Devices with Timing and Power Models

Device Family	Device	Timing Model Status	Power Model Status
Arria II GX	EP2AGX45	Final – 10.0	Final – 10.0
	EP2AGX65		
	EP2AGX95		
	EP2AGX125		
	EP2AGX190	Final – 10.0 SP1	
	EP2AGX260		
Arria II GZ	All	Final – 10.1	Final – 10.1
Arria V	All	Preliminary	Preliminary
Cyclone III LS	EPC3LS70	Final – 10.0	Final – 10.0 SP1
	EPC3LS100		
	EPC3LS150		
	EPC3LS200		
Cyclone IV E	All 1.0V	Final – 10.0 SP1	Final – 10.0 SP1
	All 1.2V	Final – 10.0	
Cyclone IV GX	EP4CGX15	Final – 10.1	Final – 11.0
	EP4CGX22	Final – 11.0	
	EP4CGX30		Final – *(1)*
	EP4CGX50	Final – 11.0	Final –11.1
	EP4CGX75		
	EP4CGX110	Final – 10.1	Final – 11.0
	EP4CGX150		

Table 5. Devices with Timing and Power Models (Continued)

Device Family	Device	Timing Model Status	Power Model Status
Cyclone V	All	Preliminary	Preliminary
HardCopy III	All	Correlated – 11.1	Correlated – 12.0
HardCopy IV E	All	Correlated – 11.1	Correlated – 12.0
HardCopy IV GX	All	Correlated – 11.1	Correlated – 12.0
MAX V	All	Final – 11.0	Final – 11.0
Stratix IV	EP4SE230	Final – 9.1 SP1 *(2)*	Final – 10.0
	EP4SGX180		
	EP4SGX230		
	EP4S40G2		
	EP4S100G2		
	EP4SE360	Final – 9.1 SP2 *(2)*	
	EP4SE530		
	EP4SGX290		
	EP4SGX360		
	EP4SGX530		
	EP4S40G5		
	EP4S100G3		
	EP4S100G4		
	EP4S100G5		
	EP4SGX70	Final – 10.0 *(2)*	Final – 10.1
	EP4SGX110		
	EP4SE820	Final – 10.0 SP1	
Stratix V	All	Preliminary	Preliminary

Notes to Table 5:

(1) EP4CGX30BF14 and EP4CGX30CF19 are final in 11.0, EP4CGX30CF23 final in 11.1.

(2) The timing is updated for PMA Direct transceiver timing in Quartus II software release 12.0.

The current version of the Quartus II software also includes final timing and power models for the Arria GX, Cyclone, Cyclone II, Cyclone III, HardCopy II, MAX, MAX II, MAX IIZ, Stratix, Stratix GX, Stratix II, Stratix II GX, and Stratix III device families. Timing models for these device families became final in the Quartus II software versions 9.0 and earlier.

Changes in Device Support

The following section is divided into device support changes according to whether the change is a notification, or whether the change has been fixed or not fixed.

Change Notifications

This section provides notifications for changes to devices.

Device Support Not Fixed

For the latest known issues related to the Quartus II software, refer to the Knowledge Base: http://www.altera.com/support/kdb/kdb-search.jsp

Negative pin location assignments not supported for MAX V LVDS pair

Description

The Quartus II software does not support pin location assignments for the negative pin of an LVDS pair for MAX V devices.

Workaround

Assign positive pins.

Applies to MAX V devices

Quartus II software restricting ATX PLL range issue

Description

The Quartus II software does not restrict the ATX PLL range to the current performance specifications, which are documented in the current *errata sheet* for Stratix V devices on the Altera website. The Quartus II software assumes that all the ATX PLLs have exactly the same data rate performance. Therefore it is possible for the Fitter to implement an ATX PLL with settings outside the performance specifications of your selected device and assigned ATX PLL location.

Workaround

Ensure that your design compiles with the specifications in the errata sheet. You may need to manually assign ATX PLLs in your design to specific locations.

Applies to all Stratix V devices

Device Support Fixed

This section provides details for device support that has been fixed.

Stratix V voltage support is incorrect

Description

In the Quartus II software versions 12.0 and 12.0 SP1, the voltage reported in the reports such as the TimeQuest reports and the Fitter report is incorrect for Stratix V speed grade C2. The reports show 850 mV when they should show 900 mV.

The issue is resolved in the Quartus II software version 12.0 SP2.

Applies to Stratix V devices.

Stratix V clock pin migration issue

Description

When migrating between 5SGXA5 or 5SGXA7 and 5SGXA9 or 5SGSAB devices, the Quartus II software is unable to determine whether the clock connectivity on the migration device is legal. The Quartus II software cannot verify that the guidelines are being correctly followed, which are described in the Stratix V Handbook chapter titled "*Clock Networks and PLLs in Stratix V Devices*".

Workaround

To verify migration compatibility, compile the design for each migration device using the same fixed pin assignments.

The issue is resolved in the Quartus II software version 12.0 SP2.

Applies to Stratix V devices

OE delay chain offset issue

Description

The Quartus II software fails to set the delay chain offset if:

- You have not defined a timing constraint on the output pin, or
- The data on the pin is connected to VCC/GND, and OE path is not I/O registered.

In power-up mode, you may observe glitches on the I/O pins. The issue is resolved in the Quartus II software version 12.0 SP1.

Applies to Arria V, Cyclone V, and Stratix V devices

Incorrect merging of TX PLLs for Arria V GT channels

Description

10G PMA Direct channels can be driven only by a TX PLL within the same triplet, but the Fitter automatically merges the TX PLLs within each six pack. This causes a TX PLL to drive data channels beyond the same triplet.

Workaround

To prevent the TX PLLs from merging incorrectly, use location assignments to constrain the locations of the TX PLLs, so that they always stay within the same triplet as the data channel that they are driving.

The location of the PLLs can be found in the Chip Planner. The TX PLL should be assigned to the central channel of a triplet.

Applies to Arria V GT devices

Stratix IV PMA Direct transceiver timing

Description

The Stratix IV timing model has changed in the Quartus II software version 12.0 to update the delay model for PMA Direct transceiver interfaces.

The issue affects designs that use the ALTGX Megafunction transceiver mode "Basic (PMA Direct)" in the transmitter. This mode uses a direct core-to-PMA register transfer on the transmit side, instead of using the hard PCS logic and phase-compensation FIFO.

The incorrect timing models in the Quartus II software version 11.1 SP2 and earlier may result in hardware errors (increased bit error rates or BER) for designs that have low timing margin on the affected timing path, especially at high temperature and low core voltage.

Workaround

Refer to the following Knowledge Base solution:
www.altera.com/support/kdb/solutions/rd04172012_965.html

Applies to Stratix IV devices

Stratix V VCCHIP power optimization

Description

For lower power consumption through VCCHIP pins, target a Stratix V production (non-ES) part and do not reference an ES part in the migration list. The VCCHIP pins must be powered up for ES parts, but not for production parts. To support pinout migration, the Quartus II software indicates that the VCCHIP pins must be powered when an ES device is used or when an ES device is included in the migration list. For more information please refer to the Stratix® V E, GS, and GX *"Device Family Pin Connection Guidelines"* on the Altera website.

Applies to Stratix V devices