Section III. I/O Standards

This section provides information on Stratix® II single-ended, voltage-referenced, and differential I/O standards.

This section contains the following chapters:

- Chapter 4, Selectable I/O Standards in Stratix II and Stratix II GX Devices
- Chapter 5, High-Speed Differential I/O Interfaces with DPA in Stratix II & Stratix II GX Devices

Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the full handbook.

4. Selectable I/O Standards in Stratix II and Stratix II GX Devices

SII52004-4.6

Introduction

This chapter provides guidelines for using industry I/O standards in Stratix® II and Stratix II GX devices, including:

- I/O features
- I/O standards
- External memory interfaces
- I/O banks
- Design considerations

Stratix II and Stratix II GX I/O Features

Stratix II and the Stratix II GX devices contain an abundance of adaptive logic modules (ALMs), embedded memory, high-bandwidth digital signal processing (DSP) blocks, and extensive routing resources, all of which can operate at very high core speed.

Stratix II and Stratix II GX devices I/O structure is designed to ensure that these internal capabilities are fully utilized. There are numerous I/O features to assist in high-speed data transfer into and out of the device including:

- Single-ended, non-voltage-referenced and voltage-referenced I/O standards
- High-speed differential I/O standards featuring serializer/deserializer (SERDES), dynamic phase alignment (DPA), capable of 1 gigabit per second (Gbps) performance for low-voltage differential signaling (LVDS), Hypertransport technology, HSTL, SSTL, and LVPECL

  HSTL and SSTL I/O standards are used only for PLL clock inputs and outputs in differential mode. LVPECL is supported on clock input and outputs of the top and bottom I/O banks.

- Double data rate (DDR) I/O pins
- Programmable output drive strength for voltage-referenced and non-voltage-referenced single-ended I/O standards
- Programmable bus-hold
- Programmable pull-up resistor
- Open-drain output
- On-chip series termination
- On-chip parallel termination

- On-chip differential termination
- Peripheral component interconnect (PCI) clamping diode
- Hot socketing

For a detailed description of each I/O feature, refer to the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook* or the *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*.

Stratix II and Stratix II GX I/O Standards Support

Stratix II and Stratix II GX devices support a wide range of industry I/O standards. Table 4–1 shows which I/O standards Stratix II devices support as well as typical applications.

Table 4–1. Stratix II and Stratix II GX I/O Standard Applications (Part 1 of 2)

I/O Standard	Application
LVTTL	General purpose
LVCMOS	General purpose
2.5 V	General purpose
1.8 V	General purpose
1.5 V	General purpose
3.3-V PCI	PC and embedded system
3.3-V PCI-X	PC and embedded system
SSTL-2 Class I	DDR SDRAM
SSTL-2 Class II	DDR SDRAM
SSTL-18 Class I	DDR2 SDRAM
SSTL-18 Class II	DDR2 SDRAM
1.8-V HSTL Class I	QDRII SRAM/RLDRAM II/SRAM
1.8-V HSTL Class II	QDRII SRAM/RLDRAM II/SRAM
1.5-V HSTL Class I	QDRII SRAM/SRAM
1.5-V HSTL Class II	QDRII SRAM/SRAM
1.2-V HSTL	General purpose
Differential SSTL-2 Class I	DDR SDRAM
Differential SSTL-2 Class II	DDR SDRAM
Differential SSTL-18 Class I	DDR2 SDRAM
Differential SSTL-18 Class II	DDR2 SDRAM
1.8-V differential HSTL Class I	Clock interfaces
1.8-V differential HSTL Class II	Clock interfaces
1.5-V differential HSTL Class I	Clock interfaces

Table 4–1. Stratix II and Stratix II GX I/O Standard Applications (Part 2 of 2)

I/O Standard	Application
1.5-V differential HSTL Class II	Clock interfaces
LVDS	High-speed communications
HyperTransport™ technology	PCB interfaces
Differential LVPECL	Video graphics and clock distribution

Single-Ended I/O Standards

In non-voltage-referenced single-ended I/O standards, the voltage at the input must be above a set voltage to be considered "on" (high, or logic value 1) or below another voltage to be considered "off" (low, or logic value 0). Voltages between the limits are undefined logically, and may fall into either a logic value 0 or 1. The non-voltage-referenced single-ended I/O standards supported by Stratix II and Stratix II GX devices are:

- Low-voltage transistor-transistor logic (LVTTL)
- Low-voltage complementary metal-oxide semiconductor (LVCMOS)
- 1.5 V
- 1.8 V
- 2.5 V
- 3.3-V PCI
- 3.3-V PCI-X

Voltage-referenced, single-ended I/O standards provide faster data rates. These standards use a constant reference voltage at the input levels. The incoming signals are compared with this constant voltage and the difference between the two defines "on" and "off" states.

Stratix II and Stratix II GX devices support stub series terminated logic (SSTL) and high-speed transceiver logic (HSTL) voltage-referenced I/O standards.

LVTTL

The LVTTL standard is formulated under EIA/JEDEC Standard, JESD8-B (Revision of JESD8-A): Interface Standard for Nominal 3-V/3.3-V Supply Digital Integrated Circuits.

The standard defines DC interface parameters for digital circuits operating from a 3.0- or 3.3-V power supply and driving or being driven by LVTTL-compatible devices. The 3.3-V LVTTL standard is a

general-purpose, single-ended standard used for 3.3-V applications. This I/O standard does not require input reference voltages (V_{REF}) or termination voltages (V_{TT}).

Stratix II and Stratix II GX devices support both input and output levels for 3.3-V LVTTL operation.

Stratix II Stratix II GX devices support a V_{CCIO} voltage level of 3.3 V ±5% as specified as the narrow range for the voltage supply by the EIA/JEDEC standard.

LVCMOS

The LVCMOS standard is formulated under EIA/JEDEC Standard, JESD8-B (Revision of JESD8-A): Interface Standard for Nominal 3-V/3.3-V Supply Digital Integrated Circuits.

The standard defines DC interface parameters for digital circuits operating from a 3.0- or 3.3-V power supply and driving or being driven by LVCMOS-compatible devices. The 3.3-V LVCMOS I/O standard is a general-purpose, single-ended standard used for 3.3-V applications. While LVCMOS has its own output specification, it specifies the same input voltage requirements as LVTTL. These I/O standards do not require V_{REF} or V_{TT}.

Stratix II and Stratix II GX devices support both input and output levels for 3.3-V LVCMOS operation.

Stratix II and Stratix II GX devices support a V_{CCIO} voltage level of 3.3 V ±5% as specified as the narrow range for the voltage supply by the EIA/JEDEC standard.

2.5 V

The 2.5-V I/O standard is formulated under EIA/JEDEC Standard, EIA/JESD8-5: 2.5-V± 0.2-V (Normal Range), and 1.8-V – 2.7-V (Wide Range) Power Supply Voltage and Interface Standard for Non-Terminated Digital Integrated Circuit.

The standard defines the DC interface parameters for high-speed, low-voltage, non-terminated digital circuits driving or being driven by other 2.5-V devices. This standard is a general-purpose, single-ended standard used for 2.5-V applications. It does not require the use of a V_{REF} or a V_{TT}.

Stratix II and Stratix II GX devices support both input and output levels for 2.5-V operation with V_{CCIO} voltage level support of 2.5 V ± 5%, which is narrower than defined in the Normal Range of the EIA/JEDEC standard.

1.8 V

The 1.8-V I/O standard is formulated under EIA/JEDEC Standard, EIA/JESD8-7: 1.8-V± 0.15-V (Normal Range), and 1.2-V – 1.95-V (Wide Range) Power Supply Voltage and Interface Standard for Non-Terminated Digital Integrated Circuit.

The standard defines the DC interface parameters for high-speed, low-voltage, non-terminated digital circuits driving or being driven by other 1.8-V devices. This standard is a general-purpose, single-ended standard used for 1.8-V applications. It does not require the use of a V_{REF} or a V_{TT}.

Stratix II and Stratix II GX devices support both input and output levels for 1.8-V operation with V_{CCIO} voltage level support of 1.8 V ± 5%, which is narrower than defined in the Normal Range of the EIA/JEDEC standard.

1.5 V

The 1.5-V I/O standard is formulated under EIA/JEDEC Standard, JESD8-11: 1.5-V± 0.1-V (Normal Range) and 0.9-V – 1.6-V (Wide Range) Power Supply Voltage and Interface Standard for Non-Terminated Digital Integrated Circuit.

The standard defines the DC interface parameters for high-speed, low-voltage, non-terminated digital circuits driving or being driven by other 1.5-V devices. This standard is a general-purpose, single-ended standard used for 1.5-V applications. It does not require the use of a V_{REF} or a V_{TT}.

Stratix II and Stratix II GX devices support both input and output levels for 1.5-V operation V_{CCIO} voltage level support of 1.5 V ± 5%, which is narrower than defined in the Normal Range of the EIA/JEDEC standard.

3.3-V PCI

The 3.3-V PCI I/O standard is formulated under PCI Local Bus Specification Revision 2.2 developed by the PCI Special Interest Group (SIG).

The PCI local bus specification is used for applications that interface to the PCI local bus, which provides a processor-independent data path between highly integrated peripheral controller components, peripheral add-in boards, and processor/memory systems. The conventional PCI specification revision 2.2 defines the PCI hardware environment including the protocol, electrical, mechanical, and configuration specifications for the PCI devices and expansion boards. This standard requires 3.3-V $V_{CCIO.}$ Stratix II and Stratix II GX devices are fully compliant with the 3.3-V PCI Local Bus Specification Revision 2.2 and meet 64-bit/66-MHz operating frequency and timing requirements.

The 3.3-V PCI standard does not require input reference voltages or board terminations. Stratix II and Stratix II GX devices support both input and output levels.

3.3-V PCI-X

The 3.3-V PCI-X I/O standard is formulated under PCI-X Local Bus Specification Revision 1.0a developed by the PCI SIG.

The PCI-X 1.0 standard is used for applications that interface to the PCI local bus. The standard enables the design of systems and devices that operate at clock speeds up to 133 MHz, or 1 Gbps for a 64-bit bus. The PCI-X 1.0 protocol enhancements enable devices to operate much more efficiently, providing more usable bandwidth at any clock frequency. By using the PCI-X 1.0 standard, you can design devices to meet PCI-X 1.0 requirements and operate as conventional 33- and 66-MHz PCI devices when installed in those systems. This standard requires 3.3-V V_{CCIO}. Stratix II and Stratix II GX devices are fully compliant with the 3.3-V PCI-X Specification Revision 1.0a and meet the 133-MHz operating frequency and timing requirements. The 3.3-V PCI-X standard does not require input reference voltages or board terminations.

Stratix II and Stratix II GX devices support both input and output levels operation.

SSTL-2 Class I and SSTL-2 Class II

The 2.5-V SSTL-2 standard is formulated under JEDEC Standard, JESD8-9A: Stub Series Terminated Logic for 2.5-V (SSTL_2).

The SSTL-2 I/O standard is a 2.5-V memory bus standard used for applications such as high-speed DDR SDRAM interfaces. This standard defines the input and output specifications for devices that operate in the SSTL-2 logic switching range of 0.0 to 2.5 V. This standard improves

operation in conditions where a bus must be isolated from large stubs. SSTL-2 requires a 1.25-V V_{REF} and a 1.25-V V_{TT} to which the series and termination resistors are connected (Figures 4–1 and 4–2).

Stratix II and Stratix II GX devices support both input and output levels operation.

Figure 4–1. 2.5-V SSTL Class I Termination

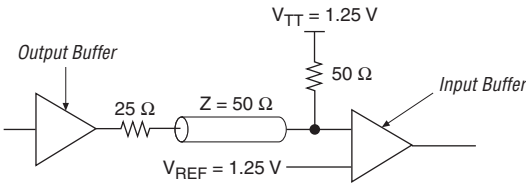
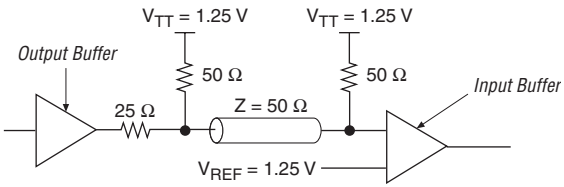


Figure 4–2. 2.5-V SSTL Class II Termination



SSTL-18 Class I and SSTL-18 Class II

The 1.8-V SSTL-18 standard is formulated under JEDEC Standard, JESD8-15: Stub Series Terminated Logic for 1.8-V (SSTL_18).

The SSTL-18 I/O standard is a 1.8-V memory bus standard used for applications such as high-speed DDR2 SDRAM interfaces. This standard is similar to SSTL-2 and defines input and output specifications for devices that are designed to operate in the SSTL-18 logic switching range 0.0 to 1.8 V. SSTL-18 requires a 0.9-V V_{REF} and a 0.9-V V_{TT} to which the series and termination resistors are connected.

There are no class definitions for the SSTL-18 standard in the JEDEC specification. The specification of this I/O standard is based on an environment that consists of both series and parallel terminating resistors. Altera provides solutions to two derived applications in JEDEC specification, and names them Class I and Class II to be consistent with other SSTL standards. Figures 4–3 and 4–4 show SSTL-18 Class I and II termination, respectively.

Stratix II and Stratix II GX devices support both input and output levels operation.

Figure 4–3. 1.8-V SSTL Class I Termination

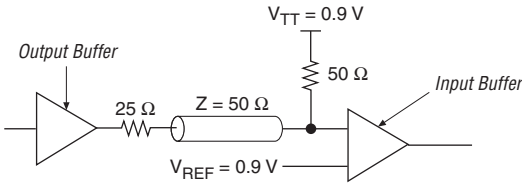
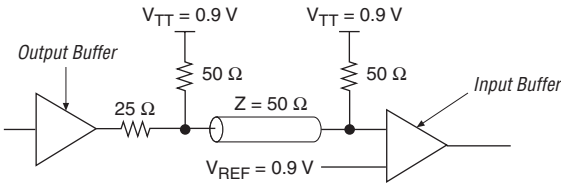


Figure 4–4. 1.8-V SSTL Class II Termination



1.8-V HSTL Class I and 1.8-V HSTL Class II

The HSTL standard is a technology-independent I/O standard developed by JEDEC to provide voltage scalability. It is used for applications designed to operate in the 0.0- to 1.8-V HSTL logic switching range such as quad data rate (QDR) memory clock interfaces.

Although JEDEC specifies a maximum V_{CCIO} value of 1.6 V, there are various memory chip vendors with HSTL standards that require a V_{CCIO} of 1.8 V. Stratix II and Stratix II GX devices support interfaces to chips with V_{CCIO} of 1.8 V for HSTL. Figures 4–5 and 4–6 show the nominal V_{REF} and V_{TT} required to track the higher value of V_{CCIO}. The value of V_{REF} is selected to provide optimum noise margin in the system.

Stratix II and Stratix II GX devices support both input and output levels operation.

Figure 4–5. 1.8-V HSTL Class I Termination

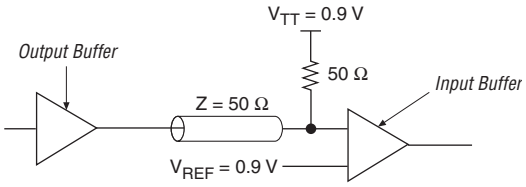
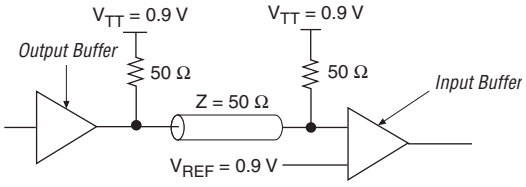


Figure 4–6. 1.8-V HSTL Class II Termination



1.5-V HSTL Class I and 1.5-V HSTL Class II

The 1.5-V HSTL standard is formulated under EIA/JEDEC Standard, EIA/JESD8-6: A 1.5-V Output Buffer Supply Voltage Based Interface Standard for Digital Integrated Circuits.

The 1.5-V HSTL I/O standard is used for applications designed to operate in the 0.0- to 1.5-V HSTL logic nominal switching range. This standard defines single-ended input and output specifications for all HSTL-compliant digital integrated circuits. The 1.5-V HSTL I/O standard in Stratix II and Stratix II GX devices are compatible with the 1.8-V HSTL I/O standard in APEX™ 20KE, APEX 20KC, and in Stratix II and Stratix II GX devices themselves because the input and output voltage thresholds are compatible (Figures 4–7 and 4–8).

Stratix II and Stratix II GX devices support both input and output levels with V_{REF} and V_{TT}.

Figure 4–7. 1.5-V HSTL Class I Termination

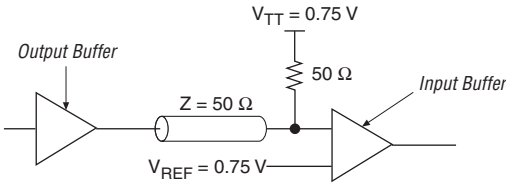
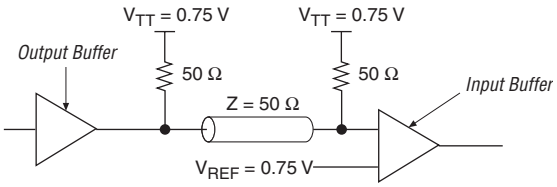


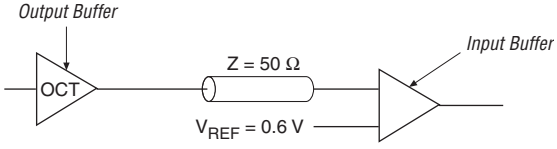
Figure 4–8. 1.5-V HSTL Class II Termination



1.2-V HSTL

Although there is no EIA/JEDEC standard available for the 1.2-V HSTL standard, Altera supports it for applications that operate in the 0.0 to 1.2-V HSTL logic nominal switching range. 1.2-V HSTL can be terminated through series or parallel on-chip termination (OCT). Figure 4–9 shows the termination scheme.

Figure 4–9. 1.2-V HSTL Termination



Differential I/O Standards

Differential I/O standards are used to achieve even faster data rates with higher noise immunity. Apart from LVDS, LVPECL, and HyperTransport technology, Stratix II and Stratix II GX devices also support differential versions of SSTL and HSTL standards.

For detailed information on differential I/O standards, refer to the *High-Speed Differential I/O Interfaces with DPA in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook* or *High-Speed Differential I/O Interfaces with DPA in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook*.

Differential SSTL-2 Class I and Differential SSTL-2 Class II

The 2.5-V differential SSTL-2 standard is formulated under JEDEC Standard, JESD8-9A: Stub Series Terminated Logic for 2.5-V (SSTL_2).

This I/O standard is a 2.5-V standard used for applications such as high-speed DDR SDRAM clock interfaces. This standard supports differential signals in systems using the SSTL-2 standard and supplements the SSTL-2 standard for differential clocks. Stratix II and Stratix II GX devices support both input and output levels. Figures 4–10 and 4–11 shows details on differential SSTL-2 termination.

Stratix II and Stratix II GX devices support differential SSTL-2 I/O standards in pseudo-differential mode, which is implemented by using two SSTL-2 single-ended buffers.

The Quartus® II software only supports pseudo-differential standards on the `INCLK`, `FBIN` and `EXTCLK` ports of enhanced PLL, as well as on DQS pins when DQS megafunction (ALTDQS, Bidirectional Data Strobe) is used. Two single-ended output buffers are automatically programmed to have opposite polarity so as to implement a pseudo-differential output. A proper V_{REF} voltage is required for the two single-ended input buffers to implement a pseudo-differential input. In this case, only the positive polarity input is used in the speed path while the negative input is not connected internally. In other words, only the non-inverted pin is required to be specified in your design, while the Quartus II software automatically generates the inverted pin for you.

Although the Quartus II software does not support pseudo-differential SSTL-2 I/O standards on the left and right I/O banks, you can implement these standards at these banks. You need to create two pins in the designs and configure the pins with single-ended SSTL-2 standards. However, this is limited only to pins that support the differential pin-pair I/O function and is dependent on the single-ended SSTL-2 standards support at these banks.

Figure 4–10. Differential SSTL-2 Class I Termination

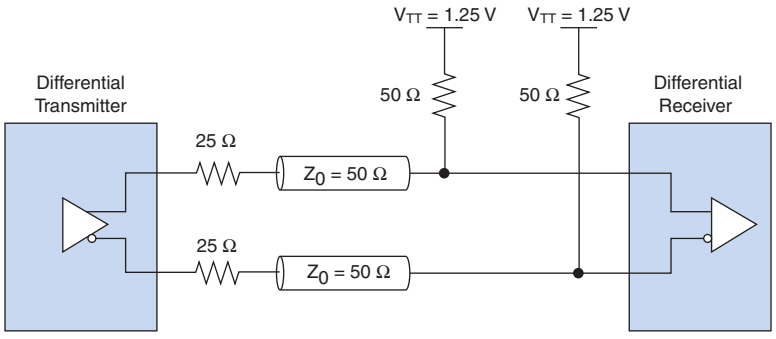
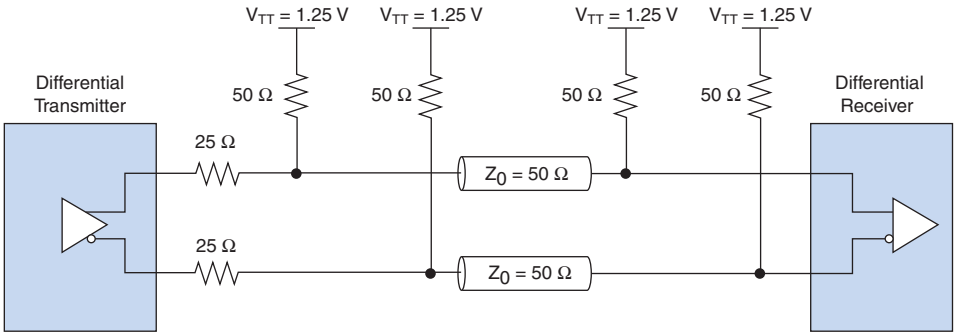


Figure 4–11. Differential SSTL-2 Class II Termination



Differential SSTL-18 Class I and Differential SSTL-18 Class II

The 1.8-V differential SSTL-18 standard is formulated under JEDEC Standard, JESD8-15: Stub Series Terminated Logic for 1.8-V (SSTL_18).

The differential SSTL-18 I/O standard is a 1.8-V standard used for applications such as high-speed DDR2 SDRAM interfaces. This standard supports differential signals in systems using the SSTL-18 standard and supplements the SSTL-18 standard for differential clocks.

Stratix II and Stratix II GX devices support both input and output levels operation.

Figures 4–12 and 4–13 shows details on differential SSTL-18 termination. Stratix II and Stratix II GX devices support differential SSTL-18 I/O standards in pseudo-differential mode, which is implemented by using two SSTL-18 single-ended buffers.

The Quartus II software only supports pseudo-differential standards on the `INCLK`, `FBIN` and `EXTCLK` ports of enhanced PLL, as well as on DQS pins when DQS megafunction (ALTDQS, Bidirectional Data Strobe) is used. Two single-ended output buffers are automatically programmed to have opposite polarity so as to implement a pseudo-differential output. A proper V_{REF} voltage is required for the two single-ended input buffers to implement a pseudo-differential input. In this case, only the positive polarity input is used in the speed path while the negative input is not connected internally. In other words, only the non-inverted pin is required to be specified in your design, while the Quartus II software automatically generates the inverted pin for you.

Although the Quartus II software does not support pseudo-differential SSTL-18 I/O standards on the left and right I/O banks, you can implement these standards at these banks. You need to create two pins in the designs and configure the pins with single-ended SSTL-18 standards. However, this is limited only to pins that support the differential pin-pair I/O function and is dependent on the single-ended SSTL-18 standards support at these banks.

Figure 4–12. Differential SSTL-18 Class I Termination

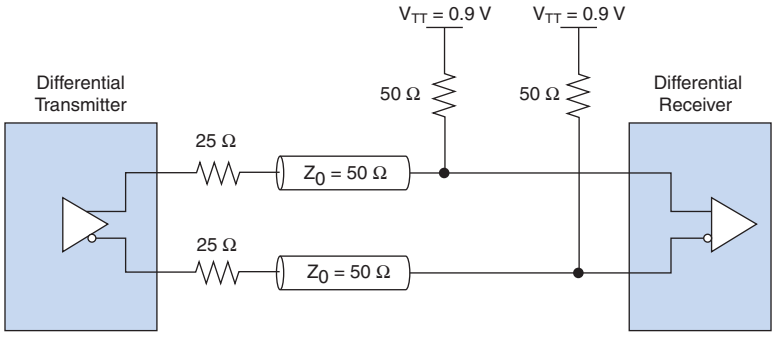
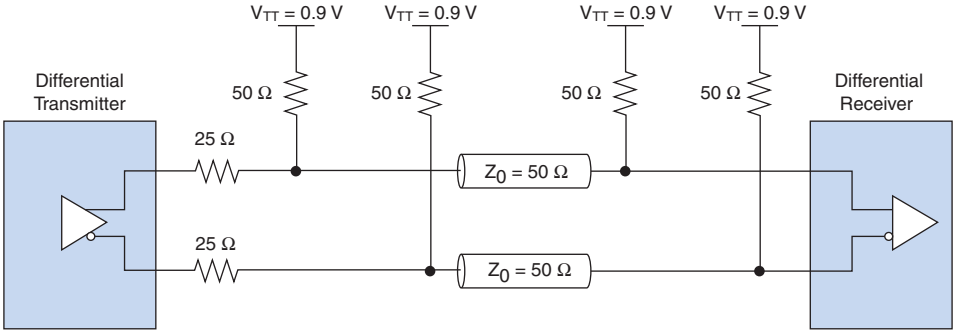


Figure 4–13. Differential SSTL-18 Class II Termination



1.8-V Differential HSTL Class I and 1.8-V Differential HSTL Class II

The 1.8-V differential HSTL specification is the same as the 1.8-V single-ended HSTL specification. It is used for applications designed to operate in the 0.0- to 1.8-V HSTL logic switching range such as QDR memory clock interfaces. Stratix II and Stratix II GX devices support both input and output levels operation. Figures 4–14 and 4–15 show details on 1.8-V differential HSTL termination.

Stratix II and Stratix II GX devices support 1.8-V differential HSTL I/O standards in pseudo-differential mode, which is implemented by using two 1.8-V HSTL single-ended buffers.

The Quartus II software only supports pseudo-differential standards on the `INCLK`, `FBIN` and `EXTCLK` ports of enhanced PLL, as well as on DQS pins when DQS megafunction (ALTDQS, Bidirectional Data Strobe) is used. Two single-ended output buffers are automatically programmed to have opposite polarity so as to implement a pseudo-differential output. A proper V_{REF} voltage is required for the two single-ended input buffers to implement a pseudo-differential input. In this case, only the positive polarity input is used in the speed path while the negative input is not connected internally. In other words, only the non-inverted pin is required to be specified in your design, while the Quartus II software automatically generates the inverted pin for you.

Although the Quartus II software does not support 1.8-V pseudo-differential HSTL I/O standards on left/right I/O banks, you can implement these standards at these banks. You need to create two pins in the designs and configure the pins with single-ended 1.8-V HSTL standards. However, this is limited only to pins that support the differential pin-pair I/O function and is dependent on the single-ended 1.8-V HSTL standards support at these banks.

Figure 4–14. 1.8-V Differential HSTL Class I Termination

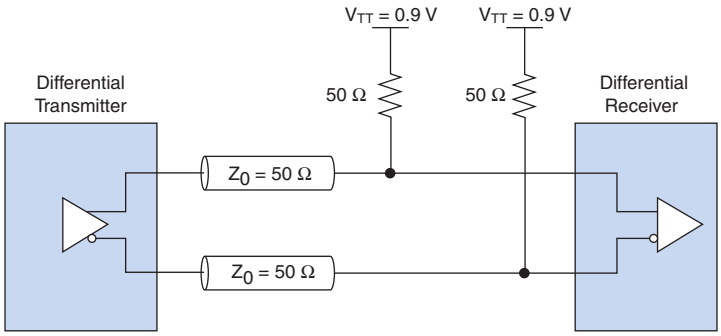
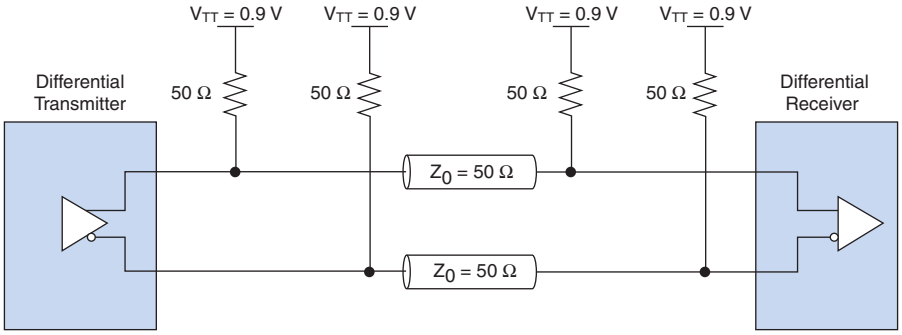


Figure 4–15. 1.8-V Differential HSTL Class II Termination



1.5-V Differential HSTL Class I and 1.5-V Differential HSTL Class II

The 1.5-V differential HSTL standard is formulated under EIA/JEDEC Standard, EIA/JESD8-6: A 1.5-V Output Buffer Supply Voltage Based Interface Standard for Digital Integrated Circuits.

The 1.5-V differential HSTL specification is the same as the 1.5-V single-ended HSTL specification. It is used for applications designed to operate in the 0.0- to 1.5-V HSTL logic switching range, such as QDR memory clock interfaces. Stratix II and Stratix II GX devices support both input and output levels operation. Figures 4–16 and 4–17 show details on the 1.5-V differential HSTL termination.

Stratix II and Stratix II GX devices support 1.5-V differential HSTL I/O standards in pseudo-differential mode, which is implemented by using two 1.5-V HSTL single-ended buffers.

The Quartus II software only supports pseudo-differential standards on the INCLK, FBIN and EXTCLK ports of enhanced PLL, as well as on DQS pins when DQS megafunction (ALTDQS, Bidirectional Data Strobe) is used. Two single-ended output buffers are automatically programmed to have opposite polarity so as to implement a pseudo-differential output. A proper V_{REF} voltage is required for the two single-ended input buffers to implement a pseudo-differential input. In this case, only the positive polarity input is used in the speed path while the negative input is not connected internally. In other words, only the non-inverted pin is required to be specified in your design, while the Quartus II software automatically generates the inverted pin for you.

Although the Quartus II software does not support 1.5-V pseudo-differential HSTL I/O standards on left/right I/O banks, you can implement these standards at these banks. You need to create two pins in the designs and configure the pins with single-ended 1.5-V HSTL standards. However, this is limited only to pins that support the differential pin-pair I/O function and is dependent on the single-ended 1.8-V HSTL standards support at these banks.

Figure 4–16. 1.5-V Differential HSTL Class I Termination

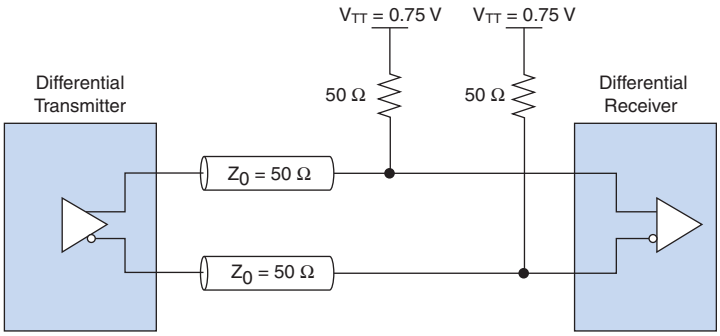
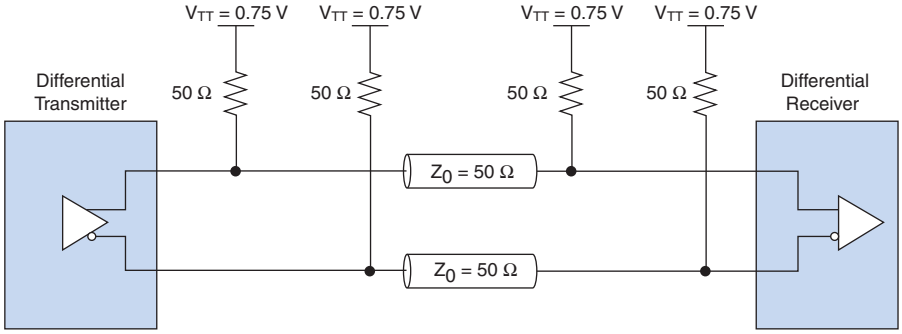


Figure 4–17. 1.5-V Differential HSTL Class II Termination



LVDS

The LVDS standard is formulated under ANSI/TIA/EIA Standard, ANSI/TIA/EIA-644: Electrical Characteristics of Low Voltage Differential Signaling Interface Circuits.

The LVDS I/O standard is a differential high-speed, low-voltage swing, low-power, general-purpose I/O interface standard. In Stratix II devices, the LVDS I/O standard requires a 2.5-V V_{CCIO} level for the side I/O pins in banks 1, 2, 5, and 6. The top and bottom banks have different V_{CCIO} requirements for the LVDS I/O standard. The LVDS clock I/O pins in banks 9 through 12 require a 3.3-V V_{CCIO} level. Within these banks, the `PLL[5,6,11,12]_OUT[1,2]` pins support output only LVDS operations. The `PLL[5,6,11,12]_FB/OUT2` pins support LVDS input or output operations but cannot be configured for bidirectional LVDS operations. The LVDS clock input pins in banks 4, 5, 7, and 8 use V_{CCINT} and have no dependency on the V_{CCIO} voltage level. This standard is used in applications requiring high-bandwidth data transfer, backplane drivers, and clock distribution. The ANSI/TIA/EIA-644 standard specifies LVDS transmitters and receivers capable of operating at recommended maximum data signaling rates of 655 megabit per second (Mbps). However, devices can operate at slower speeds if needed, and there is a theoretical maximum of 1.923 Gbps. Stratix II and Stratix II GX devices are capable of running at a maximum data rate of 1 Gbps and still meet the ANSI/TIA/EIA-644 standard.

Because of the low-voltage swing of the LVDS I/O standard, the electromagnetic interference (EMI) effects are much smaller than complementary metal-oxide semiconductor (CMOS), transistor-to-transistor logic (TTL), and positive (or psuedo) emitter coupled logic (PECL). This low EMI makes LVDS ideal for applications

with low EMI requirements or noise immunity requirements. The LVDS standard does not require an input reference voltage. However, it does require a 100-Ω termination resistor between the two signals at the input buffer. Stratix II and Stratix II GX devices provide an optional 100-Ω differential LVDS termination resistor in the device using on-chip differential termination. Stratix II and Stratix II GX devices support both input and output levels operation.

Differential LVPECL

The low-voltage positive (or pseudo) emitter coupled logic (LVPECL) standard is a differential interface standard requiring a 3.3-V V_{CCIO}. The standard is used in applications involving video graphics, telecommunications, data communications, and clock distribution. The high-speed, low-voltage swing LVPECL I/O standard uses a positive power supply and is similar to LVDS. However, LVPECL has a larger differential output voltage swing than LVDS. The LVPECL standard does not require an input reference voltage, but it does require a 100-Ω termination resistor between the two signals at the input buffer. Figures 4–18 and 4–19 show two alternate termination schemes for LVPECL.

Stratix II and Stratix II GX devices support both input and output levels operation.

Figure 4–18. LVPECL DC Coupled Termination

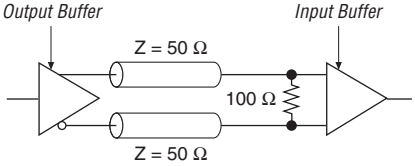
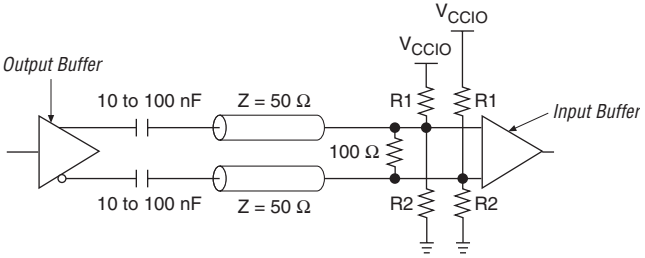


Figure 4–19. LVPECL AC Coupled Termination



HyperTransport Technology

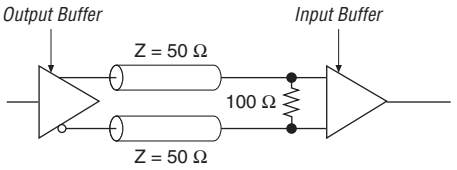
The HyperTransport standard is formulated by the HyperTransport Consortium.

The HyperTransport I/O standard is a differential high-speed, high-performance I/O interface standard requiring a 2.5- or 3.3-V V_{CCIO}. This standard is used in applications such as high-performance networking, telecommunications, embedded systems, consumer electronics, and Internet connectivity devices. The HyperTransport I/O standard is a point-to-point standard in which each HyperTransport bus consists of two point-to-point unidirectional links. Each link is 2 to 32 bits.

The HyperTransport standard does not require an input reference voltage. However, it does require a 100-Ω termination resistor between the two signals at the input buffer. Figure 4–20 shows HyperTransport termination. Stratix II and Stratix II GX devices include an optional 100-Ω differential HyperTransport termination resistor in the device using on-chip differential termination.

Stratix II and Stratix II GX devices support both input and output levels operation.

Figure 4–20. HyperTransport Termination



Stratix II and Stratix II GX External Memory Interface

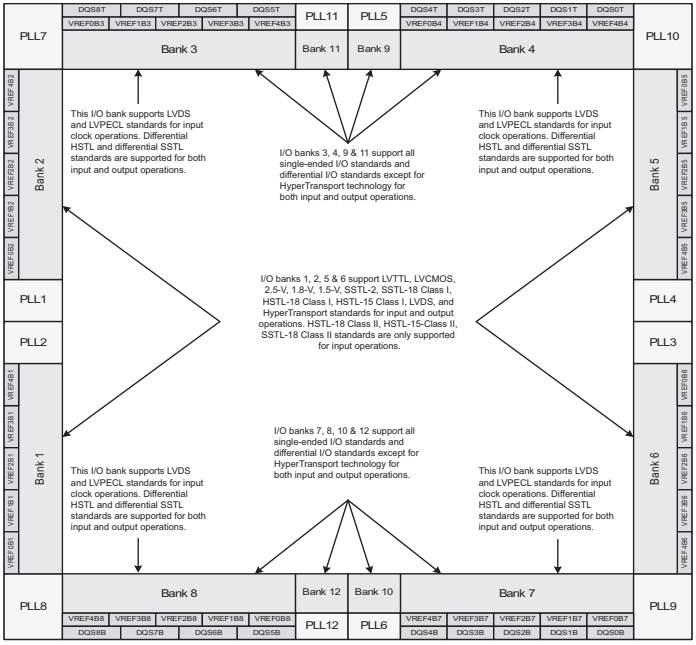
The increasing demand for higher-performance data processing systems often requires memory-intensive applications. Stratix II and Stratix II GX devices can interface with many types of external memory.

Refer to the *External Memory Interfaces in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook* or the *External Memory Interfaces in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook* for more information on the external memory interface support in Stratix II or Stratix II GX devices.

Stratix II and Stratix II GX I/O Banks

Stratix II devices have eight general I/O banks and four enhanced phase-locked loop (PLL) external clock output banks (Figure 4–21). I/O banks 1, 2, 5, and 6 are on the left or right sides of the device and I/O banks 3, 4, and 7 through 12 are at the top or bottom of the device.

Figure 4–21. Stratix II I/O Banks *Notes (1), (2), (3), (4), (5), (6), (7)*



Notes to Figure 4–21:

(1) Figure 4–21 is a top view of the silicon die that corresponds to a reverse view for flip-chip packages. It is a graphical representation only. Refer to the pin list and Quartus II software for exact locations.

(2) Depending on the size of the device, different device members have different numbers of V_{REF} groups.

(3) Banks 9 through 12 are enhanced PLL external clock output banks. These PLL banks utilize the adjacent V_{REF} group when voltage-referenced standards are implemented. For example, if an SSTL input is implemented in PLL bank 10, the voltage level at VREFB7 is the reference voltage level for the SSTL input.

(4) Differential HSTL and differential SSTL standards are available for bidirectional operations on DQS pin and input-only operations on PLL clock input pins; LVDS, LVPECL, and HyperTransport standards are available for input-only operations on PLL clock input pins. Refer to the "Differential I/O Standards" on page 4–10 for more details.

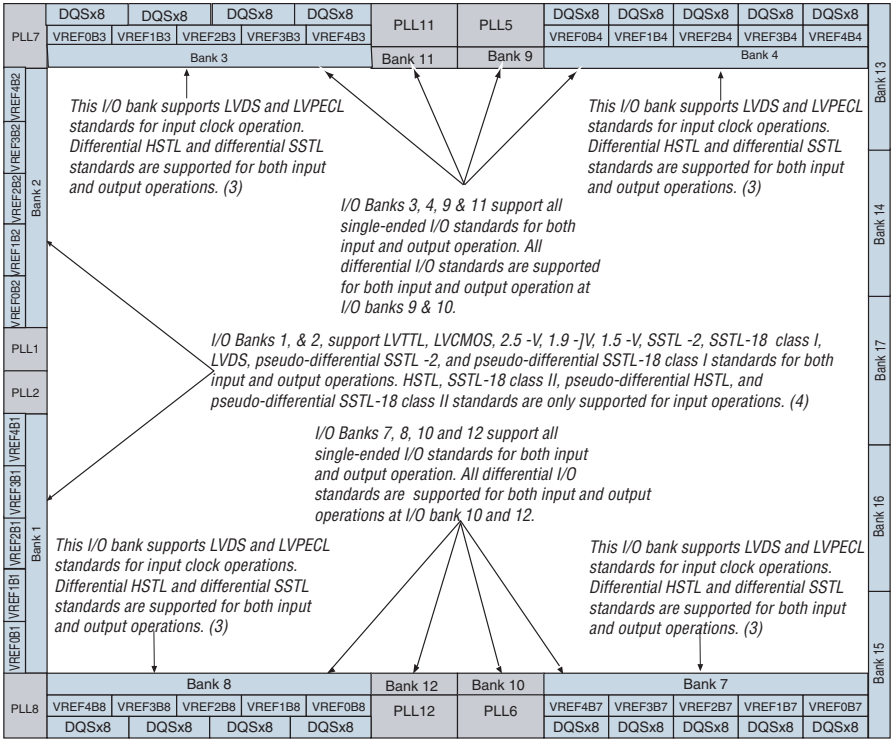
(5) Quartus II software does not support differential SSTL and differential HSTL standards at left/right I/O banks. Refer to the "Differential I/O Standards" on page 4–10 if you need to implement these standards at these I/O banks.

(6) Banks 11 and 12 are available only in EP2S60, EP2S90, EP2S130, and EP2S180 devices.

(7) PLLs 7, 8, 9 10, 11, and 12 are available only in EP2S60, EP2S90, EP2S130, and EP2S180 devices.

Stratix II GX devices have 6 general I/O banks and 4 enhanced phase-locked loop (PLL) external clock output banks (Figure 4–22). I/O banks 9 through 12 are enhanced PLL external clock output banks located on the top and bottom of the device.

Figure 4–22. Stratix II GX I/O Banks *Notes (1), (2), (3), (4)*



Notes to Figure 4–22:

(1) Figure 4–22 is a top view of the silicon die which corresponds to a reverse view for flip-chip packages. It is a graphical representation only.

(2) Depending on size of the device, different device members have different number of V_{REF} groups. Refer to the pin list and the Quartus II software for exact locations.

(3) Banks 9 through 12 are enhanced PLL external clock output banks.

(4) Horizontal I/O banks feature transceiver and DPA circuitry for high speed differential I/O standards. Refer to the *High-Speed Differential I/O Interfaces with DPA in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook*, or the *Stratix II GX Transceiver User Guide* (volume 1) of the *Stratix II GX Device Handbook* for more information on differential I/O standards.

(5) Quartus II software does not support differential SSTL and differential HSTL standards at left/right I/O banks. Refer to the "Differential I/O Standards" on page 4–10 if you need to implement these standards at these I/O banks.

(6) Banks 11 and 12 are available only in EP2SGX60C/D/E, EP2SGX90E/F, and EP2SGX130G.

(7) PLLs 7,8,11, and 12 are available only in EP2SGX60C/D/E, EP2SGXE/F, and EP2SGX130G.

Programmable I/O Standards

Stratix II and Stratix II GX device programmable I/O standards deliver high-speed and high-performance solutions in many complex design systems. This section discusses the I/O standard support in the I/O banks of Stratix II and Stratix II GX devices.

Regular I/O Pins

Most Stratix II and Stratix II GX device pins are multi-function pins. These pins support regular inputs and outputs as their primary function, and offer an optional function such as DQS, differential pin-pair, or PLL external clock outputs. For example, you can configure a multi-function pin in the enhanced PLL external clock output bank as a PLL external clock output when it is not used as a regular I/O pin.

I/O pins that reside in PLL banks 9 through 12 are powered by the VCC_PLL<*5, 6, 11, or 12*>_OUT pins, respectively. The EP2S60F484, EP2S60F780, EP2S90H484, EP2S90F780, and EP2S130F780 devices do not support PLLs 11 and 12. Therefore, any I/O pins that reside in bank 11 are powered by the VCCIO3 pin, and any I/O pins that reside in bank 12 are powered by the VCCIO8 pin.

Table 4–2 shows the I/O standards supported when a pin is used as a regular I/O pin in the I/O banks of Stratix II and Stratix II GX devices.

Table 4–2. Stratix II and Stratix II GX Regular I/O Standards Support (Part 1 of 2)

I/O Standard	General I/O Bank								Enhanced PLL External Clock Output Bank *(2)*			
	1	2	3	4	5*(1)*	6*(1)*	7	8	9	10	11	12
LVTTL	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
LVCMOS	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
2.5 V	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
1.8 V	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
1.5 V	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
3.3-V PCI			✓	✓			✓	✓	✓	✓	✓	✓
3.3-V PCI-X			✓	✓			✓	✓	✓	✓	✓	✓
SSTL-2 Class I	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
SSTL-2 Class II	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Table 4–2. Stratix II and Stratix II GX Regular I/O Standards Support (Part 2 of 2)

I/O Standard	General I/O Bank								Enhanced PLL External Clock Output Bank *(2)*			
	1	2	3	4	5*(1)*	6*(1)*	7	8	9	10	11	12
SSTL-18 Class I	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
SSTL-18 Class II	*(3)*	*(3)*	✓	✓	*(3)*	*(3)*	✓	✓	✓	✓	✓	✓
1.8-V HSTL Class I	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
1.8-V HSTL Class II	*(3)*	*(3)*	✓	✓	*(3)*	*(3)*	✓	✓	✓	✓	✓	✓
1.5-V HSTL Class I	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
1.5-V HSTL Class II	*(3)*	*(3)*	✓	✓	*(3)*	*(3)*	✓	✓	✓	✓	✓	✓
1.2-V HSTL				✓			✓	✓				
Differential SSTL-2 Class I	*(4)*	*(4)*	*(5)*	*(5)*	*(4)*	*(4)*	*(5)*	*(5)*				
Differential SSTL-2 Class II	*(4)*	*(4)*	*(5)*	*(5)*	*(4)*	*(4)*	*(5)*	*(5)*				
Differential SSTL-18 Class I	*(4)*	*(4)*	*(5)*	*(5)*	*(4)*	*(4)*	*(5)*	*(5)*				
Differential SSTL-18 Class II	*(4)*	*(4)*	*(5)*	*(5)*	*(4)*	*(4)*	*(5)*	*(5)*				
1.8-V differential HSTL Class I	*(4)*	*(4)*	*(5)*	*(5)*	*(4)*	*(4)*	*(5)*	*(5)*				
1.8-V differential HSTL Class II	*(4)*	*(4)*	*(5)*	*(5)*	*(4)*	*(4)*	*(5)*	*(5)*				
1.5-V differential HSTL Class I	*(4)*	*(4)*	*(5)*	*(5)*	*(4)*	*(4)*	*(5)*	*(5)*				
1.5-V differential HSTL Class II	*(4)*	*(4)*	*(5)*	*(5)*	*(4)*	*(4)*	*(5)*	*(5)*				
LVDS	✓	✓	*(6)*	*(6)*	✓	✓	*(6)*	*(6)*	✓	✓	✓	✓
HyperTransport technology	✓	✓			✓	✓						
Differential LVPECL			*(6)*	*(6)*			*(6)*	*(6)*	✓	✓	✓	✓

Notes to Table 4–2:

(1) This bank is not available in Stratix II GX Devices.

(2) A mixture of single-ended and differential I/O standards is not allowed in enhanced PLL external clock output bank.

(3) This I/O standard is only supported for the input operation in this I/O bank.

(4) Although the Quartus II software does not support pseudo-differential SSTL/HSTL I/O standards on the left and right I/O banks, you can implement these standards at these banks. Refer to the "Differential I/O Standards" on page 4–10 for details.

(5) This I/O standard is supported for both input and output operations for pins that support the DQS function. Refer to the "Differential I/O Standards" on page 4–10 for details.

(6) This I/O standard is only supported for the input operation for pins that support PLL `INCLK` function in this I/O bank.

Clock I/O Pins

The PLL clock I/O pins consist of clock inputs (INCLK), external feedback inputs (FBIN), and external clock outputs (EXTCLK). Clock inputs are located at the left and right I/O banks (banks 1, 2, 5, and 6) to support fast PLLs, and at the top and bottom I/O banks (banks 3, 4, 7, and 8) to support enhanced PLLs. Both external clock outputs and external feedback inputs are located at enhanced PLL external clock output banks (banks 9, 10, 11, and 12) to support enhanced PLLs. Table 4–3 shows the PLL clock I/O support in the I/O banks of Stratix II and Stratix II GX devices.

Table 4–3. I/O Standards Supported for Stratix II and Stratix II GX PLL Pins (Part 1 of 2)

I/O Standard (2)	Enhanced PLL (1)			Fast PLL
	Input		Output	Input
	INCLK	FBIN	EXTCLK	INCLK
LVTTL	✓	✓	✓	✓
LVCMOS	✓	✓	✓	✓
2.5 V	✓	✓	✓	✓
1.8 V	✓	✓	✓	✓
1.5 V	✓	✓	✓	✓
3.3-V PCI	✓	✓	✓	
3.3-V PCI-X	✓	✓	✓	
SSTL-2 Class I	✓	✓	✓	✓
SSTL-2 Class II	✓	✓	✓	✓
SSTL-18 Class I	✓	✓	✓	✓
SSTL-18 Class II	✓	✓	✓	✓
1.8-V HSTL Class I	✓	✓	✓	✓
1.8-V HSTL Class II	✓	✓	✓	✓
1.5-V HSTL Class I	✓	✓	✓	✓
1.5-V HSTL Class II	✓	✓	✓	✓
Differential SSTL-2 Class I	✓	✓	✓	
Differential SSTL-2 Class II	✓	✓	✓	
Differential SSTL-18 Class I	✓	✓	✓	
Differential SSTL-18 Class II	✓	✓	✓	

Table 4–3. I/O Standards Supported for Stratix II and Stratix II GX PLL Pins (Part 2 of 2)

I/O Standard (2)	Enhanced PLL (1)			Fast PLL
	Input		Output	Input
	INCLK	FBIN	EXTCLK	INCLK
1.8-V differential HSTL Class I	✓	✓	✓	
1.8-V differential HSTL Class II	✓	✓	✓	
1.5-V differential HSTL Class I	✓	✓	✓	
1.5-V differential HSTL Class II	✓	✓	✓	
LVDS	✓	✓	✓	✓
HyperTransport technology				✓
Differential LVPECL	✓	✓	✓	

Note to Table 4–3:
(1) The enhanced PLL external clock output bank does not allow a mixture of both single-ended and differential I/O standards.
(2) Altera does not support 1.2-V HSTL for PLL input pins on column I/O pins.

For more information, refer to the *PLLs in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook* or the *PLLs in Stratix II & Straix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook.*

Voltage Levels

Stratix II device specify a range of allowed voltage levels for supported I/O standards. Table 4–4 shows only typical values for input and output V_{CCIO}, V_{REF}, as well as the board V_{TT}.

Table 4–4. Stratix II and Stratix II GX I/O Standards and Voltage Levels (Part 1 of 3) Note (1)

I/O Standard	Stratix II and Stratix II GX					
	V_{CCIO} (V)				V_{REF} (V)	V_{TT} (V)
	Input Operation		Output Operation			
	Top and Bottom I/O Banks	Left and Right I/O Banks (3)	Top and Bottom I/O Banks	Left and Right I/O Banks (3)	Input	Termination
LVTTL	3.3/2.5	3.3/2.5	3.3	3.3	NA	NA
LVCMOS	3.3/2.5	3.3/2.5	3.3	3.3	NA	NA

Table 4–4. Stratix II and Stratix II GX I/O Standards and Voltage Levels (Part 2 of 3) *Note (1)*

I/O Standard	Stratix II and Stratix II GX					
	V_{CCIO} (V)				V_{REF} (V)	V_{TT} (V)
	Input Operation		Output Operation		Input	Termination
	Top and Bottom I/O Banks	Left and Right I/O Banks *(3)*	Top and Bottom I/O Banks	Left and Right I/O Banks *(3)*		
2.5 V	3.3/2.5	3.3/2.5	2.5	2.5	NA	NA
1.8 V	1.8/1.5	1.8/1.5	1.8	1.8	NA	NA
1.5 V	1.8/1.5	1.8/1.5	1.5	1.5	NA	NA
3.3-V PCI	3.3	NA	3.3	NA	NA	NA
3.3-V PCI-X	3.3	NA	3.3	NA	NA	NA
SSTL-2 Class I	2.5	2.5	2.5	2.5	1.25	1.25
SSTL-2 Class II	2.5	2.5	2.5	2.5	1.25	1.25
SSTL-18 Class I	1.8	1.8	1.8	1.8	0.90	0.90
SSTL-18 Class II	1.8	1.8	1.8	NA	0.90	0.90
1.8-V HSTL Class I	1.8	1.8	1.8	1.8	0.90	0.90
1.8-V HSTL Class II	1.8	1.8	1.8	NA	0.90	0.90
1.5-V HSTL Class I	1.5	1.5	1.5	1.5	0.75	0.75
1.5-V HSTL Class II	1.5	1.5	1.5	NA	0.75	0.75
1.2-V HSTL *(4)*	1.2	NA	1.2	NA	0.6	NA
Differential SSTL-2 Class I	2.5	2.5	2.5	2.5	1.25	1.25
Differential SSTL-2 Class II	2.5	2.5	2.5	2.5	1.25	1.25
Differential SSTL-18 Class I	1.8	1.8	1.8	1.8	0.90	0.90
Differential SSTL-18 Class II	1.8	1.8	1.8	NA	0.90	0.90
1.8-V differential HSTL Class I	1.8	1.8	1.8	NA	0.90	0.90
1.8-V differential HSTL Class II	1.8	1.8	1.8	NA	0.90	0.90
1.5-V differential HSTL Class I	1.5	1.5	1.5	NA	0.75	0.75
1.5-V differential HSTL Class II	1.5	1.5	1.5	NA	0.75	0.75
LVDS *(2)*	3.3/2.5/1.8/1.5	2.5	3.3	2.5	NA	NA

Table 4–4. Stratix II and Stratix II GX I/O Standards and Voltage Levels (Part 3 of 3) *Note (1)*

I/O Standard	Stratix II and Stratix II GX					
	V_{CCIO} (V)				V_{REF} (V)	V_{TT} (V)
	Input Operation		Output Operation		Input	Termination
	Top and Bottom I/O Banks	Left and Right I/O Banks *(3)*	Top and Bottom I/O Banks	Left and Right I/O Banks *(3)*		
HyperTransport technology	NA	2.5	NA	2.5	NA	NA
Differential LVPECL *(2)*	3.3/2.5/1.8/1.5	NA	3.3	NA	NA	NA

Notes to Table 4–4:

(1) Any input pins with PCI-clamping diode will clamp the V_{CCIO} to 3.3 V.

(2) LVDS and LVPECL output operation in the top and bottom banks is only supported in PLL banks 9-12. The V_{CCIO} level for differential output operation in the PLL banks is 3.3 V. The V_{CCIO} level for output operation in the left and right I/O banks is 2.5 V.

(3) The right I/O bank does not apply to the Stratix II GX. The right I/O Bank on Stratix II GX devices consists of transceivers.

(4) 1.2-V HSTL is only supported in I/O banks 4,7, and 8.

Refer to the *DC & Switching Characteristics* chapter in volume 1 of the *Stratix II Device Handbook* or the *DC & Switching Characteristics* chapter in volume 1 of the *Stratix II GX Device Handbook* for detailed electrical characteristics of each I/O standard.

On-Chip Termination

Stratix II and Stratix II GX devices feature on-chip termination to provide I/O impedance matching and termination capabilities. Apart from maintaining signal integrity, this feature also minimizes the need for external resistor networks, thereby saving board space and reducing costs.

Stratix II and Stratix II GX devices support on-chip series (R_S) and parallel (R_T) termination for single-ended I/O standards and on-chip differential termination (R_D) for differential I/O standards. This section discusses the on-chip series termination support.

For more information on differential on-chip termination, Refer to the *High-Speed Differential I/O Interfaces with DPA in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook* or the *High-Speed Differential I/O Interfaces with DPA in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook.*

The Stratix II and Stratix II GX devices supports I/O driver on-chip series (R_S) and parallel (R_T) termination through drive strength control for single-ended I/Os. There are three ways to implement the R_S and (R_T) in Stratix II and Stratix II GX devices:

- R_S without calibration for both row I/Os and column I/Os
- R_S with calibration only for column I/Os
- R_T with calibration only for column I/Os

On-Chip Series Termination without Calibration

Stratix II and Stratix II GX devices support driver impedance matching to provide the I/O driver with controlled output impedance that closely matches the impedance of the transmission line. As a result, reflections can be significantly reduced. Stratix II and Stratix II GX devices support on-chip series termination for single-ended I/O standards (see Figure 4–23). The R_S shown in Figure 4–23 is the intrinsic impedance of transistors. The typical R_S values are 25Ω and 50Ω Once matching impedance is selected, current drive strength is no longer selectable.

On-chip series termination without calibration is supported on output pins or on the output function of bidirectional pins.

Figure 4–23. Stratix II and Stratix II GX On-Chip Series Termination without Calibration

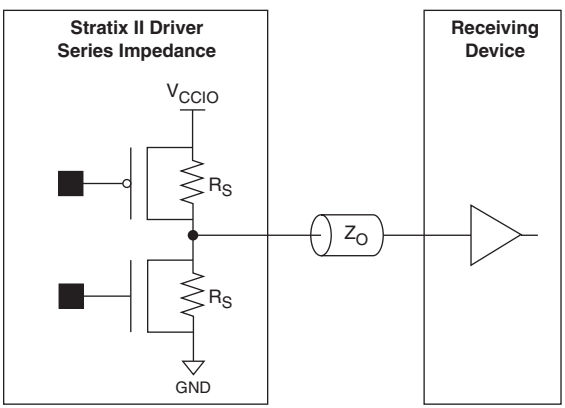


Table 4–5 shows the list of output standards that support on-chip series termination without calibration.

Table 4–5. Selectable I/O Drivers with On-Chip Series Termination without Calibration

I/O Standard	On-chip Series Termination Setting		
	Row I/O	Column I/O	Unit
3.3-V LVTTL	50	50	Ω
	25	25	Ω
3.3-V LVCMOS	50	50	Ω
	25	25	Ω
2.5-V LVTTL	50	50	Ω
	25	25	Ω
2.5-V LVCMOS	50	50	Ω
	25	25	Ω
1.8-V LVTTL	50	50	Ω
		25	Ω
1.8-V LVCMOS	50	50	Ω
		25	Ω
1.5-V LVTTL	50	50	Ω
1.5-V LVCMOS	50	50	Ω
SSTL-2 Class I	50	50	Ω
SSTL-2 Class II	25	25	Ω
SSTL-18 Class I	50	50	Ω
SSTL-18 Class II		25	Ω
1.8-V HSTL Class I	50	50	Ω
1.8-V HSTL Class II		25	Ω
1.5-V HSTL Class I	50	50	Ω
1.2-V HSTL *(1)*		50	Ω

Note to Table 4–5:
(1) 1.2-V HSTL is only supported in I/O banks 4,7, and 8.

To use on-chip termination for the SSTL Class I standard, users should select the 50-Ω on-chip series termination setting for replacing the external 25-Ω R_S (to match the 50-Ω transmission line). For the SSTL Class II standard, users should select the 25-Ω on-chip series termination setting (to match the 50-Ω transmission line and the near end 50-Ω pull-up to V_{TT}).

For more information on tolerance specifications for on-chip termination without calibration, refer to the *DC & Switching Characteristics* chapter in volume 1 of the *Stratix II Device Handbook* or the *DC & Switching Characteristics* chapter in volume 1 of the *Stratix II GX Device Handbook*.

On-Chip Series Termination with Calibration

Stratix II and Stratix II GX devices support on-chip series termination with calibration in column I/Os in top and bottom banks. Every column I/O buffer consists of a group of transistors in parallel. Each transistor can be individually enabled or disabled. The on-chip series termination calibration circuit compares the total impedance of the transistor group to the external 25-Ωor 50-Ωresistors connected to the RUP and RDN pins, and dynamically enables or disables the transistors until they match (as shown in Figure 4–24). The R_S shown in Figure 4–24 is the intrinsic impedance of transistors. Calibration happens at the end of device configuration. Once the calibration circuit finds the correct impedance, it powers down and stops changing the characteristics of the drivers.

On-chip series termination with calibration is supported on output pins or on the output function of bidirectional pins.

Figure 4–24. Stratix II and Stratix II GX On-Chip Series Termination with Calibration

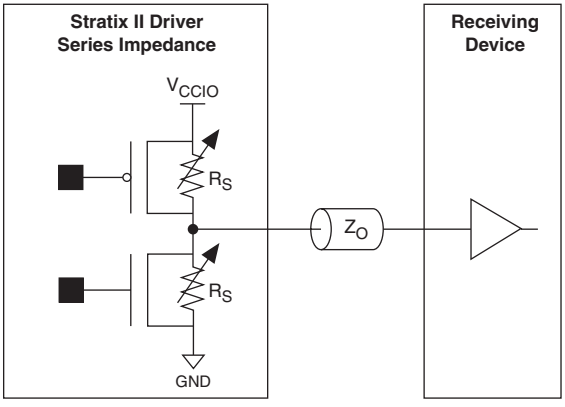


Table 4–6 shows the list of output standards that support on-chip series termination with calibration.

Table 4–6. Selectable I/O Drivers with On-Chip Series Termination with Calibration

I/O Standard	On-Chip Series Termination Setting (Column I/O)	Unit
3.3-V LVTTL	50	Ω
	25	Ω
3.3-V LVCMOS	50	Ω
	25	Ω
2.5-V LVTTL	50	Ω
	25	Ω
2.5-V LVCMOS	50	Ω
	25	Ω
1.8-V LVTTL	50	Ω
	25	Ω
1.8-V LVCMOS	50	Ω
	25	Ω
1.5 LVTTL	50	Ω
1.5 LVCMOS	50	Ω
SSTL-2 Class I	50	Ω
SSTL-2 Class II	25	Ω
SSTL-18 Class I	50	Ω
SSTL-18 Class II	25	Ω
1.8-V HSTL Class I	50	Ω
1.8-V HSTL Class II	25	Ω
1.5-V HSTL Class I	50	Ω
1.2-V HSTL *(1)*	50	Ω

Note to Table 4–6:
(1) 1.2-V HSTL is only supported in I/O banks 4,7, and 8.

On-Chip Parallel Termination with Calibration

Stratix II and Stratix II GX devices support on-chip parallel termination with calibration in column I/Os in top and bottom banks. Every column I/O buffer consists of a group of transistors in parallel. Each transistor can be individually enabled or disabled. The on-chip parallel termination calibration circuit compares the total impedance of the transistor group to

the external 50-Ω resistors connected to the RUP and RDN pins and dynamically enables or disables the transistors until they match. Calibration happens at the end of the device configuration. Once the calibration circuit finds the correct impedance, it powers down and stops changing the characteristics of the drivers.

Table 4–7. Selectable I/O Drivers with On-Chip Parallel Termination with Calibration

I/O Standard	On-Chip Parallel Termination Setting (Column I/O)	Unit
SSTL-2 Class I	50	Ω
SSTL-2 Class II	50	Ω
SSTL-18 Class I	50	Ω
SSTL-18 Class II	50	Ω
1.8-V HSTL Class I	50	Ω
1.8-V HSTL Class II	50	Ω
1.5-V HSTL Class I	50	Ω
1.5-V HSTL Class II	50	Ω
1.2-V HSTL *(1)*	50	Ω

Note to Table 4–7:
(1) 1.2-V HSTL is only supported in I/O banks 4,7, and 8.

There are two separate sets of calibration circuits in the Stratix II and Stratix II GX devices:

- One calibration circuit for top banks 3 and 4
- One calibration circuit for bottom banks 7 and 8

Calibration circuits rely on the external pull-up reference resistor (R_{UP}) and pull-down reference resistor (R_{DN}) to achieve accurate on-chip series and parallel termination. There is one pair of RUP and RDN pins in bank 4 for the calibration circuit for top I/O banks 3 and 4. Similarly, there is one pair of RUP and RDN pins in bank 7 for the calibration circuit for bottom I/O banks 7 and 8. Two banks share the same calibration circuitry, so they must have the same V_{CCIO} voltage if both banks enable on-chip series or parallel termination with calibration. If banks 3 and 4 have different V_{CCIO} voltages, only bank 4 can enable on-chip series or parallel termination with calibration because the RUP and RDN pins are located in bank 4. Bank 3 still can use on-chip series termination, but without calibration. The same rule applies to banks 7 and 8.

On-chip parallel termination with calibration is only supported for input pins. Pins configured as bidirectional do not support on-chip parallel termination.

The RUP and RDN pins are dual-purpose I/Os, which means they can be used as regular I/Os if the calibration circuit is not used. When used for calibration, the RUP pin is connected to V_{CCIO} through an external 25-Ω or 50-Ω resistor for an on-chip series termination value of 25 Ω or 50 Ω, respectively. The RDN pin is connected to GND through an external 25-Ω or 50-Ω resistor for an on-chip series termination value of 25 Ω or 50 Ω, respectively. For on-chip parallel termination, the RUP pin is connected to V_{CCIO} through an external 50-Ω resistor, and RDN is connected to GND through an external 50-Ω resistor.

For more information on tolerance specifications for on-chip termination with calibration, refer to the *DC & Switching Characteristics* chapter in volume 1 of the *Stratix II Device Handbook* or the *DC & Switching Characteristics* chapter in volume 1 of the *Stratix II GX Device Handbook*.

Design Considerations

While Stratix II and Stratix II GX devices feature various I/O capabilities for high-performance and high-speed system designs, there are several other considerations that require attention to ensure the success of those designs.

I/O Termination

I/O termination requirements for single-ended and differential I/O standards are discussed in this section.

Single-Ended I/O Standards

Although single-ended, non-voltage-referenced I/O standards do not require termination, impedance matching is necessary to reduce reflections and improve signal integrity.

Voltage-referenced I/O standards require both an input reference voltage, V_{REF}, and a termination voltage, V_{TT}. The reference voltage of the receiving device tracks the termination voltage of the transmitting device. Each voltage-referenced I/O standard requires a unique termination setup. For example, a proper resistive signal termination scheme is critical in SSTL standards to produce a reliable DDR memory system with superior noise margin.

Stratix II and Stratix II GX on-chip series and parallel termination provides the convenience of no external components. External pull-up resistors can be used to terminate the voltage-referenced I/O standards such as SSTL-2 and HSTL.

Refer to the "Stratix II and Stratix II GX I/O Standards Support" on page 4–2 for more information on the termination scheme of various single-ended I/O standards.

Differential I/O Standards

Differential I/O standards typically require a termination resistor between the two signals at the receiver. The termination resistor must match the differential load impedance of the bus. Stratix II and Stratix II GX devices provide an optional differential on-chip resistor when using LVDS and HyperTransport standards.

I/O Banks Restrictions

Each I/O bank can simultaneously support multiple I/O standards. The following sections provide guidelines for mixing non-voltage-referenced and voltage-referenced I/O standards in Stratix II and Stratix II GX devices.

Non-Voltage-Referenced Standards

Each Stratix II and Stratix II GX device I/O bank has its own V_{CCIO} pins and supports only one V_{CCIO}, either 1.5, 1.8, 2.5, or 3.3 V. An I/O bank can simultaneously support any number of input signals with different I/O standard assignments, as shown in Table 4–8.

For output signals, a single I/O bank supports non-voltage-referenced output signals that are driving at the same voltage as V_{CCIO}. Since an I/O bank can only have one V_{CCIO} value, it can only drive out that one value for non-voltage-referenced signals. For example, an I/O bank with a 2.5-V V_{CCIO} setting can support 2.5-V standard inputs and outputs and 3.3-V LVCMOS inputs (not output or bidirectional pins).

Table 4–8. Acceptable Input Levels for LVTTL and LVCMOS (Part 1 of 2)

Bank V_{CCIO} (V)	Acceptable Input Levels (V)			
	3.3	2.5	1.8	1.5
3.3	✓	✓ *(1)*		
2.5	✓	✓		

Table 4–8. Acceptable Input Levels for LVTTL and LVCMOS (Part 2 of 2)

Bank V_{CCIO} (V)	Acceptable Input Levels (V)			
	3.3	2.5	1.8	1.5
1.8	✓ (2)	✓ (2)	✓	✓ (1)
1.5	✓ (2)	✓ (2)	✓	✓

Notes to Table 4–8:

(1) Because the input signal does not drive to the rail, the input buffer does not completely shut off, and the I/O current is slightly higher than the default value.

(2) These input values overdrive the input buffer, so the pin leakage current is slightly higher than the default value. To drive inputs higher than V_{CCIO} but less than 4.0 V, disable the PCI clamping diode and select the **Allow LVTTL and LVCMOS input levels to overdrive input buffer** option in the Quartus II software.

Voltage-Referenced Standards

To accommodate voltage-referenced I/O standards, each Stratix II or Stratix II GX device's I/O bank supports multiple V_{REF} pins feeding a common V_{REF} bus. The number of available V_{REF} pins increases as device density increases. If these pins are not used as V_{REF} pins, they cannot be used as generic I/O pins. However, each bank can only have a single V_{CCIO} voltage level and a single V_{REF} voltage level at a given time.

An I/O bank featuring single-ended or differential standards can support voltage-referenced standards as long as all voltage-referenced standards use the same V_{REF} setting.

Because of performance reasons, voltage-referenced input standards use their own V_{CCIO} level as the power source. For example, you can only place 1.5-V HSTL input pins in an I/O bank with a 1.5-V V_{CCIO}.

Refer to the "Stratix II and Stratix II GX I/O Banks" on page 4–20 for details on input V_{CCIO} for voltage-referenced standards.

Voltage-referenced bidirectional and output signals must be the same as the I/O bank's V_{CCIO} voltage. For example, you can only place SSTL-2 output pins in an I/O bank with a 2.5-V V_{CCIO}.

Refer to the "I/O Placement Guidelines" on page 4–36 for details on voltage-referenced I/O standards placement.

Mixing Voltage-Referenced and Non-Voltage-Referenced Standards

An I/O bank can support both non-voltage-referenced and voltage-referenced pins by applying each of the rule sets individually. For example, an I/O bank can support SSTL-18 inputs and 1.8-V inputs and outputs with a 1.8-V V_{CCIO} and a 0.9-V V_{REF}. Similarly, an I/O bank can support 1.5-V standards, 2.5-V (inputs, but not outputs), and HSTL I/O standards with a 1.5-V V_{CCIO} and 0.75-V V_{REF}.

I/O Placement Guidelines

The I/O placement guidelines help to reduce noise issues that may be associated with a design such that Stratix II and Stratix II GX FPGAs can maintain an acceptable noise level on the V_{CCIO} supply. Because Stratix II and Stratix II GX devices require each bank to be powered separately for V_{CCIO}, these noise issues have no effect when crossing bank boundaries and, as such, these rules need not be applied.

This section provides I/O placement guidelines for the programmable I/O standards supported by Stratix II and Stratix II GX devices and includes essential information for designing systems using their devices' selectable I/O capabilities.

V_{REF} Pin Placement Restrictions

There are at least two dedicated V_{REF} pins per I/O bank to drive the V_{REF} bus. Larger Stratix II and Stratix II GX devices have more V_{REF} pins per I/O bank. All V_{REF} pins within one I/O bank are shorted together at device die level.

There are limits to the number of pins that a V_{REF} pin can support. For example, each output pin adds some noise to the V_{REF} level and an excessive number of outputs make the level too unstable to be used for incoming signals.

Restrictions on the placement of single-ended voltage-referenced I/O pads with respect to V_{REF} pins help maintain an acceptable noise level on the V_{CCIO} supply and prevent output switching noise from shifting the V_{REF} rail.

Input Pins
Each V_{REF} pin supports a maximum of 40 input pads.

Output Pins

When a voltage-referenced input or bidirectional pad does not exist in a bank, the number of output pads that can be used in that bank depends on the total number of available pads in that same bank. However, when a voltage-referenced input exists, a design can use up to 20 output pads per V_{REF} pin in a bank.

Bidirectional Pins

Bidirectional pads must satisfy both input and output guidelines simultaneously. The general formulas for input and output rules are shown in Table 4–9.

Table 4–9. Bidirectional Pin Limitation Formulas

Rules	Formulas
Input	<Total number of bidirectional pins> + <Total number of V_{REF} input pins, if any> ≤40 per V_{REF} pin
Output	<Total number of bidirectional pins> + <Total number of output pins, if any> – <Total number of pins from smallest OE group, if more than one OE groups> ≤20 per V_{REF} pin

- If the same output enable (OE) controls all the bidirectional pads (bidirectional pads in the same OE group are driving in and out at the same time) and there are no other outputs or voltage-referenced inputs in the bank, then the voltage-referenced input is never active at the same time as an output. Therefore, the output limitation rule does not apply. However, since the bidirectional pads are linked to the same OE, the bidirectional pads will all act as inputs at the same time. Therefore, there is a limit of 40 input pads, as follows:

  <Total number of bidirectional pins> + *<Total number of V_{REF} input pins>* ≤40 per V_{REF} pin

- If any of the bidirectional pads are controlled by different OE and there are no other outputs or voltage-referenced inputs in the bank, then one group of bidirectional pads can be used as inputs and another group is used as outputs. In such cases, the formula for the output rule is simplified, as follows:

  <Total number of bidirectional pins> – *<Total number of pins from smallest OE group>* ≤20 per V_{REF} pin

- Consider a case where eight bidirectional pads are controlled by OE1, eight bidirectional pads are controlled by OE2, six bidirectional pads are controlled by OE3, and there are no other outputs or voltage-referenced inputs in the bank. While this totals 22 bidirectional pads, it is safely allowable because there would be a possible maximum of 16 outputs per V_{REF} pin, assuming the worst case where OE1 and OE2 are active and OE3 is inactive. This is useful for DDR SDRAM applications.

- When at least one additional voltage-referenced input and no other outputs exist in the same V_{REF} group, the bidirectional pad limitation must simultaneously adhere to the input and output limitations. The input rule becomes:

  <Total number of bidirectional pins> + *<Total number of V_{REF} input pins>* ≤40 per V_{REF} pin

  Whereas the output rule is simplified as:

  <Total number of bidirectional pins> ≤20 per V_{REF} pin

- When at least one additional output exists but no voltage-referenced inputs exist, the output rule becomes:

  <Total number of bidirectional pins> + *<Total number of output pins>* – *<Total number of pins from smallest OE group>* ≤20 per V_{REF} pin

- When additional voltage-referenced inputs and other outputs exist in the same V_{REF} group, then the bidirectional pad limitation must again simultaneously adhere to the input and output limitations. The input rule is:

  <Total number of bidirectional pins> + *<Total number of V_{REF} input pins>* ≤40 per V_{REF} pin

  Whereas the output rule is given as:

  <Total number of bidirectional pins> + *<Total number of output pins>* – *<Total number of pins from smallest OE group>* ≤20 per V_{REF} pin

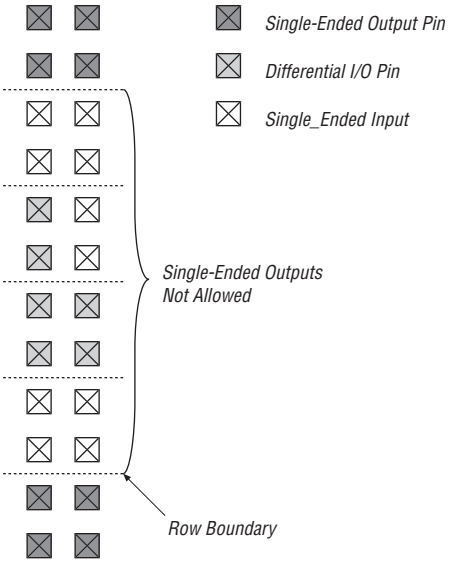
I/O Pin Placement with Respect to High-Speed Differential I/O Pins

Regardless of whether or not the SERDES circuitry is utilized, there is a restriction on the placement of single-ended output pins with respect to high-speed differential I/O pins. As shown in Figure 4–25, all

single-ended outputs must be placed at least one LAB row away from the differential I/O pins. There are no restrictions on the placement of single-ended input pins with respect to differential I/O pins. Single-ended input pins may be placed within the same LAB row as differential I/O pins. However, the single-ended input's IOE register is not available. The input must be implemented within the core logic.

This single-ended output pin placement restriction only applies when using the LVDS or HyperTransport I/O standards in the left and right I/O banks. There are no restrictions for single-ended output pin placement with respect to differential clock pins in the top and bottom I/O banks.

Figure 4–25. Single-Ended Output Pin Placement with Respect to Differential I/O Pins



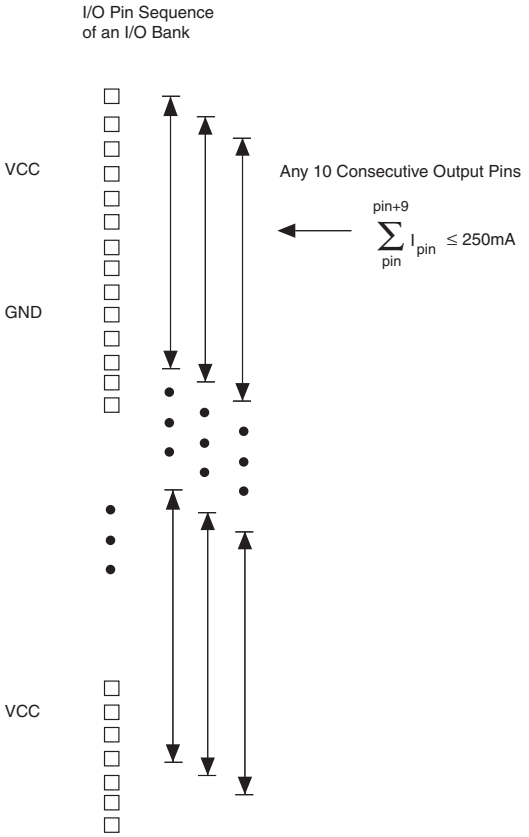
DC Guidelines

Power budgets are essential to ensure the reliability and functionality of a system application. You are often required to perform power dissipation analysis on each device in the system to come out with the total power dissipated in that system, which is composed of a static component and a dynamic component.

The static power consumption of a device is the total DC current flowing from V_{CCIO} to ground.

For any ten consecutive pads in an I/O bank of Stratix II and Stratix II GX devices, Altera recommends a maximum current of 250 mA, as shown in Figure 4–26, because the placement of V_{CCIO}/ground (GND) bumps are regular, 10 I/O pins per pair of power pins. This limit is on the static power consumed by an I/O standard, as shown in Table 4–10. Limiting static power is a way to improve reliability over the lifetime of the device.

Figure 4–26. DC Current Density Restriction *Notes (1), (2)*



Notes to Figure 4–26:

(1) The consecutive pads do not cross I/O banks.

(2) V_{REF} pins do not affect DC current calculation because there are no V_{REF} pads.

Table 4–10 shows the I/O standard DC current specification.

Table 4–10. Stratix II and Stratix II GX I/O Standard DC Current Specification (Part 1 of 2) *Note (1)*

I/O Standard	I_{PIN} (mA), Top and Bottom I/O Banks	I_{PIN} (mA), Left and Right I/O Banks *(2)*
LVTTL	*(3)*	*(3)*
LVCMOS	*(3)*	*(3)*
2.5 V	*(3)*	*(3)*
1.8 V	*(3)*	*(3)*
1.5 V	*(3)*	*(3)*
3.3-V PCI	1.5	NA
3.3-V PCI-X	1.5	NA
SSTL-2 Class I	12 *(4)*	12 *(4)*
SSTL-2 Class II	24 *(4)*	16 *(4)*
SSTL-18 Class I	12 *(4)*	10 *(4)*
SSTL-18 Class II	20 *(4)*	NA
1.8-V HSTL Class I	12 *(4)*	12
1.8-V HSTL Class II	20 *(4)*	NA
1.5-V HSTL Class I	12 *(4)*	8
1.5-V HSTL Class II	20 *(4)*	NA
Differential SSTL-2 Class I	12	12
Differential SSTL-2 Class II	24	16
Differential SSTL-18 Class I	12	10
Differential SSTL-18 Class II	20	NA
1.8-V differential HSTL Class I	12	12
1.8-V differential HSTL Class II	20	NA
1.5-V differential HSTL Class I	12	8
1.5-V differential HSTL Class II	20	NA

Table 4–10. Stratix II and Stratix II GX I/O Standard DC Current Specification (Part 2 of 2) Note (1)		
I/O Standard	I_{PIN} (mA), Top and Bottom I/O Banks	I_{PIN} (mA), Left and Right I/O Banks (2)

Notes to Table 4–10:

(1) The current value obtained for differential HSTL and differential SSTL standards is per pin and not per differential pair, as opposed to the per-pair current value of LVDS and HyperTransport standards.

(2) This does not apply to the right I/O banks of Stratix II GX devices. Stratix II GX devices have transceivers on the right I/O banks.

(3) The DC power specification of each I/O standard depends on the current sourcing and sinking capabilities of the I/O buffer programmed with that standard, as well as the load being driven. LVTTL, LVCMOS, 2.5-V, 1.8-V, and 1.5-V outputs are not included in the static power calculations because they normally do not have resistor loads in real applications. The voltage swing is rail-to-rail with capacitive load only. There is no DC current in the system.

(4) This I_{PIN} value represents the DC current specification for the default current strength of the I/O standard. The I_{PIN} varies with programmable drive strength and is the same as the drive strength as set in Quartus II software. Refer to the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook* or the *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook* for a detailed description of the programmable drive strength feature of voltage-referenced I/O standards.

Table 4–10 only shows the limit on the static power consumed by an I/O standard. The amount of power used at any moment could be much higher, and is based on the switching activities.

Conclusion

Stratix II and Stratix II GX devices provide I/O capabilities that allow you to work in compliance with current and emerging I/O standards and requirements. With the Stratix II or Stratix II GX devices features, such as programmable driver strength, you can reduce board design interface costs and increase the development flexibility.

References

Refer to the following references for more information:

- Interface Standard for Nominal 3V / 3.3-V Supply Digital Integrated Circuits, JESD8-B, Electronic Industries Association, September 1999.
- 2.5-V +/- 0.2V (Normal Range) and 1.8-V to 2.7V (Wide Range) Power Supply Voltage and Interface Standard for Non-terminated Digital Integrated Circuits, JESD8-5, Electronic Industries Association, October 1995.
- 1.8-V +/- 0.15 V (Normal Range) and 1.2 V - 1.95 V (Wide Range) Power Supply Voltage and Interface Standard for Non-terminated Digital Integrated Circuits, JESD8-7, Electronic Industries Association, February 1997.
- 1.5-V +/- 0.1 V (Normal Range) and 0.9 V - 1.6 V (Wide Range) Power Supply Voltage and Interface Standard for Non-terminated Digital Integrated Circuits, JESD8-11, Electronic Industries Association, October 2000.

- PCI Local Bus Specification, Revision 2.2, PCI Special Interest Group, December 1998.
- PCI-X Local Bus Specification, Revision 1.0a, PCI Special Interest Group.
- Stub Series Terminated Logic for 2.5-V (SSTL-2), JESD8-9A, Electronic Industries Association, December 2000.
- Stub Series Terminated Logic for 1.8 V (SSTL-18), Preliminary JC42.3, Electronic Industries Association.
- High-Speed Transceiver Logic (HSTL)—A 1.5-V Output Buffer Supply Voltage Based Interface Standard for Digital Integrated Circuits, EIA/JESD8-6, Electronic Industries Association, August 1995.
- Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits, ANSI/TIA/EIA-644, American National Standards Institute/Telecommunications Industry/Electronic Industries Association, October 1995.

Referenced Documents

This chapter references the following documents:

- *DC & Switching Characteristics* chapter in volume 1 of the *Stratix II Device Handbook*
- *DC & Switching Characteristics* chapter in volume 1 of the *Stratix II GX Device Handbook*
- *External Memory Interfaces in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook*
- *External Memory Interfaces in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook*
- *High-Speed Differential I/O Interfaces with DPA in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook*
- *High-Speed Differential I/O Interfaces with DPA in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook*
- *PLLs in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook*
- *PLLs in Stratix II & Straix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook*
- *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*
- *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*
- *Stratix II GX Transceiver User Guide* (volume 1) of the *Stratix II GX Device Handbook*

Document Revision History

Table 4–11 shows the revision history for this chapter.

Table 4–11. Document Revision History (Part 1 of 2)

Date and Document Version	Changes Made	Summary of Changes
January 2008 v4.6	Updated Figure 4–22.	—
	Updated Note 4 to Table 4–2.	—
	Added "Referenced Documents" section.	—
	Minor text edits.	—
No change	For the *Stratix II GX Device Handbook* only: Formerly chapter 9. The chapter number changed due to the addition of the *Stratix II GX Dynamic Reconfiguration* chapter. No content change.	—
May 2007 v4.5	Added a note to the "On-Chip Series Termination with Calibration" section.	—
	Added a note to the "On-Chip Series Termination without Calibration" section	—
	Updated note to the "Stratix II and Stratix II GX I/O Features" section.	—
	Updated the "LVDS" section.	—
	Updated note to "1.5 V" section	—
	• Updated Note (1) for Table 10–4 • Updated Note (2) for Table 10–3	—
	Updated Table 10–2, column heading for columns 9 and 10.	—
	Updated Table 10–10.	—
	Fixed typo in the "Stratix II and Stratix II GX I/O Features" section	—
February 2007 v4.4	Added the "Document Revision History" section to this chapter.	—
August 2006 v4.3	Updated Table 9–2, Table 9–4, Table 9–5, Table 9–6, and Table 9–7.	—
April 2006 v4.2	Chapter updated as part of the *Stratix II Device Handbook* update.	—
No change	Formerly chapter 8. Chapter number change only due to chapter addition to Section I in February 2006; no content change.	—

Table 4–11. Document Revision History (Part 2 of 2)

Date and Document Version	Changes Made	Summary of Changes
December 2005 v4.1	Chapter updated as part of the *Stratix II Device Handbook* update.	—
October 2005 v4.0	Added chapter to the *Stratix II GX Device Handbook*.	—

5. High-Speed Differential I/O Interfaces with DPA in Stratix II and Stratix II GX Devices

SII52005-2.2

Introduction

Stratix® II and Stratix® II GX device family offers up to 1-Gbps differential I/O capabilities to support source-synchronous communication protocols such as HyperTransport™ technology, Rapid I/O, XSBI, and SPI.

Stratix II and Stratix II GX devices have the following dedicated circuitry for high-speed differential I/O support:

- Differential I/O buffer
- Transmit serializer
- Receive deserializer
- Data realignment circuit
- Dynamic phase aligner (DPA)
- Synchronizer (FIFO buffer)
- Analog PLLs (fast PLLs)

For high-speed differential interfaces, Stratix II and Stratix II GX devices can accommodate different differential I/O standards, including the following:

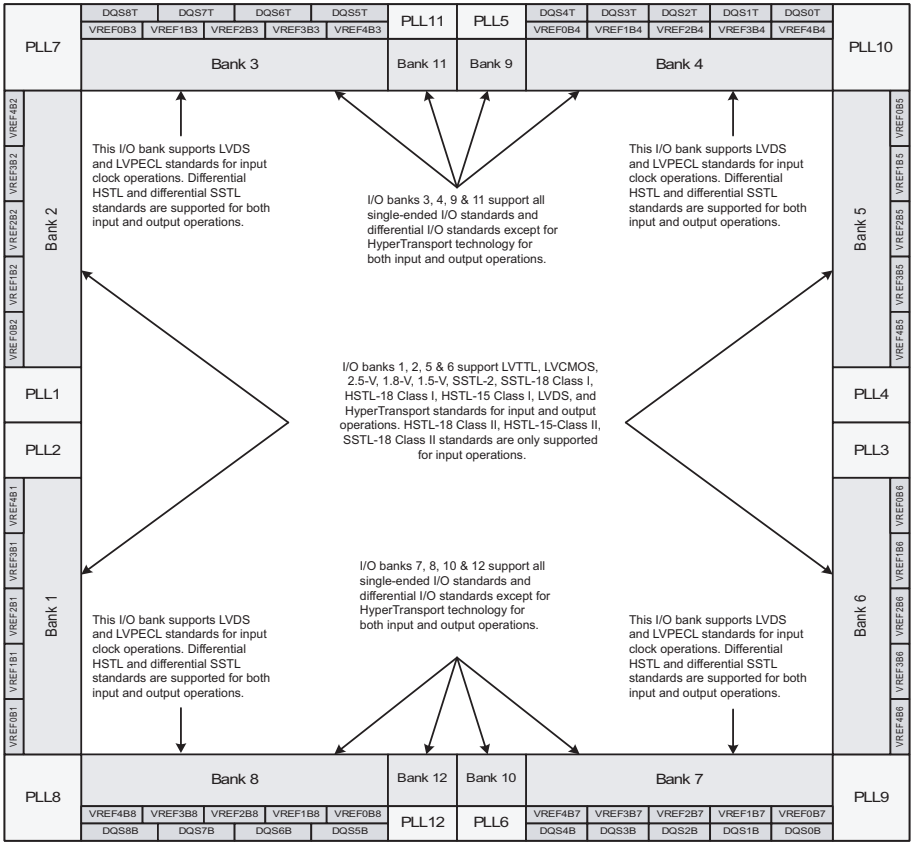
- LVDS
- HyperTransport technology
- HSTL
- SSTL
- LVPECL

HSTL, SSTL, and LVPECL I/O standards can be used only for PLL clock inputs and outputs in differential mode.

I/O Banks

Stratix II and Stratix II GX inputs and outputs are partitioned into banks located on the periphery of the die. The inputs and outputs that support LVDS and HyperTransport technology are located in row I/O banks, two on the left and two on the right side of the Stratix II device and two on the left side of the Stratix II GX device. LVPECL, HSTL, and SSTL standards are supported on certain top and bottom banks of the die (banks 9 to 12) when used as differential clock inputs/outputs. Differential HSTL and SSTL standards can be supported on banks 3, 4, 7, and 8 if the pins on these banks are used as DQS/DQSn pins. Figures 5–1 and 5–2 show where the banks and the PLLs are located on the die.

Figure 5–1. Stratix II I/O Banks *Note (1), (2), (3), (4), (5), (6), and (7)*



Notes to Figure 5–1:

(1) Figure 5–1 is a top view of the silicon die that corresponds to a reverse view for flip-chip packages. It is a graphical representation only. See the pin list and Quartus II software for exact locations.

(2) Depending on the size of the device, different device members have different numbers of V_{REF} groups.

(3) Banks 9 through 12 are enhanced PLL external clock output banks. These PLL banks utilize the adjacent V_{REF} group when voltage-referenced standards are implemented. For example, if an SSTL input is implemented in PLL bank 10, the voltage level at VREFB7 is the reference voltage level for the SSTL input.

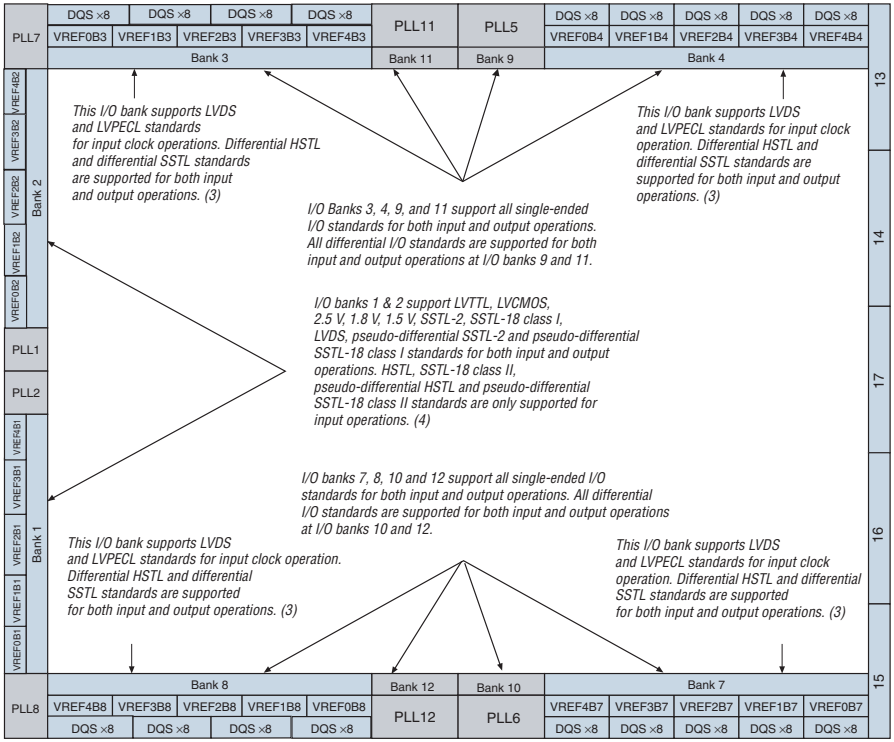
(4) Differential HSTL and differential SSTL standards are available for bidirectional operations on DQS pin and input-only operations on PLL clock input pins; LVDS, LVPECL, and HyperTransport standards are available for input-only operations on PLL clock input pins. See the *Selectable I/O standards in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook* for more details.

(5) Quartus II software does not support differential SSTL and differential HSTL standards at left/right I/O banks. See the *Selectable I/O standards in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook* if you need to implement these standards at these I/O banks.

(6) Banks 11 and 12 are available only in EP2S60, EP2S90, EP2S130, and EP2S180 devices.

(7) PLLs 7, 8, 9, 10, 11, and 12 are available only in EP2S60, EP2S90, EP2S130, and EP2S180 devices.

***Figure 5–2. Stratix II GX I/O Banks** Note (1), (2), (3), (4), (5), (6), and (7)*



Notes to Figure 5–2:

(1) Figure 5–2 is a top view of the silicon die which corresponds to a reverse view for flip-chip packages. It is a graphical representation only.

(2) Depending on size of the device, different device members have different number of V_{REF} groups. Refer to the pin list and the Quartus II software for exact locations.

(3) Banks 9 through 12 are enhanced PLL external clock output banks.

(4) Horizontal I/O banks feature transceiver and DPA circuitry for high speed differential I/O standards.

(5) Quartus II software does not support differential SSTL and differential HSTL standards at left/right I/O banks. Refer to the "Differential Pin Placement Guidelines" on page 5–21 if you need to implement these standards at these I/O banks.

(6) Banks 11 and 12 are available only in EP2SGX60C/D/E, EP2SGX90E/F, and EP2SGX130G.

(7) PLLs 7, 8, 11, and 12 are available only in EP2SGX60C/D/E, EP2SGXE/F, and EP2SGX130G.

Table 5–1 lists the differential I/O standards supported by each bank.

Table 5–1. Supported Differential I/O Types

Bank	Row I/O (Banks 1, 2, 5 and 6) (2)			Column I/O (Banks, 3, 4 and 7 through 12)		
Type	Clock Inputs	Clock Outputs	Data or Regular I/O Pins	Clock Inputs	Clock Outputs	Data or Regular I/O Pins
Differential HSTL				✓	✓	(1)
Differential SSTL				✓	✓	(1)
LVPECL				✓	✓	
LVDS	✓	✓	✓	✓	✓	
HyperTransport technology	✓	✓	✓			

Note to Table 5–1:
(1) Used as both inputs and outputs on the DQS/DQSn pins.
(2) Banks 5 and 6 are not available in Stratix II GX devices.

Table 5–2 shows the total number of differential channels available in Stratix II devices. The available channels are divided evenly between the left and right banks of the die. Non-dedicated clocks in the left and right banks can also be used as data receiver channels. The total number of receiver channels includes these four non-dedicated clock channels. Pin migration is available for different size devices in the same package.

Table 5–2. Differential Channels in Stratix II Devices (Part 1 of 2) Notes (1), (2), and (3)

Device	484-Pin FineLine BGA	484-Pin Hybrid FineLine BGA	672-Pin FineLine BGA	780-Pin FineLine BGA	1,020-Pin FineLine BGA	1,508-Pin FineLine BGA Within the 1,508-pin Fin
EP2S15	38 transmitters 42 receivers		38 transmitters 42 receivers			
EP2S30	38 transmitters 42 receivers		58 transmitters 62 receivers			
EP2S60	38 transmitters 42 receivers		58 transmitters 62 receivers		84 transmitters 84 receivers	
EP2S90		38 transmitters 42 receivers		64 transmitters 68 receivers	90 transmitters 94 receivers	118 transmitters 118 receivers
EP2S130				64 transmitters 68 receivers	88 transmitters 92 receivers	156 transmitters 156 receivers

Table 5–2. Differential Channels in Stratix II Devices (Part 2 of 2) Notes (1), (2), and (3)						
Device	**484-Pin FineLine BGA**	**484-Pin Hybrid FineLine BGA**	**672-Pin FineLine BGA**	**780-Pin FineLine BGA**	**1,020-Pin FineLine BGA**	**1,508-Pin FineLine BGA Within the 1,508-pin Fin**
EP2S180					88 transmitters 92 receivers	156 transmitters 156 receivers

Notes to Table 5–2:
(1) Pin count does not include dedicated PLL input pins.
(2) The total number of receiver channels includes the four non-dedicated clock channels that can optionally be used as data channels.
(3) Within the 1,508-pin FineLine BGA package, 92 receiver channels and 92 transmitter channels are vertically migratable.

Table 5–3 shows the total number of differential channels available in Stratix II GX devices. Non-dedicated clocks in the left bank can also be used as data receiver channels. The total number of receiver channels includes these four non-dedicated clock channels. Pin migration is available for different size devices in the same package.

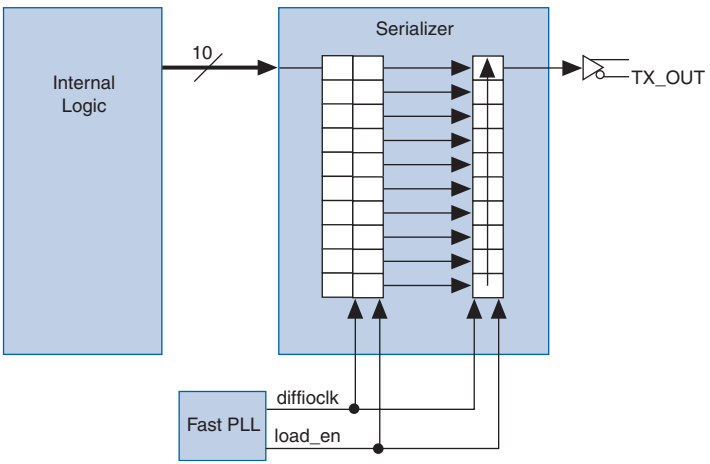
Table 5–3. Differential Channels in Stratix II GX Devices Notes (1), (2), (3)			
Device	**780-Pin FineLine BGA**	**1,152-Pin FineLine BGA**	**1,508-Pin FineLine BGA**
EP2SGX30	29 transmitters 31receivers		
EP2SGX60	29 transmitters 31 receivers	42 transmitters 42 receivers	
EP2SGX90		45 transmitters 47 receivers	59 transmitters 59 receivers
EP2SGX130			71 transmitters 73 receivers

Notes to Table 5–3:
(1) Pin count does not include dedicated PLL input pins.
(2) The total number of receiver channels includes the four non-dedicated clock channels that can optionally be used as data channels.
(3) EP2SGX30CF780 devices with four transceiver channels are vertically migratable to EP2SGX60CF780 devices with four transceiver channels. EP2SGX30DF780 devices with eight transceiver channels are vertically migratable to EP2SGX60DF780 devices with eight transceiver channels. EP2SGX60EF1152 devices with 12 transceiver channels are vertically migratable to EP2SGX90EF1152 devices with 12 transceiver channels. EP2SGX90FF1508 devices with 16 transceiver channels are vertically migratable to EP2SGX130GF1508 devices with 20 transceiver channels.

Differential Transmitter

The Stratix II and Stratix II GX transmitter has dedicated circuitry to provide support for LVDS and HyperTransport signaling. The dedicated circuitry consists of a differential buffer, a serializer, and a shared fast PLL. The differential buffer can drive out LVDS or HyperTransport signal levels that are statically set in the Quartus® II software. The serializer takes data from a parallel bus up to 10 bits wide from the internal logic, clocks it into the load registers, and serializes it using the shift registers before sending the data to the differential buffer. The most significant bit (MSB) is transmitted first. The load and shift registers are clocked by the `diffioclk` (a fast PLL clock running at the serial rate) and controlled by the load enable signal generated from the fast PLL. The serialization factor can be statically set to ×4, ×5, ×6, ×7, ×8, ×9, or ×10 using the Quartus II software. The load enable signal is automatically generated by the fast PLL and is derived from the serialization factor setting. Figure 5–3 is a block diagram of the Stratix II transmitter.

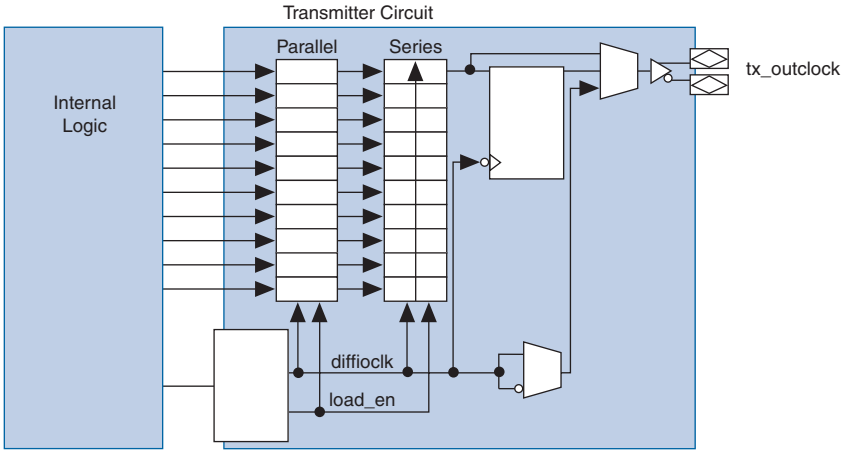
Figure 5–3. Transmitter Block Diagram



Each Stratix II and Stratix II GX transmitter data channel can be configured to operate as a transmitter clock output. This flexibility allows the designer to place the output clock near the data outputs to simplify board layout and reduce clock-to-data skew. Different applications often require specific clock to data alignments or specific data rate to clock rate factors. The transmitter can output a clock signal at the same rate as the data with a maximum frequency of 717 MHz. The output clock can also be divided by a factor of 2, 4, 8, or 10, depending on the serialization factor. The phase of the clock in relation to the data can be set at 0° or 180° (edge or center aligned). The fast PLL provides additional support for

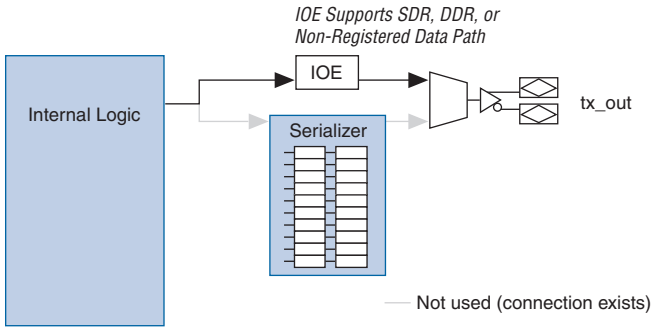
other phase shifts in 45° increments. These settings are made statically in the Quartus II MegaWizard® software. Figure 5–4 shows the transmitter in clock output mode.

Figure 5–4. Transmitter in Clock Output Mode



The serializer can be bypassed to support DDR (×2) and SDR (×1) operations. The I/O element (IOE) contains two data output registers that each can operate in either DDR or SDR mode. The clock source for the registers in the IOE can come from any routing resource, from the fast PLL, or from the enhanced PLL. Figure 5–5 shows the bypass path.

Figure 5–5. Serializer Bypass



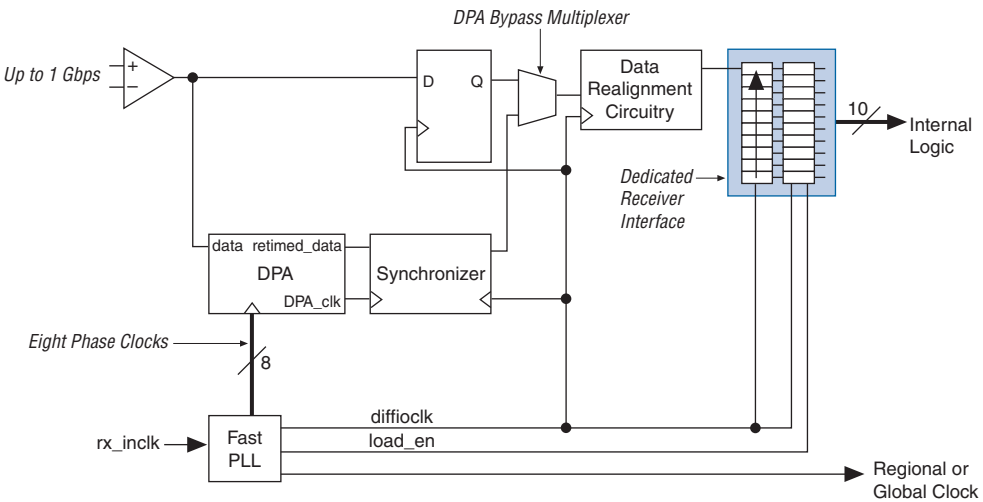
Differential Receiver

The receiver has dedicated circuitry to support high-speed LVDS and HyperTransport signaling, along with enhanced data reception. Each receiver consists of a differential buffer, dynamic phase aligner (DPA), synchronization FIFO buffer, data realignment circuit, deserializer, and a shared fast PLL. The differential buffer receives LVDS or HyperTransport signal levels, which are statically set by the Quartus II software. The DPA block aligns the incoming data to one of eight clock phases to maximize the receiver's skew margin. The DPA circuit can be bypassed on a channel-by-channel basis if it is not needed. Set the DPA bypass statically in the Quartus II MegaWizard Plug-In Manager or dynamically by using the optional RX_DPLL_ENABLE port.

The synchronizer circuit is a 1-bit wide by 6-bit deep FIFO buffer that compensates for any phase difference between the DPA block and the deserializer. If necessary, the data realignment circuit inserts a single bit of latency in the serial bit stream to align the word boundary. The deserializer includes shift registers and parallel load registers, and sends a maximum of 10 bits to the internal logic. The data path in the receiver is clocked by either the diffioclk signal or the DPA recovered clock. The deserialization factor can be statically set to 4, 5, 6, 7, 8, 9, or 10 by using the Quartus II software. The fast PLL automatically generates the load enable signal, which is derived from the deserialization factor setting.

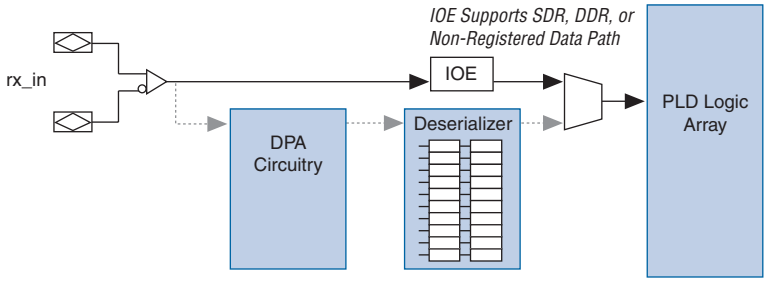
Figure 5–6 shows a block diagram of the receiver.

Figure 5–6. Receiver Block Diagram



The deserializer, like the serializer, can also be bypassed to support DDR (×2) and SDR (×1) operations. The DPA and data realignment circuit cannot be used when the deserializer is bypassed. The IOE contains two data input registers that can operate in DDR or SDR mode. The clock source for the registers in the IOE can come from any routing resource, from the fast PLL, or from the enhanced PLL. Figure 5–7 shows the bypass path.

Figure 5–7. Deserializer Bypass



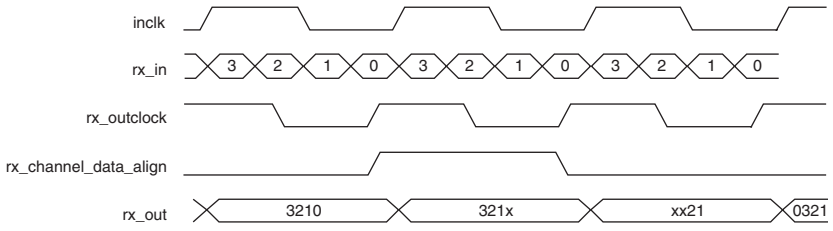
Receiver Data Realignment Circuit

The data realignment circuit aligns the word boundary of the incoming data by inserting bit latencies into the serial stream. An optional RX_CHANNEL_DATA_ALIGN port controls the bit insertion of each receiver independently controlled from the internal logic. The data slips one bit for every pulse on the RX_CHANNEL_DATA_ALIGN port. The following are requirements for the RX_CHANNEL_DATA_ALIGN port:

- The minimum pulse width is one period of the parallel clock in the logic array.
- The minimum low time between pulses is one period of parallel clock.
- There is no maximum high or low time.
- Valid data is available two parallel clock cycles after the rising edge of RX_CHANNEL_DATA_ALIGN.

Figure 5–8 shows receiver output (RX_OUT) after one bit slip pulse with the deserialization factor set to 4.

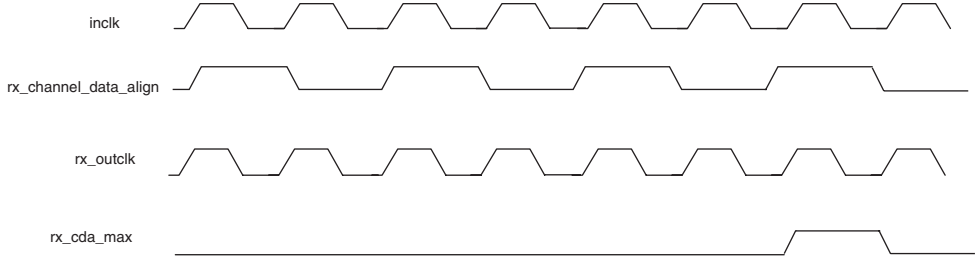
Figure 5–8. Data Realignment Timing



The data realignment circuit can have up to 11 bit-times of insertion before a rollover occurs. The programmable bit rollover point can be from 1 to 11 bit-times independent of the deserialization factor. An optional status port, rx_cda_max, is available to the FPGA from each channel to indicate when the preset rollover point is reached.

Figure 5–9 illustrates a preset value of four bit-times before rollover occurs. The rx_cda_max signal pulses for one rx_outclk cycle to indicate that the rollover has occurred.

Figure 5–9. Receiver Data Re-alignment Rollover

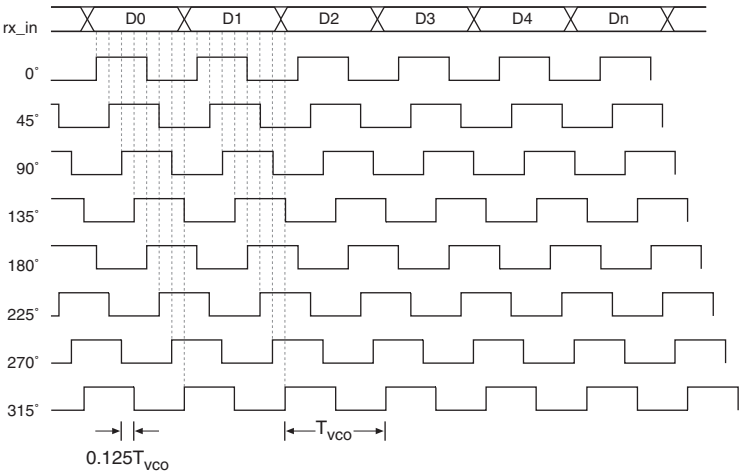


Dynamic Phase Aligner

The DPA block takes in high-speed serial data from the differential input buffer and selects one of eight phase clocks to sample the data. The DPA chooses a phase closest to the phase of the serial data. The maximum phase offset between the data and the phase-aligned clock is 1/8 UI, which is the maximum quantization error of the DPA. The eight phases

are equally divided, giving a 45-degree resolution. Figure 5–10 shows the possible phase relationships between the DPA clocks and the incoming serial data.

Figure 5–10. DPA Clock Phase to Data Bit Relationship



Each DPA block continuously monitors the phase of the incoming data stream and selects a new clock phase if needed. The selection of a new clock phase can be prevented by the optional RX_DPLL_HOLD port, which is available for each channel.

The DPA block requires a training pattern and a training sequence of at least 256 repetitions of the training pattern. The training pattern is not fixed, so you can use any training pattern with at least one transition on each channel. An optional output port, RX_DPA_LOCKED, is available to the internal logic, to indicate when the DPA block has settled on the closest phase to the incoming data phase. The RX_DPA_LOCKED de-asserts, depending on what is selected in the Quartus II MegaWizard Plug-In, when either a new phase is selected, or when the DPA has moved two phases in the same direction. The data may still be valid even when the RX_DPA_LOCKED is deasserted. Use data checkers to validate the data when RX_DPA_LOCKED is deasserted.

An independent reset port, RX_RESET, is available to reset the DPA circuitry. The DPA circuit must be retrained after reset.

Synchronizer

The synchronizer is a 1-bit × 6-bit deep FIFO buffer that compensates for the phase difference between the recovered clock from the DPA circuit and the `diffioclk` that clocks the rest of the logic in the receiver. The synchronizer can only compensate for phase differences, not frequency differences between the data and the receiver's `INCLK`. An optional port, `RX_FIFO_RESET`, is available to the internal logic to reset the synchronizer. The synchronizer is automatically reset when the DPA first locks to the incoming data. Altera® recommends using `RX_FIFO_RESET` to reset the synchronizer when the DPA signals a loss-of-lock condition beyond the initial locking condition.

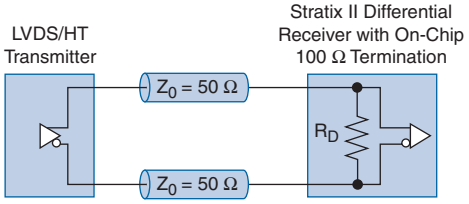
Differential I/O Termination

Stratix II and Stratix II GX devices provide an on-chip 100-Ω differential termination option on each differential receiver channel for LVDS and HyperTransport standards. The on-chip termination eliminates the need to supply an external termination resistor, simplifying the board design and reducing reflections caused by stubs between the buffer and the termination resistor. You can enable on-chip termination in the Quartus II assignments editor. Differential on-chip termination is supported across the full range of supported differential data rates.

For more information, refer to the High-Speed I/O Specifications section of the *DC & Switching Characteristics* chapter in volume 1 of the *Stratix II Device Handbook* or the High-Speed I/O Specifications section of the *DC & Switching Characteristics* chapter in volume 1 of the *Stratix II GX Device Handbook*.

Figure 5–11 illustrates on-chip termination.

Figure 5–11. On-Chip Differential Termination



On-chip differential termination is supported on all row I/O pins and on clock pins `CLK[0, 2, 8, 10]`. The clock pins `CLK[1, 3, 9, 11]`, and `FPLL[7..10]CLK`, and the clocks in the top and bottom I/O banks (`CLK[4..7, 12..15]`) do not support differential on-chip termination.

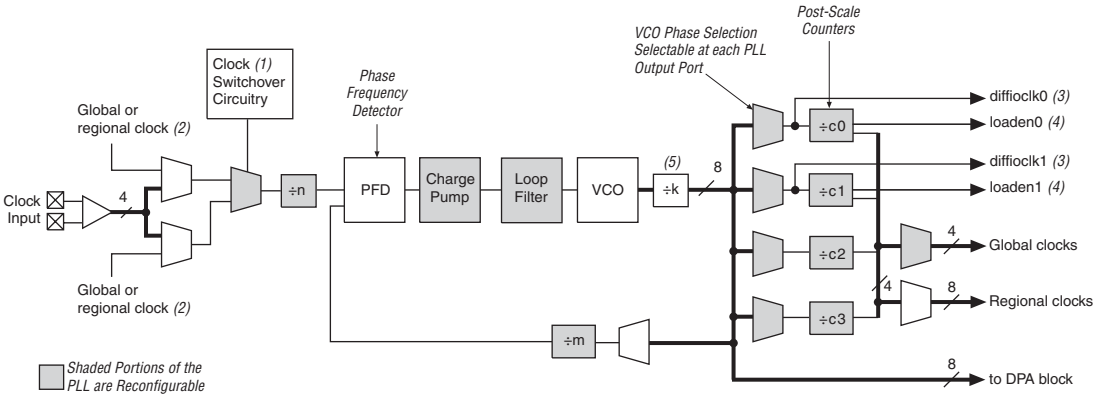
Fast PLL

The high-speed differential I/O receiver and transmitter channels use the fast PLL to generate the parallel global clocks (`rx-` or `tx-` clock) and high-speed clocks (`diffioclk`). Figure 5–12 shows the locations of the fast PLLs. The fast PLL VCO operates at the clock frequency of the data rate. Each fast PLL offers a single serial data rate support, but up to two separate serialization and/or deserialization factors (from the C0 and C1 fast PLL clock outputs) can be used. Clock switchover and dynamic fast PLL reconfiguration is available in high-speed differential I/O support mode.

For additional information on the fast PLL, refer to the *PLLs in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Handbook* or the *PLLs in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Handbook*.

Figure 5–12 shows a block diagram of the fast PLL in high-speed differential I/O support mode.

Figure 5–12. Fast PLL Block Diagram



Notes to Figure 5–12:

(1) Stratix II fast PLLs only support manual clock switchover.

(2) The global or regional clock input can be driven by an output from another PLL, a pin-driven dedicated global or regional clock, or through a clock control block provided the clock control block is fed by an output from another PLL or pin-driven dedicated global or regional clock.

(3) In high-speed differential I/O support mode, this high-speed PLL clock feeds the SERDES. Stratix II devices only support one rate of data transfer per fast PLL in high-speed differential I/O support mode.

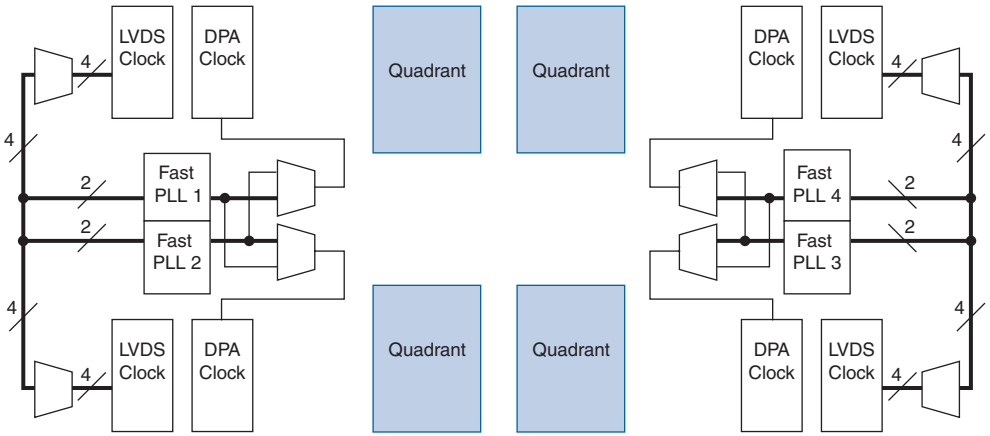
(4) This signal is a high-speed differential I/O support SERDES control signal.

(5) If the design enables this ÷2 counter, the device can use a VCO frequency range of 150 to 520 MHz.

Clocking

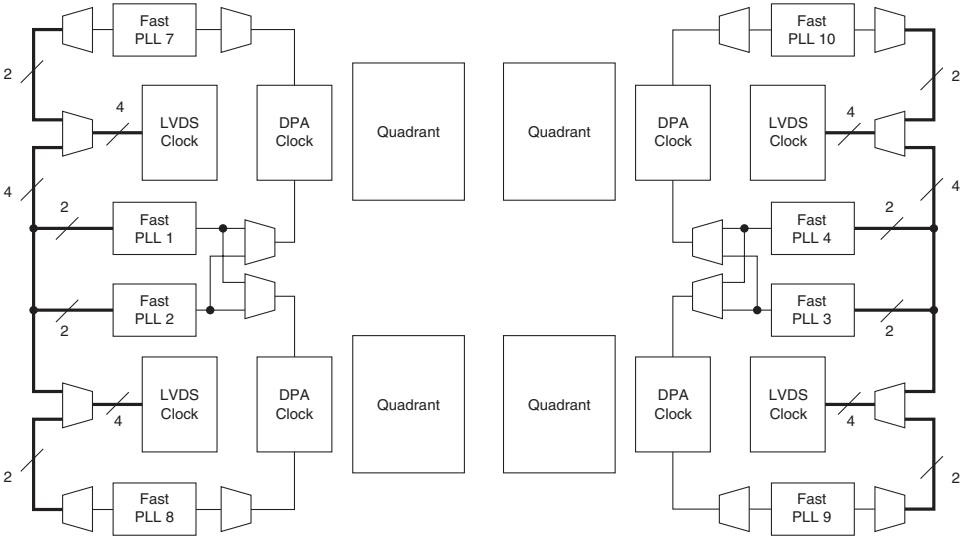
The fast PLLs feed in to the differential receiver and transmitter channels through the LVDS/DPA clock network. The center fast PLLs can independently feed the banks above and below them. The corner PLLs can feed only the banks adjacent to them. Figures 5–13 and 5–14 show the LVDS and DPA clock networks of the Stratix II devices.

Figure 5–13. Fast PLL and LVDS/DPA Clock for EP2S15, EP2S30, and EP2S60 Devices *Note (1)*



Note to Figure 5–13:
(1) Figure 5–13 applies to EP2S60 devices in the 484 and 672 pin packages.

Figure 5–14. Fast PLL and LVDS/DPA Clocks for EP2S60, EP2S90, EP2S130 and EP2S180 Devices Note (1)



Note to Figure 5–14:
(1) Figure 5–14 applies only to the EP2S60 in the 1020 Stratix II GX device.

Figures 5–15 and 5–16 show the Fast PLL and LVDS/DPA clock of the Stratix II GX devices.

Figure 5–15. Fast PLL and LVDS/DPA Clock for EP2SGX30C/D and EP2SGX60C/D Devices

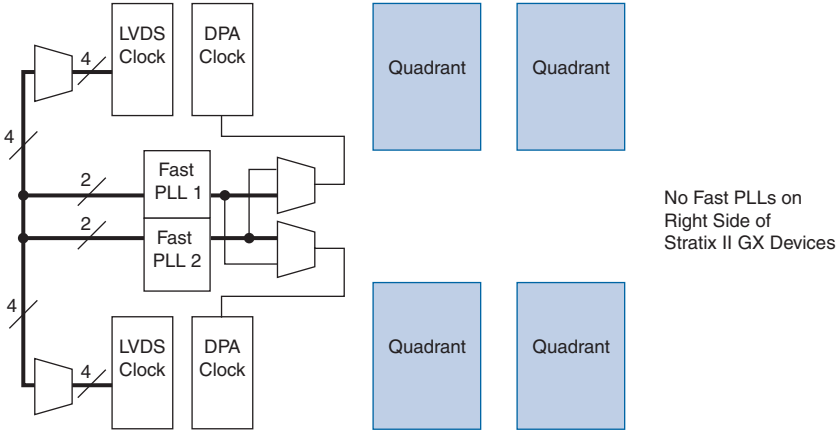
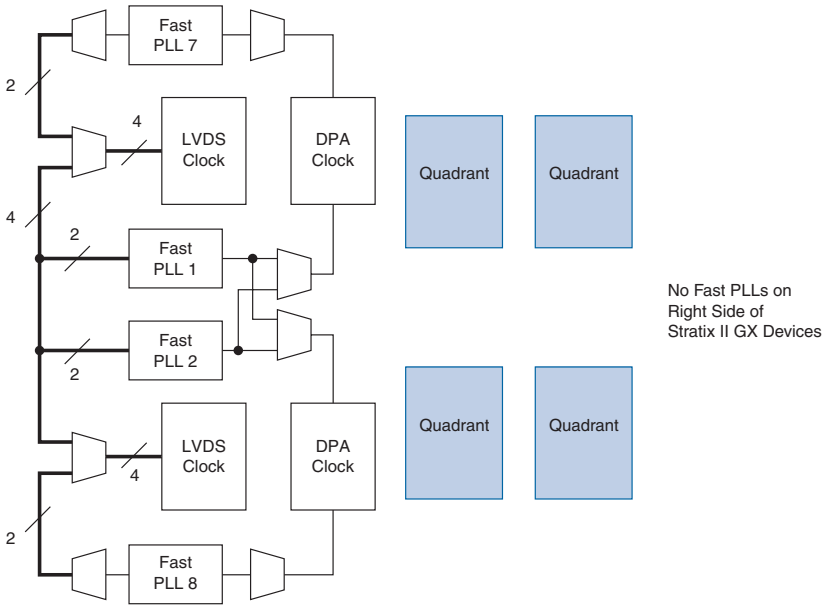


Figure 5–16. Fast PLL and LVDS/DPA Clocks for EP2SGX60E, EP2SGX90 and EP2SGX130 Devices



Source Synchronous Timing Budget

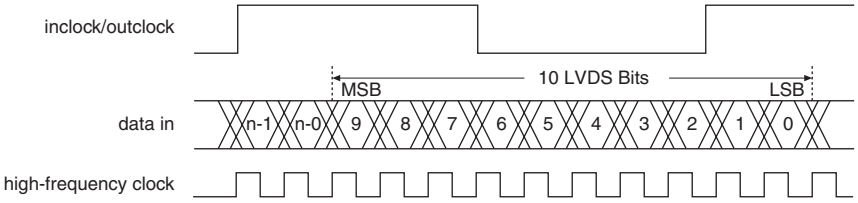
This section discusses the timing budget, waveforms, and specifications for source-synchronous signaling in Stratix II and Stratix II GX devices. LVDS and HyperTransport I/O standards enable high-speed data transmission. This high data transmission rate results in better overall system performance. To take advantage of fast system performance, it is important to understand how to analyze timing for these high-speed signals. Timing analysis for the differential block is different from traditional synchronous timing analysis techniques.

Rather than focusing on clock-to-output and setup times, source-synchronous timing analysis is based on the skew between the data and the clock signals. High-speed differential data transmission requires the use of timing parameters provided by IC vendors and is strongly influenced by board skew, cable skew, and clock jitter. This section defines the source-synchronous differential data orientation timing parameters, the timing budget definitions for Stratix II and Stratix II GX devices, and how to use these timing parameters to determine a design's maximum performance.

Differential Data Orientation

There is a set relationship between an external clock and the incoming data. For operation at 1 Gbps and SERDES factor of 10, the external clock is multiplied by 10, and phase-alignment can be set in the PLL to coincide with the sampling window of each data bit. The data is sampled on the falling edge of the multiplied clock. Figure 5–17 shows the data bit orientation of the ×10 mode.

Figure 5–17. Bit Orientation in the Quartus II Software



Differential I/O Bit Position

Data synchronization is necessary for successful data transmission at high frequencies. Figure 5–18 shows the data bit orientation for a channel operation. These figures are based on the following:

- SERDES factor equals clock multiplication factor
- Edge alignment is selected for phase alignment
- Implemented in hard SERDES

For other serialization factors use the Quartus II software tools and find the bit position within the word. The bit positions after deserialization are listed in Table 5–4.

Figure 5–18 also shows a functional waveform. Timing waveforms may produce different results. Altera recommends performing a timing simulation to predict actual device behavior.

Figure 5–18. Bit Order for One Channel of Differential Data

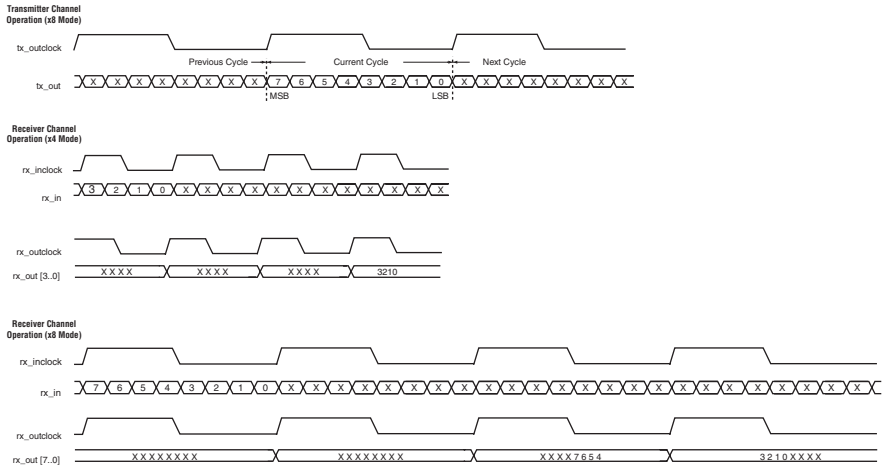


Table 5–4 shows the conventions for differential bit naming for 18 differential channels. The MSB and LSB positions increase with the number of channels used in a system.

Table 5–4. LVDS Bit Naming

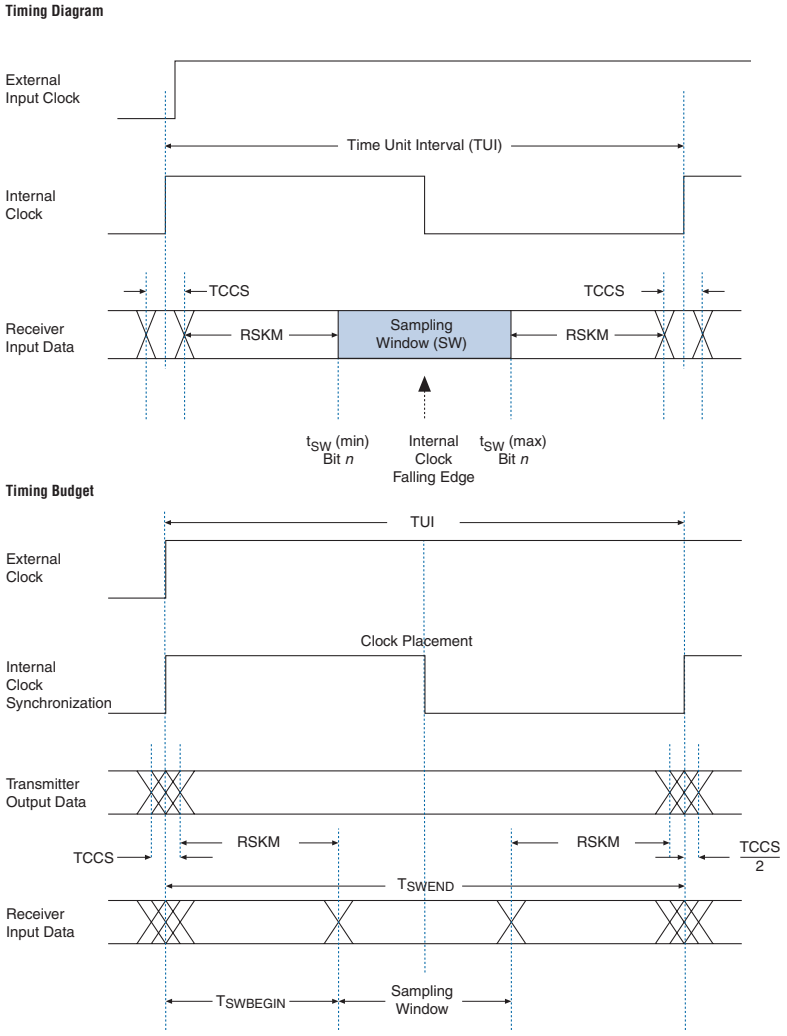
Receiver Channel Data Number	Internal 8-Bit Parallel Data	
	MSB Position	LSB Position
1	7	0
2	15	8
3	23	16
4	31	24
5	39	32
6	47	40
7	55	48
8	63	56
9	71	64
10	79	72
11	87	80
12	95	88
13	103	96
14	111	104
15	119	112
16	127	120
17	135	128
18	143	136

Receiver Skew Margin for Non-DPA

Changes in system environment, such as temperature, media (cable, connector, or PCB) loading effect, the receiver's setup and hold times, and internal skew, reduce the sampling window for the receiver. The timing margin between the receiver's clock input and the data input sampling window is called Receiver Skew Margin (RSKM). Figure 5–19 shows the relationship between the RSKM and the receiver's sampling window.

TCCS, RSKM, and the sampling window specifications are used for high-speed source-synchronous differential signals without DPA. When using DPA, these specifications are exchanged for the simpler single DPA jitter tolerance specification. For instance, the receiver skew is why each input with DPA selects a different phase of the clock, thus removing the requirement for this margin.

Figure 5–19. Differential High-Speed Timing Diagram and Timing Budget for Non-DPA



Differential Pin Placement Guidelines

In order to ensure proper high-speed operation, differential pin placement guidelines have been established. The Quartus II compiler automatically checks that these guidelines are followed and will issue an error message if these guidelines are not met. PLL driving distance information is separated into guidelines with and without DPA usage.

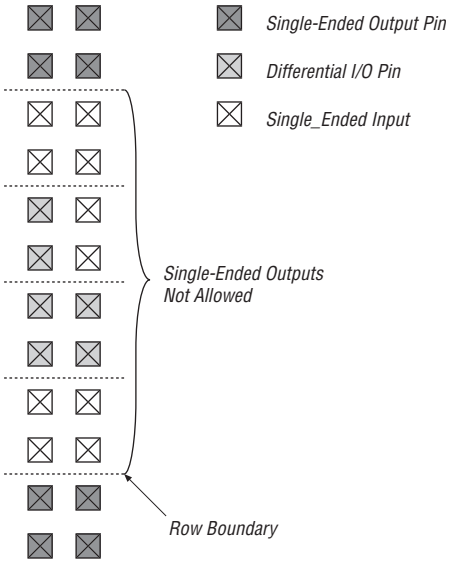
High-Speed Differential I/Os and Single-Ended I/Os

When a differential channel or channels of side banks are used (with or without DPA), you must adhere to the guidelines described in the following sections.

- Single-ended I/Os are allowed in the same bank as the LVDS channels (with or without DPA) as long as the single-ended I/O standard uses the same V_{CCIO} as the LVDS bank.
- Single-ended inputs can be in the same LAB row. Outputs cannot be on the same LAB row with LVDS I/Os. If input registers are used in the IOE, single-ended inputs cannot be in the same LAB row as an LVDS SERDES block.
- LVDS (non-SERDES) I/Os are allowed in the same row as LVDS SERDES but the use of IOE registers are not allowed.
- Single-ended outputs are limited to 120 mA drive strength on LVDS banks (with or without DPA).
    - LVTTL equation for maximum number of I/Os in an LVDS bank:
        - 120 mA = (number of LVTTL outputs) × (drive strength of each LVTTL output)
    - SSTL-2 equation:
        - 120 mA = (number of SSTL-2 I/Os) × (drive strength of each output) ÷ 2
    - LVTTL and SSTL-2 mix equation:
        - 120 mA= (total drive strength of all LVTTL outputs) + (total drive strength of all SSTL2 outputs) ÷ 2
- Single-ended inputs can be in the same LAB row as a differential channel using the SERDES circuitry; however, IOE input registers are not available for the single-ended I/Os placed in the same LAB row as differential I/Os. The same rule for input registers applies for non-SERDES differential inputs placed within the same LAB row as a SERDES differential channel. The input register must be implemented within the core logic. The same rule for input registers applies for non-SERDES differential inputs placed within the same LAB row as a SERDES differential channel.

- Single-ended output pins must be at least one LAB row away from differential output pins, as shown in Figure 5–20.

Figure 5–20. Single-Ended Output Pin Placement with Respect to Differential I/O Pins



DPA Usage Guidelines

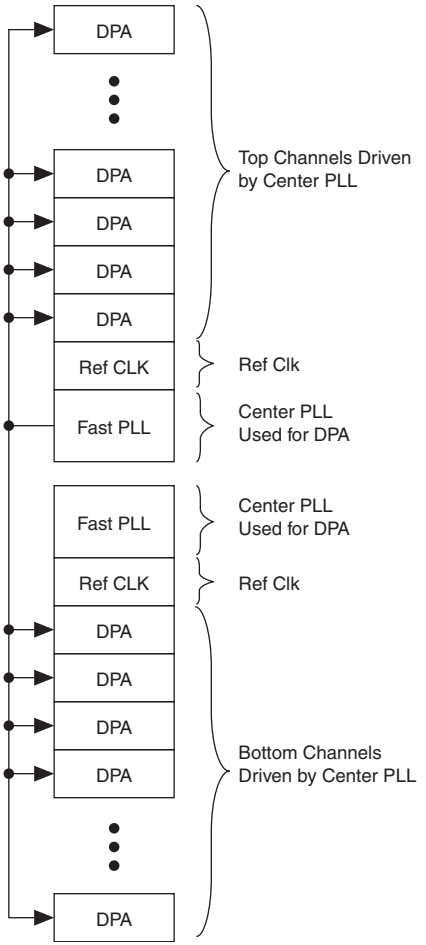
The Stratix II and Stratix II GX device have differential receivers and transmitters on the Row banks of the device. Each receiver has a dedicated DPA circuit to align the phase of the clock to the data phase of its associated channel. When a channel or channels of left or right banks are used in DPA mode, the guidelines listed below must be adhered to.

Fast PLL/DPA Channel Driving Distance

- Each fast PLL can drive up to 25 contiguous rows in DPA mode in a single bank (not including the reference clock row). The unbonded SERDES I/O rows are included in the 25 row calculation. These channels can be anywhere in the bank, their distance from the PLL is not relevant, but the channels must be within 25 rows of each other.

- Unused channels can be within the 25 row span, but all used channels must be in DPA mode from the same fast PLL. Center fast PLLs can drive two I/O banks simultaneously, up to 50 channels (25 on the upper bank and 25 on the lower bank) as shown in Figure 5–21.
- If one center fast PLL drives DPA channels in the upper and lower banks, the other center fast PLL cannot be used for DPA.

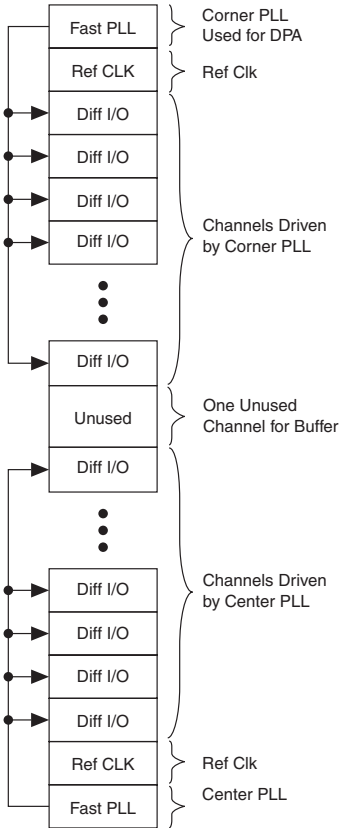
Figure 5–21. Driving Capabilities of a Center Fast PLL



Using Corner and Center Fast PLLs

- If a differential bank is being driven by two fast PLLs, where the corner PLL is driving one group and the center fast PLL is driving another group, there must be at least 1 row of separation between the two groups of DPA channels (see Figure 5–22). The two groups can operate at independent frequencies. Not all the channels are bonded out of the die. Each LAB row is considered a channel, whether or not it has I/O support.
- No separation is necessary if a single fast PLL is driving DPA channels as well as non-DPA channels as long as the DPA channels are contiguous.

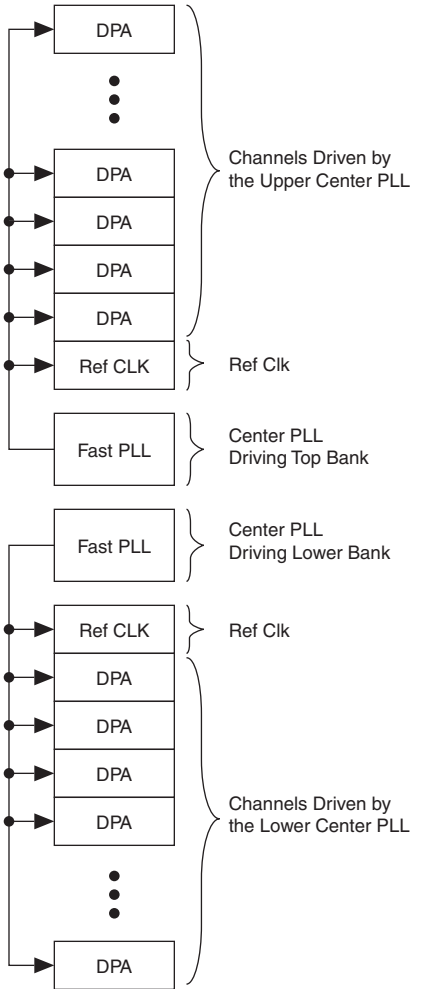
Figure 5–22. Usage of Corner and Center Fast PLLs Driving DPA Channels in a Single Bank



Using Both Center Fast PLLs

- Both center fast PLLs can be used for DPA as long as they drive DPA channels in their adjacent quadrant only. See Figure 5–23.
- Both center fast PLLs cannot be used for DPA if one of the fast PLLs drives the top and bottom banks, or if they are driving cross banks (e.g., the lower fast PLL drives the top bank and the top fast PLL drives the lower bank).

Figure 5–23. Center Fast PLL Usage When Driving DPA Channels



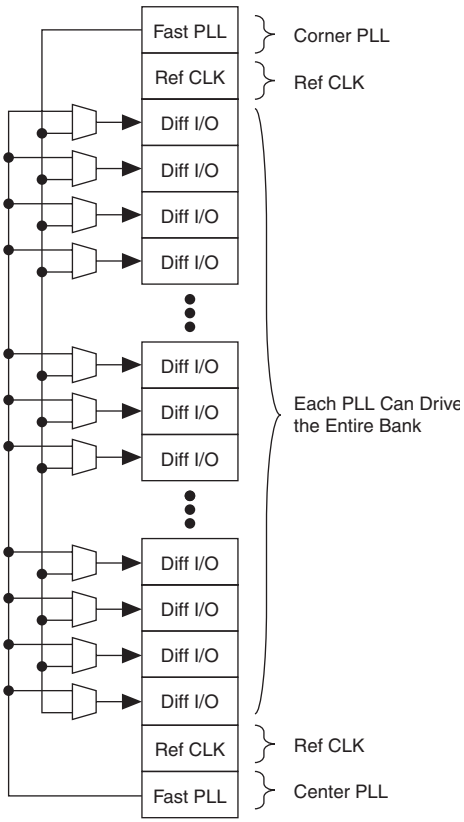
Non-DPA Differential I/O Usage Guidelines

When a differential channel or channels of left or right banks are used in non-DPA mode, you must adhere to the guidelines in the following sections.

Fast PLL/Differential I/O Driving Distance

- As shown in Figure 5–24, each fast PLL can drive all the channels in the entire bank.

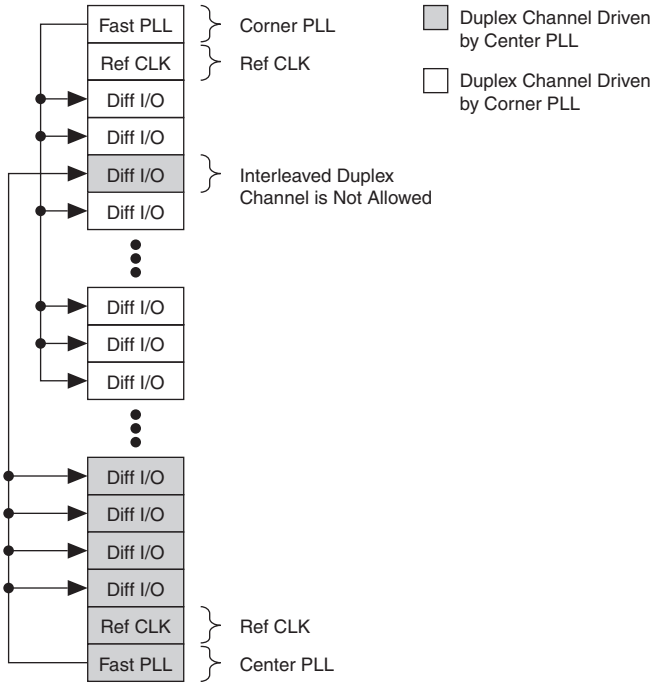
Figure 5–24. Fast PLL Driving Capability When Driving Non-DPA Differential Channels



Using Corner and Center Fast PLLs

- The corner and center fast PLLs can be used as long as the channels driven by separate fast PLLs do not have their transmitter or receiver channels interleaved. Figure 5–25 shows illegal placement of differential channels when using corner and center fast PLLs.
- If one fast PLL is driving transmitter channels only, and the other fast PLL drives receiver channels only, the channels driven by those fast PLLs can overlap each other.
- Center fast PLLs can be used for both transmitter and receiver channels.

Figure 5–25. Illegal Placement of Interlaced Duplex Channels in an I/O Bank



Board Design Considerations

This section explains how to achieve the optimal performance from the Stratix II and Stratix II GX high-speed I/O block and ensure first-time success in implementing a functional design with optimal signal quality.

For more information on board layout recommendations and I/O pin terminations, refer to *AN 224: High-Speed Board Layout Guidelines*.

To achieve the best performance from the device, pay attention to the impedances of traces and connectors, differential routing, and termination techniques.

Use this section together with the *Stratix II Device Family Data Sheet* in volume 1 of the *Stratix II Device Handbook*.

The Stratix II and Stratix II GX high-speed module generates signals that travel over the media at frequencies as high as one Gbps. Board designers should use the following guidelines:

- Base board designs on controlled differential impedance. Calculate and compare all parameters such as trace width, trace thickness, and the distance between two differential traces.
- Place external reference resistors as close to receiver input pins as possible.
- Use surface mount components.
- Avoid 90° or 45° corners.
- Use high-performance connectors such as HMZD or VHDM connectors for backplane designs. Two suppliers of high-performance connectors are Teradyne Corp (**www.teradyne.com**) and Tyco International Ltd. (**www.tyco.com**).
- Design backplane and card traces so that trace impedance matches the connector's or the termination's impedance.
- Keep an equal number of vias for both signal traces.
- Create equal trace lengths to avoid skew between signals. Unequal trace lengths also result in misplaced crossing points and system margins when the TCCS value increases.
- Limit vias, because they cause impedance discontinuities.
- Use the common bypass capacitor values such as 0.001, 0.01, and 0.1 µF to decouple the fast PLL power and ground planes. You can also use 0.0047 µF and 0.047 µF.
- Keep switching TTL signals away from differential signals to avoid possible noise coupling.
- Do not route TTL clock signals to areas under or above the differential signals.
- Route signals on adjacent layers orthogonally to each other.

Conclusion

Stratix II and Stratix II GX high-speed differential inputs and outputs, with their DPA and data realignment circuitry, allow users to build a robust multi-Gigabit system. The DPA circuitry allows users to compensate for any timing skews resulting from physical layouts. The data realignment circuitry allows the devices to align the data packet between the transmitter and receiver. Together with the on-chip differential termination, Stratix II and Stratix II GX devices can be used as a single-chip solution for high-speed applications.

Referenced Documents

This chapter references the following documents:

- *AN 224: High-Speed Board Layout Guidelines*
- *DC & Switching Characteristics* chapter in volume 1 of the *Stratix II Device Handbook*
- *DC & Switching Characteristics* chapter in volume 1 of the *Stratix II GX Device Handbook*
- *PLLs in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Handbook*
- *PLLs in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Handbook*
- *Selectable I/O standards in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook*
- *Stratix II Device Family Data Sheet* in volume 1 of the *Stratix II Device Handbook*

Document Revision History

Table 5–5 shows the revision history for this chapter.

Table 5–5. Document Revision History (Part 1 of 2)

Date and Document Version	Changes Made	Summary of Changes
January 2008, v2.2	Updated Figure 5–2.	—
	Added "Referenced Documents" section.	—
	Minor text edits.	—
	Added Figure 5–9.	—
	Updated "Receiver Data Realignment Circuit".	—
	For the *Stratix II GX Device Handbook* only: Formerly chapter 10. The chapter number changed due to the addition of the *Stratix II GX Dynamic Reconfiguration* chapter.	—
May 2007, v2.1	Updated entire chapter to include Stratix II GX information.	—
	Changed chapter part number.	—
	Fixed two types in "High-Speed Differential I/Os and Single-Ended I/Os" section	—

Table 5–5. Document Revision History (Part 2 of 2)

Date and Document Version	Changes Made	Summary of Changes
February 2007 v2.0	This chapter changed from High-Speed, Source-Synchronous Differential I/O Interfaces in Stratix II GX Devices to "High-Speed Differential I/O Interfaces with DPA in Stratix II and Stratix II GX Devices".	—
	Added the "Document Revision History" section to this chapter.	—
	Added "and Stratix II GX" after each instance of "Stratix II".	—
	Updated Figures 10–4, 10–20, 10–22.	—
	Updated Note (4) of Figure 10–2.	—
	Updated Table 10–1.	—
	Updated the following sections: • "I/O Banks" • "Differential I/O Termination" • "Fast PLL " • "Differential I/O Bit Position" • "DPA Usage Guidelines" • "Fast PLL/DPA Channel Driving Distance"	—
	Updated Note (1) of Tables 10–2 and 10–3.	—
	Added Note (5) to Figure 10–11.	—
	Added Table 10–3.	—
	Added Figures 10–14, 10–15, 10–19.	—
	Deleted old section called High-Speed Differential I/Os and Single-Ended I/Os and added a new "High-Speed Differential I/Os and Single-Ended I/Os" section.	—
	Deleted DPA and Single-Ended I/Os section.	—
	Updated title and added Note (1) to Figure 10–12.	—
	Added Note (1) to Figure 10–13.	—
April 2006, v1.2	• Updated all the MegaWizard Plug-In Manager figures to match the Quartus II software GUI. • Updated "Dedicated Source-Synchronous Circuitry" section, including Table 10–3.	—
February 2006, v1.1	• Updated chapter number from 9 to 10. • Updated Figures 10–11 and 10–12.	—
October 2005 v1.0	Added chapter to the *Stratix II GX Device Handbook*.	—