Section IV. I/O Standards

This section provides information about the I/O standards and interfaces for Stratix and Stratix® GX devices.

This section includes the following chapters:

- Chapter 16, Selectable I/O Standards in Stratix & Stratix GX Devices
- Chapter 17, High-Speed Source-Synchronous Differential I/O Interfaces in Stratix GX Devices

Revision History

The table below shows the revision history for Chapters 16 and 17.

Chapter(s)	Date / Version	Changes Made
16	June 2006, v3.4	Chapter updated as part of the *Stratix Device Handbook* update.
	July 2005, v3.3	Updated as part of the *Stratix Device Handbook* update.
	January 2005, v3.2	Added document to *Stratix GX Device Handbook*.
17	June 2006, v1.2	• Updated "DPA Input Support" section. • Updated "Receiver Data Realignment In DPA Mode" section. • Updated the "Software Support" section, including updating the MegaWizard Plug-In Manager figures to match the Quartus II software GUI.
	August 2005, v1.1	Updated Table 17-3.

16. Selectable I/O Standards in Stratix & Stratix GX Devices

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Introduction

The proliferation of I/O standards and the need for higher I/O performance have made it critical that devices have flexible I/O capabilities. Stratix® and Stratix GX programmable logic devices (PLDs) feature programmable I/O pins that support a wide range of industry I/O standards, permitting increased design flexibility. These I/O capabilities enable fast time-to-market and high-performance solutions to meet the demands of complex system designs. Additionally, Stratix and Stratix GX devices simplify system board design and make it easy to connect to microprocessors, peripherals, memories, gate arrays, programmable logic circuits, and standard logic functions.

This chapter provides guidelines for using one or more industry I/O standards in Stratix and Stratix GX devices, including:

- Stratix and Stratix GX I/O standards
- High-speed interfaces
- Stratix and Stratix GX I/O banks
- Programmable current drive strength
- Hot socketing
- Differential on-chip termination
- I/O pad placement guidelines
- Quartus® II software support

Stratix & Stratix GX I/O Standards

Stratix and Stratix GX devices support a wide range of industry I/O standards as shown in the *Stratix Device Family Data Sheet* section in the *Stratix Device Handbook, Volume 1* and the *Stratix GX Device Family Data Sheet* section of the *Stratix GX Device Handbook, Volume 1*. Several applications that use these I/O standards are listed in Table 16–1.

Table 16–1. I/O Standard Applications & Performance (Part 1 of 2) Note (1)

I/O Standard	Application	Performance
3.3-V LVTTL/LVCMOS	General purpose	350 MHz
2.5-V LVTTL/LVCMOS	General purpose	350 MHz
1.8-V LVTTL/LVCMOS	General purpose	250 MHz
1.5-V LVCMOS	General purpose	225 MHz
PCI/CompactPCI	PC/embedded systems	66 MHz

Table 16–1. I/O Standard Applications & Performance (Part 2 of 2) Note (1)

I/O Standard	Application	Performance
PCI-X 1.0	PC/embedded systems	133 MHz
AGP 1× and 2×	Graphics processors	66 to 133 MHz
SSTL-3 Class I and II	SDRAM	167 MHz
SSTL-2 Class I and II	DDR I SDRAM	160 to 400 Mbps
HSTL Class I	QDR SRAM/SRAM/CSIX	150 to 225 MHz
HSTL Class II	QDR SRAM/SRAM/CSIX	150 to 250 MHz
Differential HSTL	Clock interfaces	150 to 225 MHz
GTL	Backplane driver	200 MHz
GTL+	Pentium processor interface	133 to 200 MHz
LVDS	Communications	840 Mbps
HyperTransport technology	Motherboard interfaces	800 Mbps
LVPECL	PHY interface	840 Mbps
PCML	Communications	840 Mbps
Differential SSTL-2	DDR I SDRAM	160 to 400 Mbps
CTT	Back planes and bus interfaces	200 MHz

Note to Table 16–1:

(1) These performance values are dependent on device speed grade, package type (flip-chip or wirebond) and location of I/Os (top/bottom or left/right). See the *DC & Switching Characteristics* chapter of the *Stratix Device Handbook, Volume 1*.

3.3-V Low Voltage Transistor-Transistor Logic (LVTTL) - EIA/JEDEC Standard JESD8-B

The 3.3-V LVTTL I/O standard is a general-purpose, single-ended standard used for 3.3-V applications. The LVTTL standard defines the DC interface parameters for digital circuits operating from a 3.0-V or 3.3-V power supply and driving or being driven by LVTTL-compatible devices.

The LVTTL input standard specifies a wider input voltage range of $-0.5\ V \leq V_I \leq 3.8\ V$. Altera allows an input voltage range of $-0.5\ V \leq V_I \leq 4.1\ V$. The LVTTL standard does not require input reference voltages or board terminations.

Stratix and Stratix GX devices support both input and output levels for 3.3-V LVTTL operation.

3.3-V LVCMOS - EIA/JEDEC Standard JESD8-B

The 3.3-V low voltage complementary metal oxide semiconductor (LVCMOS) I/O standard is a general-purpose, single-ended standard used for 3.3-V applications. The LVCMOS standard defines the DC interface parameters for digital circuits operating from a 3.0-V or 3.3-V power supply and driving or being driven by LVCMOS-compatible devices.

The LVCMOS standard specifies the same input voltage requirements as LVTTL (–0.5 V $\leq V_I \leq$ 3.8 V). The output buffer drives to the rail to meet the minimum high-level output voltage requirements. The 3.3-V I/O standard does not require input reference voltages or board terminations.

Stratix and Stratix GX devices support both input and output levels for 3.3-V LVCMOS operation.

2.5-V LVTTL Normal Voltage Range - EIA/JEDEC Standard EIA/JESD8-5

The 2.5-V I/O standard is used for 2.5-V LVTTL applications. This standard defines the DC interface parameters for high-speed, low-voltage, non-terminated digital circuits driving or being driven by other 2.5-V devices. The input and output voltage ranges are:

- The 2.5-V normal range input standards specify an input voltage range of – 0.3 V $\leq V_I \leq$ 3.0 V.
- The normal range minimum high-level output voltage requirement (V_{OH}) is 2.1 V.

Stratix and Stratix GX devices support both input and output levels for 2.5-V LVTTL operation.

2.5-V LVCMOS Normal Voltage Range - EIA/JEDEC Standard EIA/JESD8-5

The 2.5-V I/O standard is used for 2.5-V LVCMOS applications. This standard defines the DC interface parameters for high-speed, low-voltage, non-terminated digital circuits driving or being driven by other 2.5-V parts. The input and output voltage ranges are:

- The 2.5-V normal range input standards specify an input voltage range of – 0.5 V $\leq V_I \leq$ 3.0 V.
- The normal range minimum V_{OH} requirement is 2.1 V.

Stratix and Stratix GX devices support both input and output levels for 2.5-V LVCMOS operation.

1.8-V LVTTL Normal Voltage Range - EIA/JEDEC Standard EIA/JESD8-7

The 1.8-V I/O standard is used for 1.8-V LVTTL applications. This standard defines the DC interface parameters for high-speed, low-voltage, non-terminated digital circuits driving or being driven by other 1.8-V parts. The input and output voltage ranges are:

- The 1.8-V normal range input standards specify an input voltage range of – 0.5 V $\leq V_I \leq$ 2.3 V.
- The normal range minimum V_{OH} requirement is V_{CCIO} – 0.45 V.

Stratix and Stratix GX devices support both input and output levels for 1.8-V LVTTL operation.

1.8-V LVCMOS Normal Voltage Range - EIA/JEDEC Standard EIA/JESD8-7

The 1.8-V I/O standard is used for 1.8-V LVCMOS applications. This standard defines the DC interface parameters for high-speed, low-voltage, non-terminated digital circuits driving or being driven by other 1.8-V devices. The input and output voltage ranges are:

- The 1.8-V normal range input standards specify an input voltage range of – 0.5 V $\leq V_I \leq$ 2.5 V.
- The normal range minimum V_{OH} requirement is V_{CCIO} – 0.45 V.

Stratix and Stratix GX devices support both input and output levels for 1.8-V LVCMOS operation.

1.5-V LVCMOS Normal Voltage Range - EIA/JEDEC Standard JESD8-11

The 1.5-V I/O standard is used for 1.5-V applications. This standard defines the DC interface parameters for high-speed, low-voltage, non-terminated digital circuits driving or being driven by other 1.5-V devices. The input and output voltage ranges are:

- The 1.5-V normal range input standards specify an input voltage range of – 0.5 V $\leq V_I \leq$ 2.0 V.
- The normal range minimum V_{OH} requirement is 1.05 V.

Stratix and Stratix GX devices support both input and output levels for 1.5-V LVCMOS operation.

1.5-V HSTL Class I & II - EIA/JEDEC Standard EIA/JESD8-6

The high-speed transceiver logic (HSTL) I/O standard is used for applications designed to operate in the 0.0- to 1.5-V HSTL logic switching range. This standard defines single ended input and output specifications for all HSTL-compliant digital integrated circuits. The single ended input standard specifies an input voltage range of $-0.3\ V \le V_I \le V_{CCIO} + 0.3\ V$. Stratix and Stratix GX devices support both input and output levels specified by the 1.5-V HSTL I/O standard. The input clock is implemented using dedicated differential input buffers. Two single-ended output buffers are automatically programmed to have opposite polarity so as to implement a differential output clock. Additionally, the 1.5-V HSTL I/O standard in Stratix and Stratix GX devices is compatible with the 1.8-V HSTL I/O standard in APEX™ 20KE and APEX 20KC devices because the input and output voltage thresholds are compatible. See Figures 16–1 and 16–2. Stratix and Stratix GX devices support both input and output levels with V_{REF} and V_{TT}.

Figure 16–1. HSTL Class I Termination

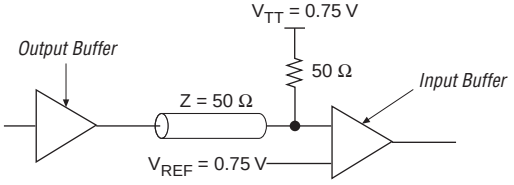
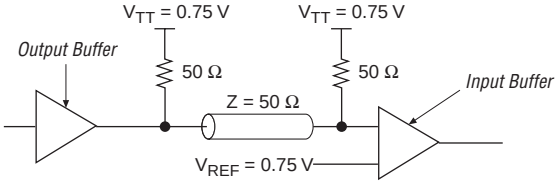


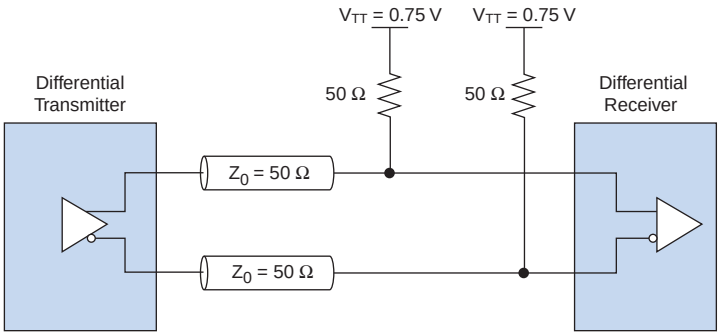
Figure 16–2. HSTL Class II Termination



1.5-V Differential HSTL - EIA/JEDEC Standard EIA/JESD8-6

The differential HSTL I/O standard is used for applications designed to operate in the 0.0- to 1.5-V HSTL logic switching range such as quad data rate (QDR) memory clock interfaces. The differential HSTL specification is the same as the single ended HSTL specification. The standard specifies an input voltage range of $-0.3\ V \le V_I \le V_{CCIO} + 0.3\ V$. Differential HSTL does not require an input reference voltage, however, it does require a 50 Ω resistor termination resistor to V_{TT} at the input buffer (see Figure 16–3). Stratix and Stratix GX devices support both input and output clock levels for 1.5-V differential HSTL. The input clock is implemented using dedicated differential input buffer. Two single-ended output buffers are automatically programmed to have opposite polarity so as to implement a differential output clock.

Figure 16–3. 1.5-V Differential HSTL Class I Termination



3.3-V PCI Local Bus - PCI Special Interest Group PCI Local Bus Specification Rev. 2.3

The PCI local bus specification is used for applications that interface to the PCI local bus, which provides a processor-independent data path between highly integrated peripheral controller components, peripheral add-in boards, and processor/memory systems. The conventional PCI specification revision 2.3 defines the PCI hardware environment including the protocol, electrical, mechanical, and configuration specifications for the PCI devices and expansion boards. This standard requires 3.3-V V_{CCIO}. Stratix and Stratix GX devices are fully compliant with the 3.3-V *PCI Local Bus Specification Revision 2.3* and meet 64-bit/66-MHz operating frequency and timing requirements. The 3.3-V PCI standard does not require input reference voltages or board terminations. Stratix and Stratix GX devices support both input and output levels.

3.3-V PCI-X 1.0 Local Bus - PCI-SIG PCI-X Local Bus Specification Revision 1.0a

The PCI-X 1.0 standard is used for applications that interface to the PCI local bus. The standard enables the design of systems and devices that operate at clock speeds up to 133 MHz, or 1 gigabit per second (Gbps) for a 64-bit bus. The PCI-X 1.0 protocol enhancements enable devices to operate much more efficiently, providing more usable bandwidth at any clock frequency. By using the PCI-X 1.0 standard, devices can be designed to meet PCI-X 1.0 requirements and operate as conventional 33- and 66-MHz PCI devices when installed in those systems. This standard requires 3.3-V $V_{CCIO.}$ Stratix and Stratix GX devices are fully compliant with the 3.3-V *PCI-X Specification Revision 1.0a* and meet the 133-MHz operating frequency and timing requirements. The 3.3-V PCI standard does not require input reference voltages or board terminations. Stratix and Stratix GX devices support both input and output levels.

3.3-V Compact PCI Bus - PCI SIG PCI Local Bus Specification Revision 2.3

The Compact PCI local bus specification is used for applications that interface to the PCI local bus. It follows the *PCI Local Bus Specification Revision 2.3* plus additional requirements in PCI Industrial Computers Manufacturing Group (PICMG) specifications PICMG 2.0 R3.0, CompactPCI specification, and the hot swap requirements in PICMG 2.1 R2.0, CompactPCI Hot Swap Specification. This standard has similar electrical requirements as LVTTL and requires 3.3-V $V_{CCIO.}$ Stratix and Stratix GX devices are compliant with the Compact PCI electrical requirements. The 3.3-V PCI standard does not require input reference voltages or board terminations. Stratix and Stratix GX devices support both input and output levels.

3.3-V 1× AGP - Intel Corporation Accelerated Graphics Port Interface Specification 2.0

The AGP interface is a platform bus specification that enables high-performance graphics by providing a dedicated high-speed port for the movement of large blocks of 3-dimensional texture data between a PC's graphics controller and system memory. The 1× AGP I/O standard is a single-ended standard used for 3.3-V graphics applications. The 1× AGP input standard specifies an input voltage range of $-0.5\ V \leq V_I \leq V_{CCIO} + 0.5\ V$. The 1× AGP standard does not require input reference voltages or board terminations. Stratix and Stratix GX devices support both input and output levels.

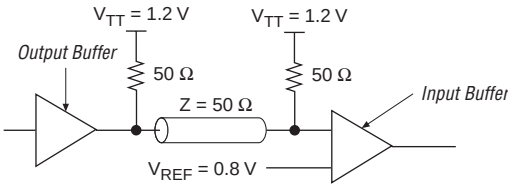
3.3-V 2× AGP - Intel Corporation Accelerated Graphics Port Interface Specification 2.0

The 2× AGP I/O standard is a voltage-referenced, single-ended standard used for 3.3-V graphics applications. The 2× AGP input standard specifies an input voltage range of $-0.5V \leq V_I \leq V_{CCIO} + 0.5V$. The 2× AGP standard does not require board terminations. Stratix and Stratix GX devices support both input and output levels.

GTL - EIA/JEDEC Standard EIA/JESD8-3

The GTL I/O standard is a low-level, high-speed back plane standard used for a wide range of applications from ASICs and processors to interface logic devices. The GTL standard defines the DC interface parameters for digital circuits operating from power supplies of 2.5, 3.3, and 5.0 V. The GTL standard is an open-drain standard, and Stratix and Stratix GX devices support a 2.5- or 3.3-V V_{CCIO} to meet this standard. GTL requires a 0.8-V V_{REF} and open-drain outputs with a 1.2-V V_{TT} (see Figure 16–4). Stratix and Stratix GX devices support both input and output levels.

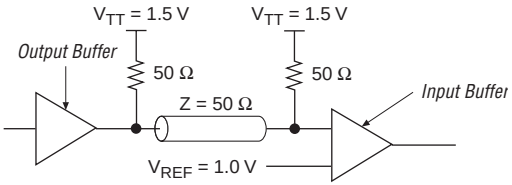
Figure 16–4. GTL Termination



GTL+

The GTL+ I/O standard is used for high-speed back plane drivers and Pentium processor interfaces. The GTL+ standard defines the DC interface parameters for digital circuits operating from power supplies of 2.5, 3.3, and 5.0 V. The GTL+ standard is an open-drain standard, and Stratix and Stratix GX devices support a 2.5- or 3.3-V V_{CCIO} to meet this standard. GTL+ requires a 1.0-V V_{REF} and open-drain outputs with a 1.5-V V_{TT} (see Figure 16–5). Stratix and Stratix GX devices support both input and output levels.

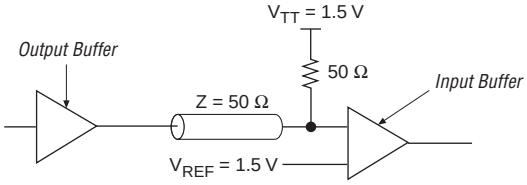
Figure 16–5. GTL+ Termination



CTT - EIA/JEDEC Standard JESD8-4

The CTT I/O standard is used for backplanes and memory bus interfaces. The CTT standard defines the DC interface parameters for digital circuits operating from 2.5- and 3.3-V power supplies. The CTT standard does not require special circuitry to interface with LVTTL or LVCMOS devices when the CTT driver is not terminated. The CTT standard requires a 1.5-V V_{REF} and a 1.5-V V_{TT} (see Figure 16–6). Stratix and Stratix GX devices support both input and output levels.

Figure 16–6. CTT Termination



SSTL-3 Class I & II - EIA/JEDEC Standard JESD8-8

The SSTL-3 I/O standard is a 3.3-V memory bus standard used for applications such as high-speed SDRAM interfaces. This standard defines the input and output specifications for devices that operate in the SSTL-3 logic switching range of 0.0 to 3.3 V. The SSTL-3 standard specifies an input voltage range of $-0.3\ V \le V_I \le V_{CCIO} + 0.3\ V$. SSTL-3 requires a 1.5-V V_{REF} and a 1.5-V V_{TT} to which the series and termination resistors are connected (see Figures 16–7 and 16–8). Stratix and Stratix GX devices support both input and output levels.

Figure 16–7. SSTL-3 Class I Termination

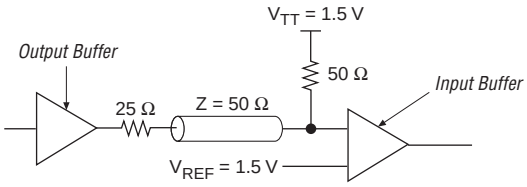
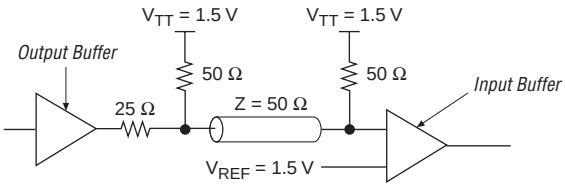


Figure 16–8. SSTL-3 Class II Termination



SSTL-2 Class I & II - EIA/JEDEC Standard JESD8-9A

The SSTL-2 I/O standard is a 2.5-V memory bus standard used for applications such as high-speed DDR SDRAM interfaces. This standard defines the input and output specifications for devices that operate in the SSTL-2 logic switching range of 0.0 to 2.5 V. This standard improves operation in conditions where a bus must be isolated from large stubs. The SSTL-2 standard specifies an input voltage range of $-0.3\ V \le V_I \le V_{CCIO} + 0.3\ V$. SSTL-2 requires a 1.25-V V_{REF} and a 1.25-V V_{TT} to which the series and termination resistors are connected (see Figures 16–9 and 16–10). Stratix and Stratix GX devices support both input and output levels.

Figure 16–9. SSTL-2 Class I Termination

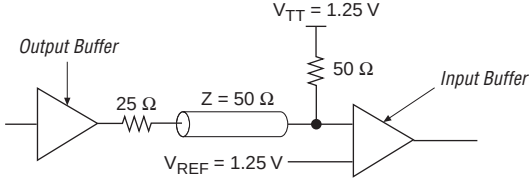
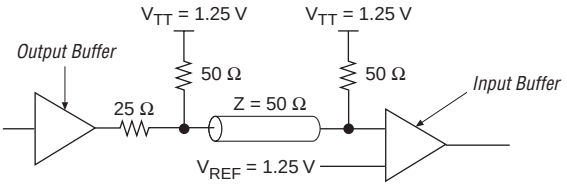


Figure 16–10. SSTL-2 Class II Termination



SSTL-18 Class I & II - EIA/JEDEC Preliminary Standard JC42.3

The SSTL-18 I/O standard is a 1.8-V memory bus standard. This standard is similar to SSTL-2 and defines input and output specifications for devices that are designed to operate in the SSTL-18 logic switching range 0.0 to 1.8 V. SSTL-18 requires a 0.9-V V_{REF} and a 0.9-V V_{TT} to which the series and termination resistors are connected. See Figures 16–11 and 16–12 for details on SSTL-18 Class I and II termination. Stratix and Stratix GX devices support both input and output levels.

Figure 16–11. SSTL-18 Class I Termination

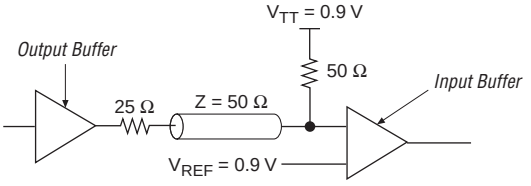
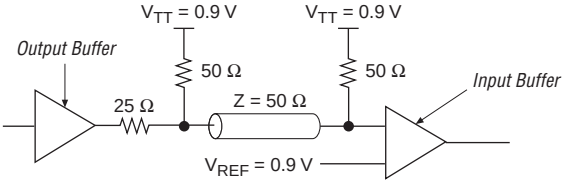


Figure 16–12. SSTL-18 Class II Termination

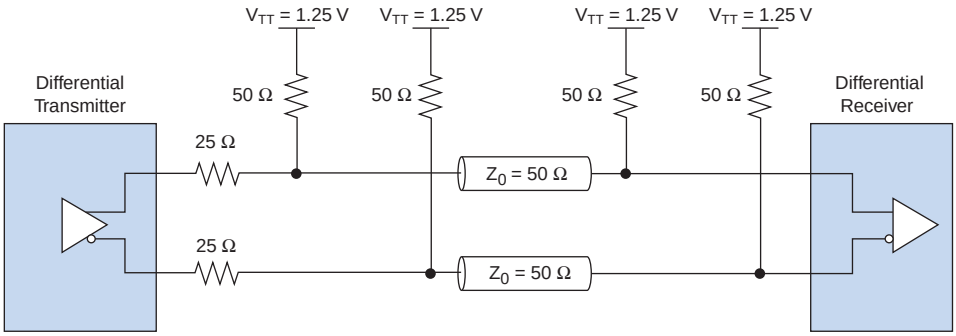


Differential SSTL-2 - EIA/JEDEC Standard JESD8-9A

The differential SSTL-2 I/O standard is a 2.5-V standard used for applications such as high-speed DDR SDRAM clock interfaces. This standard supports differential signals in systems using the SSTL-2

standard and supplements the SSTL-2 standard for differential clocks. The differential SSTL-2 standard specifies an input voltage range of $-0.3\ V \le V_I \le V_{CCIO} + 0.3\ V$. The differential SSTL-2 standard does not require an input reference voltage differential. See Figure 16–13 for details on differential SSTL-2 termination. Stratix and Stratix GX devices support output clock levels for differential SSTL-2 Class II operation. The output clock is implemented using two single-ended output buffers which are programmed to have opposite polarity.

Figure 16–13. Differential SSTL-2 Class II Termination



LVDS - ANSI/TIA/EIA Standard ANSI/TIA/EIA-644

The LVDS I/O standard is a differential high-speed, low-voltage swing, low-power, general-purpose I/O interface standard requiring a 3.3-V V_{CCIO}. This standard is used in applications requiring high-bandwidth data transfer, backplane drivers, and clock distribution. The ANSI/TIA/EIA-644 standard specifies LVDS transmitters and receivers capable of operating at recommended maximum data signaling rates of 655 Mbps. However, devices can operate at slower speeds if needed, and there is a theoretical maximum of 1.923 Gbps. Stratix and Stratix GX devices meet the ANSI/TIA/EIA-644 standard.

Due to the low voltage swing of the LVDS I/O standard, the electromagnetic interference (EMI) effects are much smaller than CMOS, TTL, and PECL. This low EMI makes LVDS ideal for applications with low EMI requirements or noise immunity requirements. The LVDS standard does not require an input reference voltage, however, it does require a 100 Ω termination resistor between the two signals at the input buffer. Stratix and Stratix GX devices include an optional differential LVDS termination resistor within the device using differential on-chip termination. Stratix and Stratix GX devices support both input and output levels.

For more information on the LVDS I/O standard in Stratix devices, see the *High-Speed Differential I/O Interfaces in Stratix Devices* chapter.

LVPECL

The LVPECL I/O standard is a differential interface standard requiring a 3.3-V V_{CCIO}. The standard is used in applications involving video graphics, telecommunications, data communications, and clock distribution. The high-speed, low-voltage swing LVPECL I/O standard uses a positive power supply and is similar to LVDS, however, LVPECL has a larger differential output voltage swing than LVDS. The LVPECL standard does not require an input reference voltage, but it does require a 100-Ω termination resistor between the two signals at the input buffer. See Figures 16–14 and 16–15 for two alternate termination schemes for LVPECL. Stratix and Stratix GX devices support both input and output levels.

Figure 16–14. LVPECL DC Coupled Termination

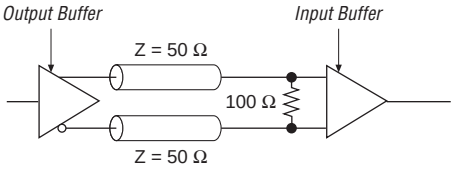
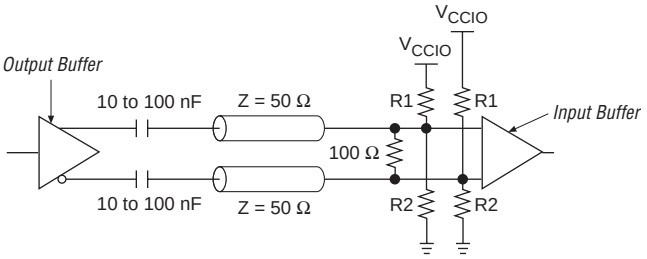


Figure 16–15. LVPECL AC Coupled Termination



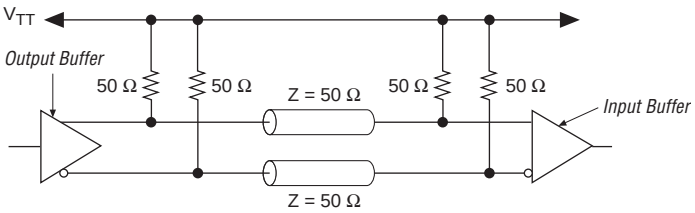
Pseudo Current Mode Logic (PCML)

The PCML I/O standard is a differential high-speed, low-power I/O interface standard used in applications such as networking and telecommunications. The standard requires a 3.3-V V_{CCIO}. The PCML I/O standard consumes less power than the LVPECL I/O standard. The

PCML standard is similar to LVPECL, but PCML has a reduced voltage swing, which allows for a faster switching time and lower power consumption. The PCML standard uses open drain outputs and requires a differential output signal. See Figure 16–16 for details on PCML termination. Stratix and Stratix GX devices support both input and output levels.

Additionally, Stratix GX devices support 1.5-V PCML as described in the *Stratix GX Device Handbook, Volume 1*.

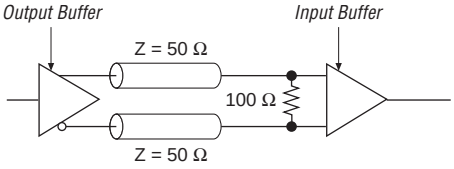
Figure 16–16. PCML Termination



HyperTransport Technology - HyperTransport Consortium

The HyperTransport technology I/O standard is a differential high-speed, high-performance I/O interface standard requiring a 2.5-V V_{CCIO}. This standard is used in applications such as high-performance networking, telecommunications, embedded systems, consumer electronics, and Internet connectivity devices. The HyperTransport technology I/O standard is a point-to-point standard in which each HyperTransport technology bus consists of two point-to-point unidirectional links. Each link is 2 to 32 bits. The HyperTransport technology standard does not require an input reference voltage. However, it does require a 100-Ω termination resistor between the two signals at the input buffer. See Figure 16–17 for details on HyperTransport technology termination. Stratix and Stratix GX devices support both input and output levels.

Figure 16–17. HyperTransport Technology Termination



See the *Stratix Device Family Data Sheet* section in the *Stratix Device Handbook, Volume 1*; the *Stratix GX Device Family Data Sheet* section of the *Stratix GX Device Handbook, Volume 1*; and the *High-Speed Differential I/O Interfaces in Stratix Devices* chapter for more information on differential I/O standards.

High-Speed Interfaces

In addition to current industry physical I/O standards, Stratix and Stratix GX devices also support a variety of emerging high-speed interfaces. This section provides an overview of these interfaces.

OIF-SPI4.2

This implementation agreement is widely used in the industry for OC-192 and 10-Gbps multi-service system interfaces. SONET and SDH are synchronous transmission systems over which data packets are transferred. POS-PHY Level 4 is a standard interface for switches and routers, and defines the operation between a physical layer (PHY) device and link layer devices (ATM, Internet protocol, and Gigabit Ethernet) for bandwidths of OC-192 ATM, POS, and 10-Gigabit Ethernet applications. Some key POS-PHY Level 4 system features include:

- Large selection of POS-PHY Level 4-based PHYs
- Independent of data protocol
- Wide industry support
- LVDS I/O standard to improve signal integrity
- Inband addressing/control
- Out of band flow control
- Scalable architecture
- Over 622-Mbps operation
- Dynamic interface timing mode

POS-PHY Level 4 operates at a wide range of frequencies.

OIF-SFI4.1

This implementation agreement is widely used in the industry for interfacing physical layer (PHY) to the serializer-deserializer (SERDES) devices in OC-192 and 10 Gbps multi-service systems. The POS-PHY Level 4 interface standard defines the SFI-4 standard. POS-PHY Level 4: SFI-4 is a standardized 16-bit × 622-Mbps line-side interface for 10-Gbps applications. Internet LAN and WAN architectures use telecommunication SONET protocols for data transferring data over the PHY layer. SFI-4 interfaces between OC-192 SERDES and SONET framers.

10 Gigabit Ethernet Sixteen Bit Interface (XSBI) - IEEE Draft Standard P802.3ae/D2.0

10 Gigabit Ethernet XSBI is an interface standard for LANs, metropolitan area networks (MANs), storage area networks (SANs), and WANs. 10 Gigabit Ethernet XSBI provides many features for efficient, effective high-speed networking, including easy migration to higher performance levels without disruption, lower cost of ownership including acquisition and support versus other alternatives, familiar management tools and common skills, ability to support new applications and data protocols, flexibility in network design, and multiple vendor sourcing and interoperability.

Under the ISO Open Systems Interconnection (OSI) model, Ethernet is a Layer 2 protocol. 10 Gigabit Ethernet XSBI uses the IEEE 802.3 Ethernet media access control (MAC) protocol, Ethernet frame format, and the minimum/maximum frame size. An Ethernet PHY corresponding to OSI layer 1 connects the media to the MAC layer that corresponds to OSI layer 2. The PHY is divided into a physical media dependent (PMD) element, such as optical transceivers, and a physical coding sub-layer (PCS), which has coding and a serializer/multiplexor. This standard defines two PHY types, including the LAN PHY and the WAN PHY, which are distinguished by the PCS. The 10 Gigabit Ethernet XSBI standard is a full-duplex technology standard that can increase the speed and distance of Ethernet.

RapidIO Interconnect Specification Revision 1.1

The RapidIO interface is a communications standard used to connect devices on a circuit board and circuit boards on a backplane. RapidIO is a packet-switched interconnect standard designed for embedded systems such as those used in networking and communications. The RapidIO interface standard is a high-performance interconnect interface used for transferring data and control information between microprocessors, DSPs, system memory, communications and network processors, and peripheral devices in a system.

RapidIO replaces existing peripheral bus and processor technologies such as PCI. Some features of RapidIO include multiprocessing support, an open standard, flexible topologies, higher bandwidth, low latency, error management support in hardware, small silicon footprint, widely available process and I/O technologies, and transparency to existing applications and operating system software. The RapidIO standard provides 10-Gbps device bandwidth using 8-bit-wide input and output data ports. RapidIO uses LVDS technology, has the capability to be scaled to multi-GHz frequencies, and features a 10-bit interface.

HyperTransport Technology - HyperTransport Consortium

The HyperTransport technology I/O standard is a differential high-speed, high performance I/O interface standard developed for communications and networking chip-to-chip communications. HyperTransport technology is used in applications such as high-performance networking, telecommunications, embedded systems, consumer electronics, and Internet connectivity devices. The HyperTransport technology I/O standard is a point-to-point (one source connected to exactly one destination) standard that provides a high-performance interconnect between integrated circuits in a system, such as on a motherboard.

Stratix devices support HyperTransport technology at data rates up to 800 Mbps and 32 bits in each direction. HyperTransport technology uses an enhanced differential signaling technology to improve performance. HyperTransport technology supports data widths of 2, 4, 8, 16, or 32 bits in each direction. HyperTransport technology in Stratix and Stratix GX devices operates at multiple clock speeds up to 400 MHz.

UTOPIA Level 4 – ATM Forum Technical Committee Standard AF-PHY-0144.001

The UTOPIA Level 4 frame-based interface standard allows device manufacturers and network developers to develop components that can operate at data rates up to 10 Gbps. This standard increases interface speeds using LVDS I/O and advanced silicon technologies for fast data transfers.

UTOPIA Level 4 provides new control techniques and a 32-, 16-, or 8-bit LVDS bus, a symmetric transmit/receive bus structure for easier application design and testability, nominal data rates of 10 Gbps, in-band control of cell delimiters and flow control to minimize pin count, source-synchronous clocking, and supports variable length packet systems. UTOPIA Level 4 handles sustained data rates for OC-192 and supports ATM cells. UTOPIA Level 4 also supports interconnections across motherboards, daughtercards, and backplane interfaces.

Stratix & Stratix GX I/O Banks

Stratix devices have eight I/O banks in addition to the four enhanced PLL external clock output banks, as shown in Table 16–2 and Figure 16–18. I/O banks 3, 4, 7, and 8 support all single-ended I/O standards. I/O banks 1, 2, 5, and 6 support differential HSTL (on input clocks), LVDS, LVPECL, PCML, and HyperTransport technology, as well as all single-ended I/O standards except HSTL Class II, GTL, SSTL-18 Class II, PCI/PCI-X 1.0, and 1× /2× AGP. The four enhanced PLL external clock output banks (I/O banks 9, 10, 11, and 12) support clock outputs all

single-ended I/O standards in addition to differential SSTL-2 and HSTL (both on the output clock only). Since Stratix devices support both non-voltage-referenced and voltage-referenced I/O standards, there are different guidelines when working with either separately or when working with both.

Table 16–2. I/O Standards Supported in Stratix I/O Banks (Part 1 of 2)

I/O Standard	I/O Bank								Enhanced PLL External Clock Output Banks			
	1	2	3	4	5	6	7	8	9	10	11	12
3.3-V LVTTL/LVCMOS	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
2.5-V LVTTL/LVCMOS	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
1.8-V LVTTL/LVCMOS	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
1.5-V LVCMOS	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
PCI/PCIX//Compact PCI			✓	✓			✓	✓	✓	✓	✓	✓
AGP 1×			✓	✓			✓	✓	✓	✓	✓	✓
AGP 2×			✓	✓			✓	✓	✓	✓	✓	✓
SSTL-3 Class I	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
SSTL-3 Class II	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
SSTL-2 Class I	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
SSTL-2 Class II	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
SSTL-18 Class I	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
SSTL-18 Class II			✓	✓			✓	✓	✓	✓	✓	✓
Differential SSTL-2 (output clocks)									✓	✓	✓	✓
HSTL Class I	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
1.5-V HSTL Class I	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
1.8-V HSTL Class I	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
HSTL Class II			✓	✓			✓	✓	✓	✓	✓	✓
1.5-V HSTL Class II			✓	✓			✓	✓	✓	✓	✓	✓
1.8-V HSTL Class II			✓	✓			✓	✓	✓	✓	✓	✓
Differential HSTL (input clocks)	✓	✓	✓	✓	✓	✓	✓	✓				
Differential HSTL (output clocks)									✓	✓	✓	✓

Table 16–2. I/O Standards Supported in Stratix I/O Banks (Part 2 of 2)

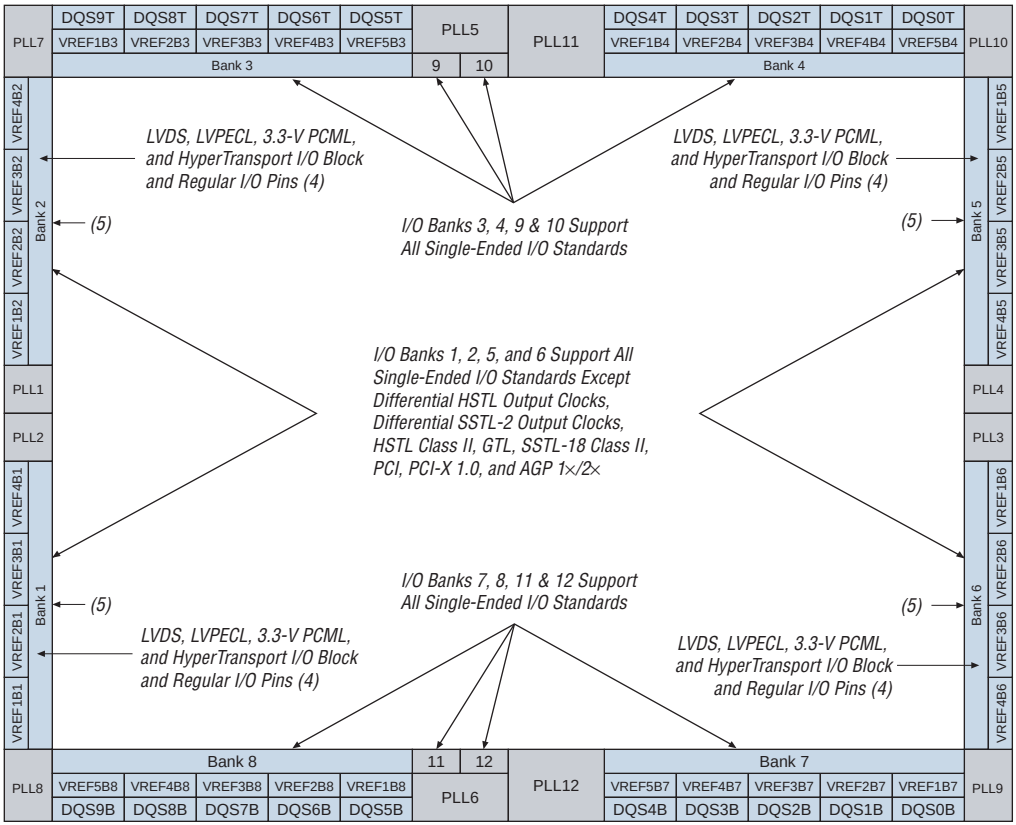
I/O Standard	I/O Bank								Enhanced PLL External Clock Output Banks			
	1	2	3	4	5	6	7	8	9	10	11	12
GTL			✓	✓			✓	✓	✓	✓	✓	✓
GTL+	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
CTT	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
LVDS	✓	✓	(1)	(1)	✓	✓	(1)	(1)	(2)	(2)	(2)	(2)
HyperTransport technology	✓	✓	(1)	(1)	✓	✓	(1)	(1)	(2)	(2)	(2)	(2)
LVPECL	✓	✓	(1)	(1)	✓	✓	(1)	(1)	(2)	(2)	(2)	(2)
PCML	✓	✓	(1)	(1)	✓	✓	(1)	(1)	(2)	(2)	(2)	(2)

Notes to Table 16–2:

(1) This I/O standard is only supported on input clocks in this I/O bank.

(2) This I/O standard is only supported on output clocks in this I/O bank.

Figure 16–18. Stratix I/O Banks *Notes (1), (2), (3)*



Notes to Figure 16–18:

(1) Figure 16–18 is a top view of the silicon die. This corresponds to a top-down view for non-flip-chip packages, but is a reverse view for flip-chip packages.

(2) Figure 16–18 is a graphic representation only. See the pin list and the Quartus II software for exact locations.

(3) Banks 9 through 12 are enhanced PLL external clock output banks.

(4) If the high-speed differential I/O pins are not used for high-speed differential signaling, they can support all of the I/O standards except HSTL Class II, GTL, SSTL-18 Class II, PCI, PCI-X 1.0, and AGP 1×/2×.

(5) For guidelines on placing single-ended I/O pads next to differential I/O pads, see "I/O Pad Placement Guidelines" on page 16–30.

Tables 16–3 and 16–4 list the I/O standards that Stratix GX enhanced and fast PLL pins support. Figure 16–19 shows the I/O standards that each Stratix GX I/O bank supports.

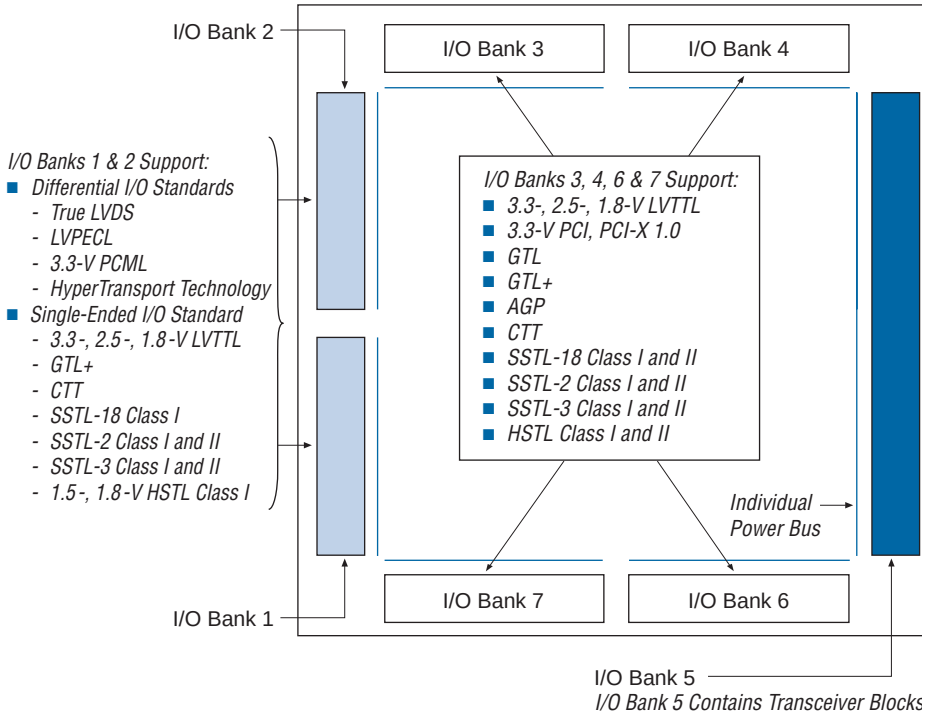
Table 16–3. I/O Standards Supported in Stratix & Stratix GX Enhanced PLL Pins

I/O Standard	Input			Output
	INCLK	FBIN	PLLENABLE	EXTCLK
LVTTL	✓	✓	✓	✓
LVCMOS	✓	✓	✓	✓
2.5 V	✓	✓		✓
1.8 V	✓	✓		✓
1.5 V	✓	✓		✓
3.3-V PCI	✓	✓		✓
3.3-V PCI-X 1.0	✓	✓		✓
LVPECL	✓	✓		✓
3.3-V PCML	✓	✓		✓
LVDS	✓	✓		✓
HyperTransport technology	✓	✓		✓
Differential HSTL	✓			✓
Differential SSTL				✓
3.3-V GTL	✓	✓		✓
3.3-V GTL+	✓	✓		✓
1.5-V HSTL Class I	✓	✓		✓
1.5-V HSTL Class II	✓	✓		✓
SSTL-18 Class I	✓	✓		✓
SSTL-18 Class II	✓	✓		✓
SSTL-2 Class I	✓	✓		✓
SSTL-2 Class II	✓	✓		✓
SSTL-3 Class I	✓	✓		✓
SSTL-3 Class II	✓	✓		✓
AGP (1× and 2×)	✓	✓		✓
CTT	✓	✓		✓

Table 16–4. I/O Standards Supported in Stratix & Stratix GX Fast PLL Pins

I/O Standard	Input	
	INCLK	PLLENABLE
LVTTL	✓	✓
LVCMOS	✓	✓
2.5 V	✓	
1.8 V	✓	
1.5 V	✓	
3.3-V PCI		
3.3-V PCI-X 1.0		
LVPECL	✓	
3.3-V PCML	✓	
LVDS	✓	
HyperTransport technology	✓	
Differential HSTL	✓	
Differential SSTL		
3.3-V GTL		
3.3-V GTL+		
1.5V HSTL Class I	✓	
1.5V HSTL Class II		
SSTL-18 Class I	✓	
SSTL-18 Class II		
SSTL-2 Class I	✓	
SSTL-2 Class II	✓	
SSTL-3 Class I	✓	
SSTL-3 Class II	✓	
AGP (1× and 2×)		
CTT	✓	

Figure 16–19. Stratix GX I/O Banks



There is some flexibility with the number of I/O standards each Stratix I/O bank can simultaneously support. The following sections provide guidelines for mixing non-voltage-referenced and voltage-referenced I/O standards in Stratix devices.

Non-Voltage-Referenced Standards

Each Stratix I/O bank has its own VCCIO pins and supports only one V_{CCIO}, either 1.5, 1.8, 2.5 or 3.3 V. A Stratix I/O bank can simultaneously support any number of input signals with different I/O standard assignments, as shown in Table 16–5.

Table 16–5. Acceptable Input Levels for LVTTL/LVCMOS

Bank V_{CCIO}	Acceptable Input Levels			
	3.3 V	2.5 V	1.8 V	1.5 V
3.3 V	✓	✓		
2.5 V	✓	✓		
1.8 V	✓ (2)	✓ (2)	✓	✓ (1)
1.5 V	✓ (2)	✓ (2)	✓	✓

Notes to Table 16–5:

(1) Because the input signal will not drive to the rail, the input buffer does not completely shut off, and the I/O current will be slightly higher than the default value.

(2) These input values overdrive the input buffer, so the pin leakage current will be slightly higher than the default value.

For output signals, a single I/O bank can only support non-voltage-referenced output signals driving at the same voltage as V_{CCIO}. A Stratix I/O bank can only have one V_{CCIO} value, so it can only drive out that one value for non-voltage referenced signals. For example, an I/O bank with a 2.5-V V_{CCIO} setting can support 2.5-V LVTTL inputs and outputs, HyperTransport technology inputs and outputs, and 3.3-V LVCMOS inputs (not output or bidirectional pins).

If the output buffer overdrives the input buffer, you must turn on the **Allow voltage overdrive for LVTTL/LVCMOS** option in the Quartus II software. To see this option, click the **Device & Pin Options** button in the **Device** page of the **Settings** dialog box (Assignments menu). Then click the **Pin Placement** tab in the **Device & Pin Options** dialog box.

Voltage-Referenced Standards

To accommodate voltage-referenced I/O standards, each Stratix I/O bank supports multiple VREF pins feeding a common VREF bus. The number of available VREF pins increases as device density increases. If these pins are not used as VREF pins, they can not be used as generic I/O pins.

An I/O bank featuring single-ended or differential standards can support voltage-referenced standards as long as all voltage-referenced standards use the same V_{REF} setting. For example, although one I/O bank can implement both SSTL-3 and SSTL-2 I/O standards, I/O pins using these standards must be in different banks since they require different V_{REF} values

For voltage-referenced inputs, the receiver compares the input voltage to the voltage reference and does not take into account the V_{CCIO} setting. Therefore, the V_{CCIO} setting is irrelevant for voltage referenced inputs.

Voltage-referenced bidirectional and output signals must be the same as the I/O bank's V_{CCIO} voltage. For example, although you can place an SSTL-2 input pin in any I/O bank with a 1.25-V V_{REF} level, you can only place SSTL-2 output pins in an I/O bank with a 2.5-V V_{CCIO}.

Mixing Voltage Referenced & Non-Voltage Referenced Standards

Non-voltage referenced and voltage referenced pins can safely be mixed in a bank by applying each of the rule-sets individually. For example, on I/O bank can support SSTL-3 inputs and 1.8-V LVCMOS inputs and outputs with a 1.8-V V_{CCIO} and a 1.5-V V_{REF}. Similarly, an I/O bank can support 1.5-V LVCMOS, 3.3-V LVTTL (inputs, but not outputs), and HSTL I/O standards with a 1.5-V V_{CCIO} and 0.75-V V_{REF}.

For the voltage-referenced examples, see the "I/O Pad Placement Guidelines" section. For details on how the Quartus II software supports I/O standards, see the "Quartus II Software Support"section.

Drive Strength

Each I/O standard supported by Stratix and Stratix GX devices drives out a minimum drive strength. When an I/O is configured as LVTTL or LVCMOS I/O standards, you can specify the current drive strength, as summarized in Table 16–7.

Standard Current Drive Strength

Each I/O standard supported by Stratix and Stratix GX devices drives out a minimum drive strength. Table 16–6 summarizes the minimum drive strength of each I/O standard.

Table 16–6. Minimum Current Drive Strength of Each I/O Standard

I/O Standard	Current Strength, I_{OL}/I_{OH} (mA)
GTL	40 *(1)*
GTL+	34 *(1)*
SSTL-3 Class I	8
SSTL-3 Class II	16
SSTL-2 Class I	8.1
SSTL-2 Class II	16.4
SSTL-18 Class I	6.7
SSTL-18 Class II	13.4
1.5-V HSTL Class I	8
1.5-V HSTL Class II	16
CTT	8
AGP 1×	I_{OL} = 1.5, I_{OH} = –0.5

Note to Table 16–6:
(1) Because this I/O standard uses an open drain buffer, this value refers to I_{OL}.

When the SSTL-2 Class I and II I/O standards are implemented on top or bottom I/O pins, the drive strength is designed to be higher than the drive strength of the buffer when implemented on side I/O pins. This allows the top or bottom I/O pins to support 200-MHz operation with the standard 35-pF load. At the same time, the current consumption when using top or bottom I/O pins is higher than the side I/O pins. The high current strength may not be necessary for certain applications where the value of the load is less than the standard test load (e.g., DDR interface). The Quartus II software allows you to reduce the drive strength when the I/O pins are used for the SSTL-2 Class I or Class II I/O standard and being implemented on the top or bottom I/O through the Current Strength setting. Select the minimum strength for lower drive strength.

Programmable Current Drive Strength

The Stratix and Stratix GX device I/O pins support various output current drive settings as shown in Table 16–7. These programmable drive strength settings help decrease the effects of simultaneously switching outputs (SSO) in conjunction with reducing system noise. The supported settings ensure that the device driver meets the I_{OH} and I_{OL} specifications for the corresponding I/O standard.

Table 16–7. Programmable Drive Strength

I/O Standard	I_{OH} / I_{OL} Current Strength Setting (mA)
3.3-V LVTTL	24 *(1)*, 16, 12, 8, 4
3.3-V LVCMOS	24 *(2)*, 12 *(1)*, 8, 4, 2
2.5-V LVTTL/LVCMOS	16 *(1)*, 12, 8, 2
1.8-V LVTTL/LVCMOS	12 *(1)*, 8, 2
1.5-V LVCMOS	8 *(1)*, 4, 2

Notes to Table 16–7:
(1) This is the Quartus II software default current setting.
(2) I/O banks 1, 2, 5, and 6 do not support this setting.

These drive-strength settings are programmable on a per-pin basis (for output and bidirectional pins only) using the Quartus II software. To modify the current strength of a particular pin, see "Programmable Drive Strength Settings" on page 16–40.

Hot Socketing

Stratix devices support hot socketing without any external components. In a hot socketing situation, a device's output buffers are turned off during system power-up or power-down. Stratix and Stratix GX devices support any power-up or power-down sequence (V_{CCIO} and V_{CCINT}) to simplify designs. For mixed-voltage environments, you can drive signals into the device before or during power-up or power-down without damaging the device. Stratix and Stratix GX devices do not drive out until the device is configured and has attained proper operating conditions.

Even though you can power up or down the V_{CCIO} and V_{CCINT} power supplies in any sequence you should not power down any I/O bank(s) that contains the configuration pins while leaving other I/O banks powered on. For power up and power down, all supplies (V_{CCINT} and all V_{CCIO} power planes) must be powered up and down within 100 ms of one another. This prevents I/O pins from driving out.

You can power up or power down the V_{CCIO} and V_{CCINT} pins in any sequence. The power supply ramp rates can range from 100 ns to 100 ms. During hot socketing, the I/O pin capacitance is less than 15 pF and the clock pin capacitance is less than 20 pF.

DC Hot Socketing Specification

The hot socketing DC specification is $| I_{IOPIN} | < 300 \mu A$.

AC Hot Socketing Specification

The hot socketing AC specification is $| I_{IOPIN} | < 8$ mA for 10 ns or less.

This specification takes into account the pin capacitance, but not board trace and external loading capacitance. Additional capacitance for trace, connector, and loading must be considered separately.

I_{IOPIN} is the current at any user I/O pin on the device. The DC specification applies when all VCC supplies to the device are stable in the powered-up or powered-down conditions. For the AC specification, the peak current duration because of power-up transients is 10 ns or less. For more information, refer to the *Hot-Socketing & Power-Sequencing Feature & Testing for Altera Devices* white paper.

I/O Termination

Although single-ended, non-voltage-referenced I/O standards do not require termination, Altera recommends using external termination to improve signal integrity where required.

The following I/O standards do not require termination:

- LVTTL
- LVCMOS
- 2.5 V
- 1.8 V
- 1.5 V
- 3.3-V PCI/Compact PCI
- 3.3-V PCI-X 1.0
- 3.3-V AGP 1×

Voltage-Referenced I/O Standards

Voltage-referenced I/O standards require both an input reference voltage, $V_{REF,}$ and a termination voltage, V_{TT}. Off-chip termination on the board should be used for series and parallel termination.

For more information on termination for voltage-referenced I/O standards, see the *Selectable I/O Standards in Stratix & Stratix GX Devices* chapter in the *Stratix Device Handbook, Volume 2*; or the *Stratix GX Device Handbook, Volume 2*.

Differential I/O Standards

Differential I/O standards typically require a termination resistor between the two signals at the receiver. The termination resistor must match the differential load impedance of the bus. Stratix and Stratix GX devices provide an optional differential termination on-chip resistor when using LVDS.

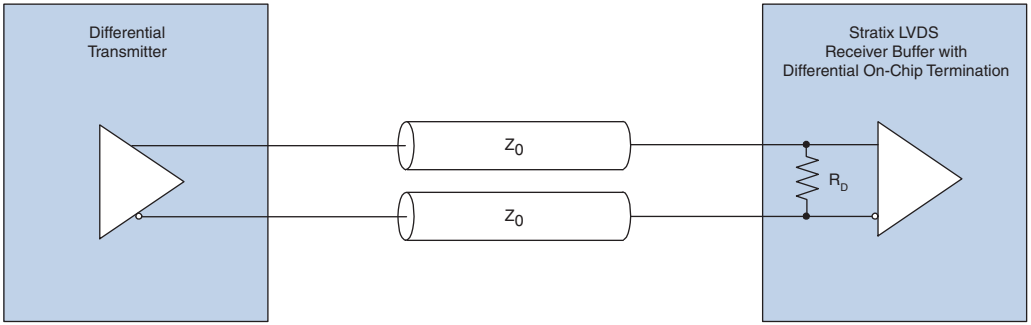
See the *High-Speed Differential I/O Interfaces in Stratix Devices* chapter for more information on differential I/O standards and their interfaces.

For differential I/O standards, I/O banks support differential termination when V_{CCIO} equals 3.3 V.

Differential Termination (R_D)

Stratix devices support differential on-chip termination for source-synchronous LVDS signaling. The differential termination resistors are adjacent to the differential input buffers on the device. This placement eliminates stub effects, improving the signal integrity of the serial link. Using differential on-chip termination resistors also saves board space. Figure 16–20 shows the differential termination connections for Stratix and Stratix GX devices.

Figure 16–20. Differential Termination



Differential termination for Stratix devices is supported for the left and right I/O banks. Differential termination for Stratix GX devices is supported for the left, source-synchronous I/O bank. Some of the clock input pins are in the top and bottom I/O banks, which do not support differential termination. Clock pins CLK[1,3,8,10] support differential on-chip termination. Clock pins CLK[0,2,9,11], CLK[4-7], and CLK[12-15] do not support differential on-chip termination.

Transceiver Termination

Stratix GX devices feature built-in on-chip termination within the transceiver at both the transmit and receive buffers. This termination improves signal integrity and provides support for the 1.5-V PCML I/O standard.

I/O Pad Placement Guidelines

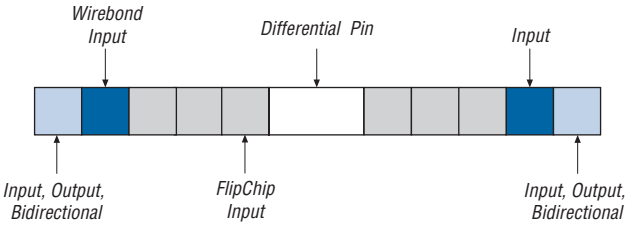
This section provides pad placement guidelines for the programmable I/O standards supported by Stratix and Stratix GX devices and includes essential information for designing systems using the devices' selectable I/O capabilities. These guidelines will reduce noise problems so that FPGA devices can maintain an acceptable noise level on the line from the V_{CCIO} supply. Since Altera FPGAs require that a separate V_{CCIO} power each bank, these noise issues do not have any effect when crossing bank boundaries and these guidelines do not apply. Although pad placement rules need not be considered between I/O banks, some rules must be considered if you are using a `VREF` signal in a `PLLOUT` bank. Note that the signals in the `PLLOUT` banks share the V_{REF} supply with neighboring I/O banks and, therefore, must adhere to the V_{REF} rules discussed in "VREF Pad Placement Guidelines".

Differential Pad Placement Guidelines

To avoid cross coupling and maintain an acceptable noise level on the V_{CCIO} supply, there are restrictions on the placement of single-ended I/O pads in relation to differential pads. Use the following guidelines for placing single-ended pads with respect to differential pads in Stratix devices. These guidelines apply for LVDS, HyperTransport technology, LVPECL, and PCML I/O standards. The differential pad placement guidelines do not apply for differential HSTL and differential SSTL output clocks since each differential output clock is essentially implemented using two single-ended output buffers. These rules do not apply to differential HSTL input clocks either even though the dedicated input buffers are used. However, both differential HSTL and differential SSTL output standards must adhere to the single-ended (`VREF`) pad placement restrictions discussed in "VREF Pad Placement Guidelines".

- For flip-chip packages, there are no restrictions for placement of single-ended input signals with respect to differential signals (see Figure 16–21). For wire-bond packages, single ended input pads may only be placed four or more pads away from a differential pad.
- Single-ended outputs and bidirectional pads may only be placed five or more pads away from a differential pad (see Figure 16–21), regardless of package type.

Figure 16–21. Legal Pin Placement *Note (1)*



Note to Figure 16–21:
(1) Input pads on a flip-chip packages have no restrictions.

VREF Pad Placement Guidelines

Restrictions on the placement of single-ended voltage-referenced I/O pads with respect to VREF pads help maintain an acceptable noise level on the V_{CCIO} supply and to prevent output switching noise from shifting the VREF rail. The following guidelines are for placing single-ended pads in Stratix devices.

Input Pins

Each VREF pad supports a maximum of 40 input pads with up to 20 on each side of the VREF pad.

Output Pins

When a voltage referenced input or bidirectional pad does not exist in a bank, there is no limit to the number of output pads that can be implemented in that bank. When a voltage referenced input exists, each VREF pad supports 20 outputs for thermally enhanced FineLine BGA® and thermally enhanced BGA cavity up packages or 15 outputs for Non-thermally enhanced cavity up and non-thermally enhanced FineLine BGA packages.

Bidirectional Pins

Bidirectional pads must satisfy input and output guidelines simultaneously. If the bidirectional pads are all controlled by the same OE and there are no other outputs or voltage referenced inputs in the bank, then there is no case where there is a voltage referenced input active at the same time as an output. Therefore, the output limitation does not apply. However, since the bidirectional pads are linked to the same OE, the bidirectional pads act as inputs at the same time. Therefore, the input limitation of 40 input pads (20 on each side of the VREF pad) applies.

If any of the bidirectional pads are controlled by different output enables (OE) and there are no other outputs or voltage referenced inputs in the bank, then there may be a case where one group of bidirectional pads is acting as inputs while another group is acting as outputs. In such cases, apply the formulas shown in Table 16–8.

Table 16–8. Input-Only Bidirectional Pin Limitation Formulas

Package Type	Formula
Thermally enhanced FineLine BGA and thermally enhanced BGA cavity up	<*Total number of bidirectional pads*> – <*Total number of pads from the smallest group of pads controlled by an OE*> ≤20 (per VREF pad)
Non-thermally enhanced cavity up and non-thermally enhanced FineLine BGA	<*Total number of bidirectional pads*> – <*Total number of pads from the smallest group of pads controlled by an OE*> ≤15 (per VREF pad).

Consider a thermally enhanced FineLine BGA package with eight bidirectional pads controlled by OE1, eight bidirectional pads controlled by OE2, and six bidirectional pads controlled by OE3. While this totals 22 bidirectional pads, it is safely allowable because there would be a maximum of 16 outputs per VREF pad possible assuming the worst case where OE1 and OE2 are active and OE3 is inactive. This is particularly relevant in DDR SDRAM applications.

When at least one additional voltage referenced input and no other outputs exist in the same VREF bank, then the bidirectional pad limitation must simultaneously adhere to the input and output limitations. See the following equation.

<*Total number of bidirectional pads*> + <*Total number of input pads*> ≤40 (20 on each side of the VREF pad)

The previous equation accounts for the input limitations, but you must apply the appropriate equation from Table 16–9 to determine the output limitations.

Table 16–9. Bidirectional pad Limitation Formulas (Where VREF Inputs Exist)

Package Type	Formula
Thermally enhanced FineLine BGA and thermally enhanced BGA cavity up	<*Total number of bidirectional pads*> ≤20 (per VREF pad)
Non-thermally enhanced cavity up and non-thermally enhanced FineLine BGA	<*Total number of bidirectional pads*> ≤15 (per VREF pad)

When at least one additional output exists but no voltage referenced inputs exist, apply the appropriate formula from Table 16–10.

Table 16–10. Bidirectional Pad Limitation Formulas (Where VREF Outputs Exist)

Package Type	Formula
Thermally enhanced FineLine BGA and thermally enhanced BGA cavity up	<*Total number of bidirectional pads*> + <*Total number of additional output pads*> – <*Total number of pads from the smallest group of pads controlled by an OE*> ≤20 (per VREF pad)
Non-thermally enhanced cavity up and non-thermally enhanced FineLine BGA	<*Total number of bidirectional pads*> + <*Total number of additional output pads*> – <*Total number of pads from the smallest group of pads controlled by an OE*> ≤15 (per VREF pad)

When additional voltage referenced inputs and other outputs exist in the same VREF bank, then the bidirectional pad limitation must again simultaneously adhere to the input and output limitations. See the following equation.

<*Total number of bidirectional pads*> + <*Total number of input pads*> ≤40 (20 on each side of the VREF pad)

The previous equation accounts for the input limitations, but you must apply the appropriate equation from Table 16–9 to determine the output limitations.

Table 16–11. Bidirectional Pad Limitation Formulas (Multiple VREF Inputs & Outputs)

Package Type	Formula
Thermally enhanced FineLine BGA and thermally enhanced BGA cavity up	<*Total number of bidirectional pads*> + <*Total number of additional output pads*> ≤20 (per VREF pad)
non-thermally enhanced cavity up and non-thermally enhanced FineLine BGA	<*Total number of bidirectional pads*> + <*Total number of additional output pads*> ≤15 (per VREF pad)

In addition to the pad placement guidelines, use the following guidelines when working with V_{REF} standards:

- Each bank can only have a single V_{CCIO} voltage level and a single V_{REF} voltage level at a given time. Pins of different I/O standards can share the bank if they have compatible V_{CCIO} values (see Table 16–12 for more details).
- In all cases listed above, the Quartus II software generates an error message for illegally placed pads.

Output Enable Group Logic Option in Quartus II

The Quartus II software can check a design to make sure that the pad placement does not violate the rules mentioned above. When the software checks the design, if the design contains more bidirectional pins than what is allowed, the Quartus II software returns a fitting error. When all the bidirectional pins are either input or output but not both (for example, in a DDR memory interface), you can use the **Output Enable Group Logic** option. Turning on this option directs the Quartus II Fitter to view the specified nodes as an output enable group. This way, the Fitter does not violate the requirements for the maximum number of pins driving out of a V_{REF} bank when a voltaged-referenced input pin or bidirectional pin is present.

In a design that implements DDR memory interface with dq, dqs and dm pins utilized, there are two ways to enable the above logic options. You can enable the logic options through the Assignment Editor or by adding the following assignments to your project's ESF file:

```
OPTIONS_FOR_INDIVIDUAL_NODES_ONLY
{
    dq  : OUTPUT_ENABLE_GROUP 1;
    dqs : OUTPUT_ENABLE_GROUP 1;
```

```
    dm  : OUTPUT_ENABLE_GROUP 1;
}
```

As a result, the Quartus II Fitter does not count the bidirectional pin potential outputs, and the number of V_{REF} bank outputs remains in the legal range.

Toggle Rate Logic Option in Quartus II

You should specify the pin's output toggling rate in order to perform a stricter pad placement check in the Quartus II software. Specify the frequency at which a pin toggles in the Quartus II Assignment Editor. This option is useful for adjusting the pin toggle rate in order to place them closer to differential pins. The option directs the Quartus II Fitter toggle-rate checking while allowing you to place a single-ended pin closer to a differential pin.

DC Guidelines

Variables affecting the DC current draw include package type and desired termination methods. This section provides information on each of these variables and also shows how to calculate the DC current for pin placement.

The Quartus II software automatically takes these variables into account during compilation.

For any 10 consecutive output pads in an I/O bank, Altera recommends a maximum current of 200 mA for thermally enhanced FineLine BGA and thermally enhanced BGA cavity up packages and 164 mA for non-thermally enhanced cavity up and non-thermally enhanced FineLine BGA packages. The following equation shows the current density limitation equation for thermally enhanced FineLine BGA and thermally enhanced BGA cavity up packages:

$$\sum_{pin}^{pin+9} I_{pin} < 200\ mA$$

The following equation shows the current density limitation equation for non-thermally enhanced cavity up and non-thermally enhanced FineLine BGA packages:

$$\sum_{pin}^{pin+9} I_{pin} < 164\ mA$$

Table 16–12 shows the DC current specification per pin for each I/O standard. I/O standards not shown in the table do not exceed these current limitations.

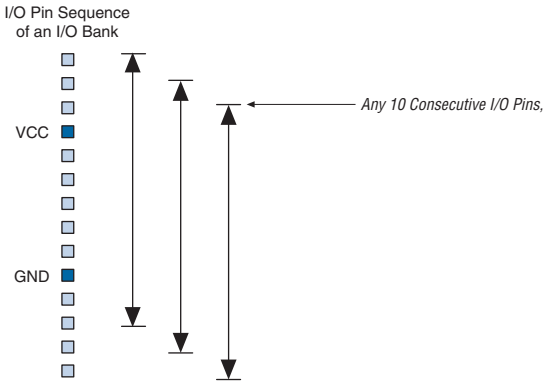
Table 16–12. I/O Standard DC Specification *Note (1)*

Pin I/O Standard	I_{PIN} (mA)		
	3.3-V V_{CCIO}	2.5-V V_{CCIO}	1.5-V V_{CCIO}
GTL	40	40	-
GTL+	34	34	-
SSTL-3 Class I	8	-	-
SSTL-3 Class II	16	-	-
CTT	8	-	-
SSTL-2 Class I	-	8.1	-
SSTL-2 Class II	-	16.4	-
HSTL Class I	-	-	8
HSTL Class II	-	-	16

Note to Table 16–12:
(1) The current rating on a V_{REF} pin is less than 10µA.

For more information on Altera device packaging, see the *Package Information for Stratix Devices* chapter in the *Stratix Device Handbook, Volume 2*.

Figure 16–22. Current Draw Limitation Guidelines



Any 10 consecutive I/O pads cannot exceed 200 mA in thermally enhanced FineLine BGA and thermally enhanced BGA cavity up packages or 164 mA in non-thermally enhanced cavity up and non-thermally enhanced FineLine BGA packages.

For example, consider a case where a group of 10 consecutive pads are configured as follows for a thermally enhanced FineLine BGA and thermally enhanced BGA cavity up package:

- Number of SSTL-3 Class I output pads = 3
- Number of GTL+ output pads = 4
- The rest of the surrounding I/O pads in the consecutive group of 10 are unused

In this case, the total current draw for these 10 consecutive I/O pads would be:

(# of SSTL-3 Class I pads × 8 mA) +
(# of GTL+ output pads × 34 mA) = (3 × 8 mA) + (4 × 34 mA) = 160 mA

In the above example, the total current draw for all 10 consecutive I/O pads is less than 200 mA.

Power Source of Various I/O Standards

For Stratix and Stratix GX devices, the I/O standards are powered by different power sources. To determine which source powers the input buffers, see Table 16–13. All output buffers are powered by V_{CCIO}.

Table 16–13. The Relationships Between Various I/O Standards and the Power Sources

I/O Standard	Power Source
2.5V/3.3V LVTTL	V_{CCIO}
PCI/PCI-X 1.0	V_{CCIO}
AGP	V_{CCIO}
1.5V/1.8V	V_{CCIO}
GTL	V_{CCINT}
GTL+	V_{CCINT}
SSTL	V_{CCINT}
HSTL	V_{CCINT}
CTT	V_{CCINT}
LVDS	V_{CCINT}
LVPECL	V_{CCINT}
PCML	V_{CCINT}
HyperTransport	V_{CCINT}

Quartus II Software Support

You specify which programmable I/O standards to use for Stratix and Stratix GX devices with the Quartus II software. This section describes Quartus II implementation, placement, and assignment guidelines, including

- Compiler Settings
- Device & Pin Options
- Assign Pins
- Programmable Drive Strength Settings
- I/O Banks in the Floorplan View
- Auto Placement & Verification

Compiler Settings

You make Compiler settings in the **Compiler Settings** dialog box (Processing menu). Click the **Chips & Devices** tab to specify the device family, specific device, package, pin count, and speed grade to use for your design.

Device & Pin Options

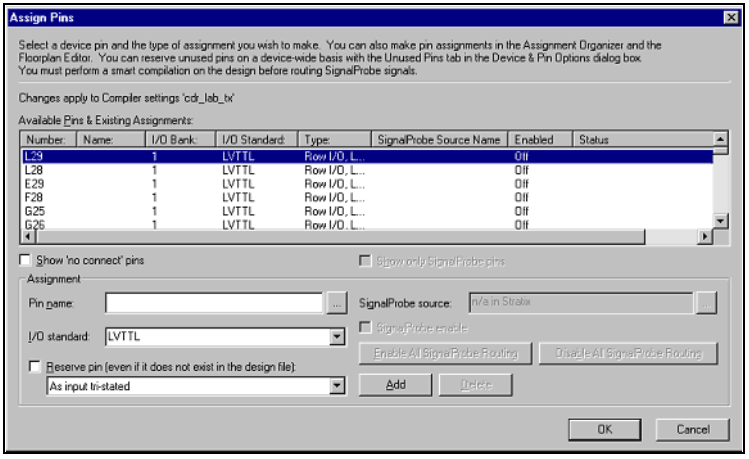
Click **Device & Pin Options** in the **Compiler Settings** dialog box to access the I/O pin settings. For example, in the **Voltage** tab you can select a default I/O standard for all pins for the targeted device. I/O pins that do not have a specific I/O standard assignment default this standard. Click **OK** when you are done setting I/O pin options to return to the **Compiler Settings** dialog box.

Assign Pins

Click **Assign Pins** in the **Compiler Settings** dialog box to view the device's pin settings and pin assignments (see Figure 16–23). You can view the pin settings under **Available Pins & Existing Assignments**. The listing does not include V_{REF} pins because they are dedicated pins. The information for each pin includes:

- Number
- Name
- I/O Bank
- I/O Standard
- Type (e.g., row or column I/O and differential or control)
- SignalProbe Source Name
- Enabled (that is, whether SignalProbe routing is enabled or disabled
- Status

Figure 16–23. Assign Pins



When you assign an I/O standard that requires a reference voltage to an I/O pin, the Quartus II software automatically assigns V_{REF} pins. See the Quartus II Help for instructions on how to use an I/O standard for a pin.

Programmable Drive Strength Settings

To make programmable drive strength settings, perform the following steps:

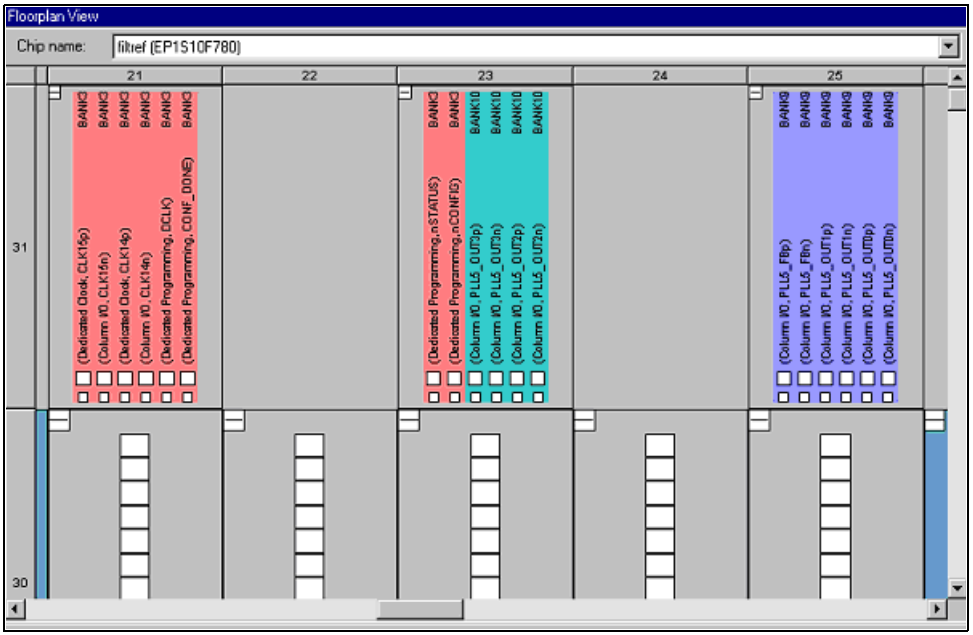
1. In the Tools menu, choose **Assignment Organizer**.
2. Choose the **Edit specific entity & node settings for:** setting, then select the output or bidirectional pin to specify the current strength for.
3. In the **Assignment Categories** dialog box, select **Options for Individual Nodes Only**.
4. Select **Click here to add a new assignment**.
5. In the **Assignment** dialog box, set the **Name** field to **Current Strength** and set the **Setting** field to the desired, allowable value.
6. Click **Add**.
7. Click **Apply**, then **OK**.

I/O Banks in the Floorplan View

You can view the arrangement of the device I/O banks in the **Floorplan View** (View menu) as shown in Figure 16–24. You can assign multiple I/O standards to the I/O pins in any given I/O bank as long as the V_{CCIO} of the standards is the same. Pins that belong to the same I/O bank must use the same V_{CCIO} signal.

Each device I/O pin belongs to a specific, numbered I/O bank. The Quartus II software color codes the I/O bank to which each I/O pin and V_{CCIO} pin belong. Turn on the **Show I/O Banks** option to display the I/O bank color and the bank numbers for each pin.

Figure 16–24. Floorplan View Window



Auto Placement & Verification of Selectable I/O Standards

The Quartus II software automatically verifies the placement for all I/O and V_{REF} pins and performs the following actions.

- Automatically places I/O pins of different V_{REF} standards without pin assignments in separate I/O banks and enables the V_{REF} pins of these I/O banks.
- Verifies that voltage-referenced I/O pins requiring different V_{REF} levels are not placed in the same bank.
- Reports an error message if the current limit is exceeded for a Stratix or Stratix GX power bank, as determined by the equation documented in "DC Guidelines" on page 16–35.
- Reserves the unused high-speed differential I/O channels and regular user I/O pins in the high-speed differential I/O banks when any of the high-speed differential I/O channels are being used.
- Automatically assigns V_{REF} pins and I/O pins such that the current requirements are met and I/O standards are placed properly.

Conclusion

Stratix and Stratix GX devices provide the I/O capabilities to allow you to work with current and emerging I/O standards and requirements. Today's complex designs demand increased flexibility to work with the wide variety of available I/O standards and to simplify board design. With Stratix and Stratix GX device features, such as hot socketing and differential on-chip termination, you can reduce board design interface costs and increase your development flexibility.

More Information

For more information, see the following sources:

- The *Stratix Device Family Data Sheet* section in the *Stratix Device Handbook, Volume 1*
- The *Stratix GX Device Family Data Sheet* section of the *Stratix GX Device Handbook, Volume 1*
- The *High-Speed Differential I/O Interfaces in Stratix Devices* chapter
- *AN 224: High-Speed Board Layout Guidelines*

References

For more information, see the following references:

- Stub Series Terminated Logic for 2.5-V (SSTL-2), JESD8-9B, Electronic Industries Association, December 2000.
- High-Speed Transceiver Logic (HSTL) – A 1.5-V Output Buffer Supply Voltage Based Interface Standard for Digital Integrated Circuits, EIA/JESD8-6, Electronic Industries Association, August 1995.
- 1.5-V +/- 0.1 V (Normal Range) and 0.9 V – 1.6 V (Wide Range) Power Supply Voltage and Interface Standard for Non-terminated Digital Integrated Circuits, JESD8-11, Electronic Industries Association, October 2000.
- 1.8-V +/- 0.15 V (Normal Range) and 1.2 V – 1.95 V (Wide Range) Power Supply Voltage and Interface Standard for Non-terminated Digital Integrated Circuits, JESD8-7, Electronic Industries Association, February 1997.
- Center-Tap-Terminated (CTT) Low-Level, High-Speed Interface Standard for Digital Integrated Circuits, JESD8-9A, Electronic Industries Association, November 1993.
- 2.5-V +/- 0.2V (Normal Range) and 1.8-V to 2.7V (Wide Range) Power Supply Voltage and Interface Standard for Non-terminated Digital Integrated Circuits, JESD8-5, Electronic Industries Association, October 1995.
- Interface Standard for Nominal 3V/ 3.3-V Supply Digital Integrated Circuits, JESD8-B, Electronic Industries Association, September 1999.
- Gunning Transceiver Logic (GTL) Low-Level, High-Speed Interface Standard for Digital Integrated Circuits, JESD8-3, Electronic Industries Association, November 1993.

- Accelerated Graphics Port Interface Specification 2.0, Intel Corporation.
- Stub Series Terminated Logic for 1.8-V (SSTL-18), Preliminary JC42.3, Electronic Industries Association.
- PCI Local Bus Specification, Revision 2.2, PCI Special Interest Group, December 1998.
- PCI-X Local Bus Specification, Revision 1.0a, PCI Special Interest Group.
- UTOPIA Level 4, AF-PHY-0144.001, ATM Technical Committee.
- POS-PHY Level 4: SPI-4, OIF-SPI4-02.0, Optical Internetworking Forum.
- POS-PHY Level 4: SFI-4, OIF-SFI4-01.0, Optical Internetworking Forum.
- Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits, ANSI/TIA/EIA-644, American National Standards Institute/Telecommunications Industry/Electronic Industries Association, October 1995.

17. High-Speed Source-Synchronous Differential I/O Interfaces in Stratix GX Devices

SGX52013-1.2

Introduction

Expansion in the telecommunications market and growth in Internet use requires systems to move more data faster than ever. To meet this demand, system designers rely on solutions such as differential signaling and emerging high-speed interface standards including RapidIO, POS-PHY 4, SFI-4, or XSBI.

These new protocols support differential data rates up to 1 gigabit per second (Gbps) and higher. At these high data rates, it becomes more challenging to manage the skew between the clock and data signals. One solution to this challenge is to use clock data recovery (CDR) to eliminate skew between data channels and clock signals. Another potential solution, dynamic phase alignment (DPA), is beginning to be incorporated by some of these protocols.

The Stratix® GX family of devices are the first FPGA devices to have an embedded dynamic phase aligner. This application note explains how to take advantage of the DPA feature in device high-speed I/O circuitry to increase system efficiencies and bandwidth. It will describe the skew issue in high-speed systems and provide a brief description of the source-synchronous circuitry in Stratix GX devices. The document will then describe an overview of the DPA block, I/O support with DPA, fast PLL support with DPA, a full description of DPA operation, and finally a comparison between CDR and source-synchronous interfaces.

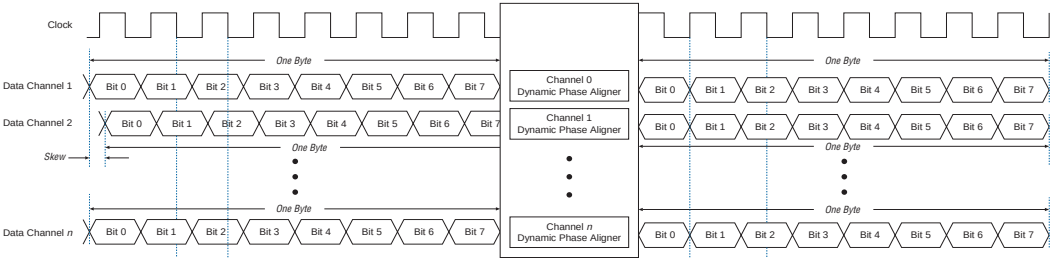
The source-synchronous high-speed interface in Stratix GX devices is a dedicated circuit embedded into the programmable logic device (PLD) allowing for high-speed communications. *AN 202: Using High-Speed Differential I/O Standards in Stratix Devices* provides information on Stratix GX device high-speed I/O standard features and functions.

Skew & Dynamic Phase Alignment

A typical problem designers face with high-speed source-synchronous systems is when clock or data signal transitions occur at different times with respect to each other (see Figure 17–1). When this happens, the receiver does not sample the data at the correct time, causing system errors. This problem is due to the inherent skew of the transmitter device, varying trace lengths and capacitive loading, variations in threshold voltages, transmission-line mis-terminations, or system reconfigurations. This results in inaccurate data transmission from one point to another and interrupted communication between components within the system.

A dynamic clock-data synchronization or phase alignment solution is optimal for high-speed systems because it provides a better tolerance to signal noise without the higher power consumption of devices which correct for skew using an individual analog PLL for each receiver channel. The dynamic phase aligner in Stratix GX devices shares the same components across many receiver channels, therefore reducing power consumption.

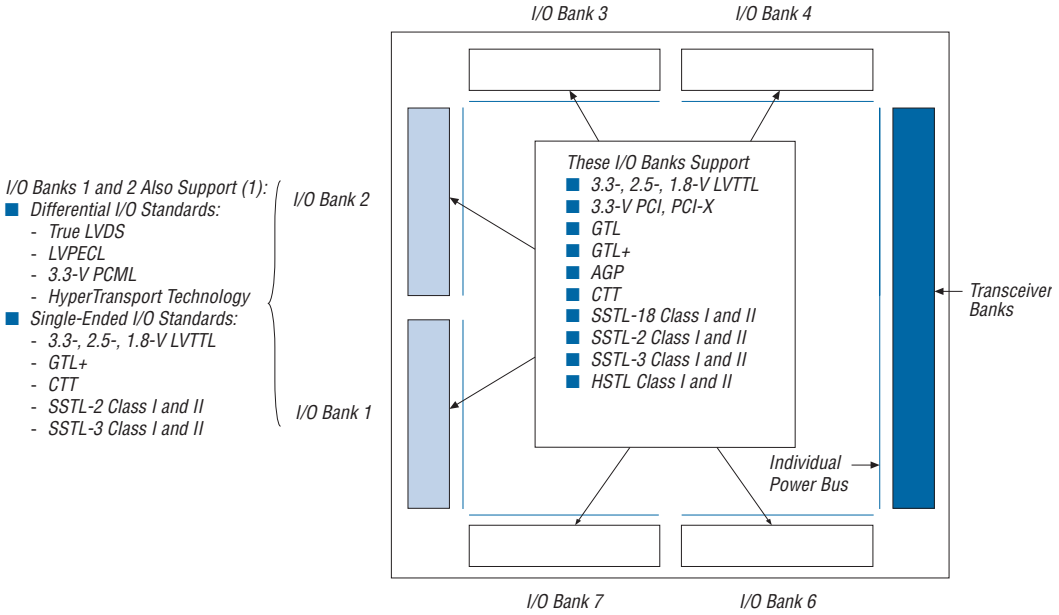
Figure 17–1. Clock to Data Skew



Stratix GX I/O Banks

Stratix GX devices contain seven I/O banks, as shown in Figure 17–2. I/O banks one and two support high-speed LVDS, LVPECL, 3.3-V PCML, HSTL class I and II, and SSTL-2 class I and II inputs and outputs. These two banks also incorporate an embedded dynamic phase aligner within the source-synchronous interface (see Figure 17–2). The dynamic phase aligner corrects for the phase difference between the clock and data lines caused by skew. The dynamic phase aligner operates automatically and continuously without requiring a fixed training pattern, and allows the source-synchronous circuitry to capture data correctly regardless of the channel-to-clock skew.

Figure 17–2. DPA Support in Stratix GX Devices



Note to Figure 17–2:
(1) You can only use the differential receiver and clock input pins as inputs for single-ended standards.

Dedicated Source-Synchronous Circuitry

The differential I/O channels in Stratix GX I/O banks 1 and 2 can interface with LVDS, LVPECL, or 3.3-V PCML I/O standards in source-synchronous mode. Stratix GX devices transmit or receive serial channels along with clocks. The receiving Stratix GX device can multiply the low-speed clock by a factor of 1, 2, 4, 8, or 10 for serializer/deserializer (SERDES) operation. The SERDES factor (*J*) can be 4, 8, or 10 (only 8 or 10 with DPA) and determines the width of the bus driving into the logic array. The SERDES factor (*J*) does not have to equal the clock-multiplication value (*W*). The Stratix GX device can bypass the dedicated SERDES for a serialization or deserialization factor of 1 or 2. If the serialization/deserialization factor is 2, the I/O element (IOE) uses the

double data rate (DDR) input and output. Table 17–1 shows the clock multiplication factors and the SERDES factors supported by Stratix GX devices.

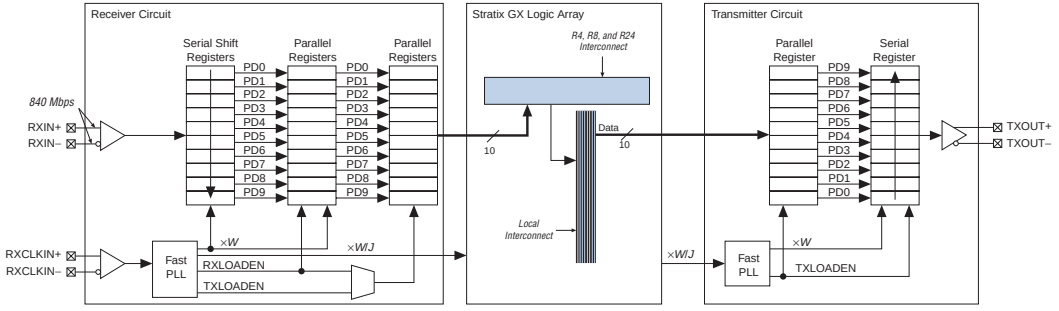
Table 17–1. Clock Multiplication Factors

Factor	Integer
Clock Multiplication *W*	1, 2, 4, 8, or 10
SERDES *J*	4, 8, or 10 *(1)*

Note to Table 17–1:
(1) The SERDES factor *J* can only be 8 or 10 when using DPA.

In the receiver circuitry, the fast PLL generates the high-frequency clock to deserialize the serial data through a shift register. The parallel data is synchronized with the low-frequency clock, and the receiver sends both to the logic array. On the transmitter side, the parallel data from the logic array is first fed into a parallel-in, serial-out shift register synchronized with the low-frequency clock and then transmitted out by the output buffers. Figure 17–3 shows the dedicated receiver and transmitter interface. For more information on the Stratix GX source-synchronous operation, refer to *AN 202: Using High-Speed Differential I/O Interfaces in Stratix Devices*.

Figure 17–3. Source-Synchronous Differential I/O Receiver/Transmitter Interface



The enable signal RXLOADEN loads the parallel data into the next parallel register on the second rising edge of the low-frequency clock in both modes (with or without DPA). Figure 17–4 shows the clock and data relationship in the receiver.

Figure 17–4. Receiver Timing Diagram

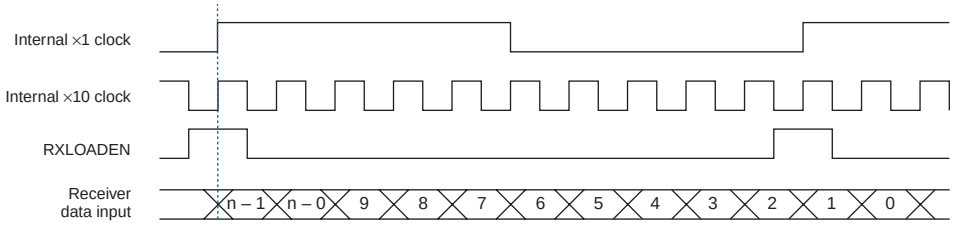
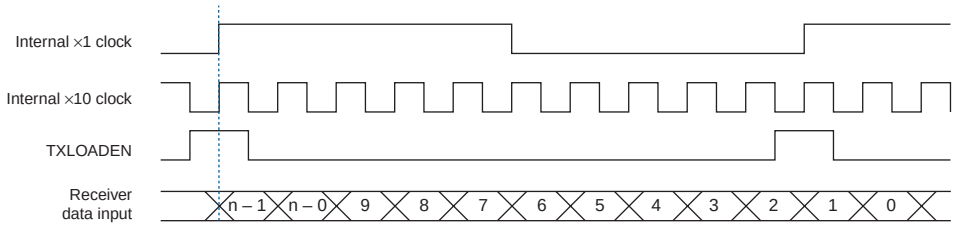


Figure 17–5 shows the timing relationship between the data and clock in the Stratix GX transmitter in ×10 mode.

Figure 17–5. Transmitter Timing Diagram

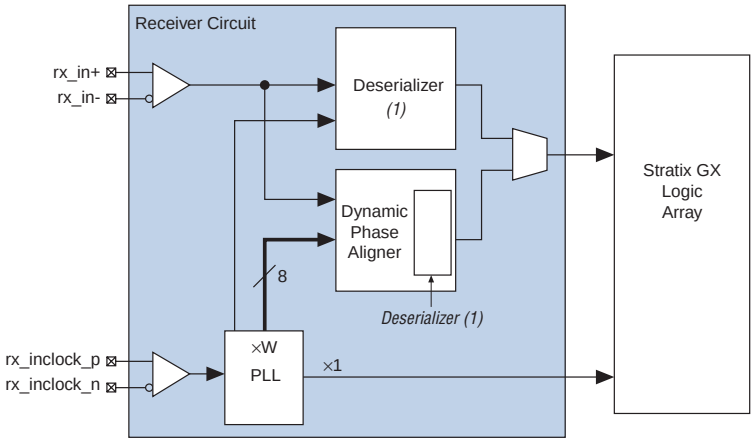


DPA Block Overview

Each Stratix GX receiver channel features a DPA block. The block contains a dynamic phase selector for phase detection and selection, a SERDES, a synchronizer, and a data realigner circuit. You can bypass the dynamic phase aligner without affecting the basic source-synchronous operation of the channel by using a separate deserializer shown in Figure 17–6.

The dynamic phase aligner uses both the source clock and the serial data. The dynamic phase aligner automatically and continuously tracks fluctuations caused by system variations and self-adjusts to eliminate the phase skew between the multiplied clock and the serial data. Figure 17–6 shows the relationship between Stratix GX source-synchronous circuitry and the Stratix GX source-synchronous circuitry with DPA.

Figure 17–6. Source-Synchronous DPA Circuitry



Unlike the de-skew function in APEX™ 20KE and APEX 20KC devices or the clock-data synchronization (CDS) circuit in APEX II devices, you do not have to use a fixed training pattern with DPA in Stratix GX devices or assert a pin to activate the circuit.

DPA Input Support

Stratix GX device I/O banks 1 and 2 contain dedicated circuitry to support differential I/O standards at speeds up to 1 Gbps with DPA (or up to 840 Mbps without DPA). Stratix GX device source-synchronous circuitry supports LVDS, LVPECL, and 3.3-V PCML I/O standards. Additionally, the clock input pins in I/O banks 1 and 2 support differential HSTL. Table 17–2 shows the I/O standards that the dynamic phase aligner supports and their corresponding supply voltage. All Stratix GX device differential receiver input pins and clock pins in I/O banks 1 and 2 are dedicated input pins. Transmitter pins can be either input or output pins for both differential and single-ended I/O standards. Refer to Table 17–3.

Table 17–2. DPA Differential I/O Standards

I/O Standard	V_{CC} I/O (V)
LVDS, LVPECL, 3.3-V PCML	3.3

Table 17–3. Bank 1 & 2 Input Pins

Input Pin Type	I/O Standard	Receiver Pin	Transmitter Pin
Differential	Differential	Input only	Output only
Single ended	Single ended	Input only	Input or output

Interface & Fast PLL

This section describes the number of channels that support DPA and their relationship with the PLL in Stratix GX devices. EP1SGX10 and EP1SGX25 devices have two dedicated fast PLLs and EP1SGX40 devices have four dedicated fast PLLs for clock multiplication. Table 17–4 shows the maximum number of channels in each Stratix GX device that support DPA.

Table 17–4. Stratix GX Source-Synchronous Differential I/O Resources

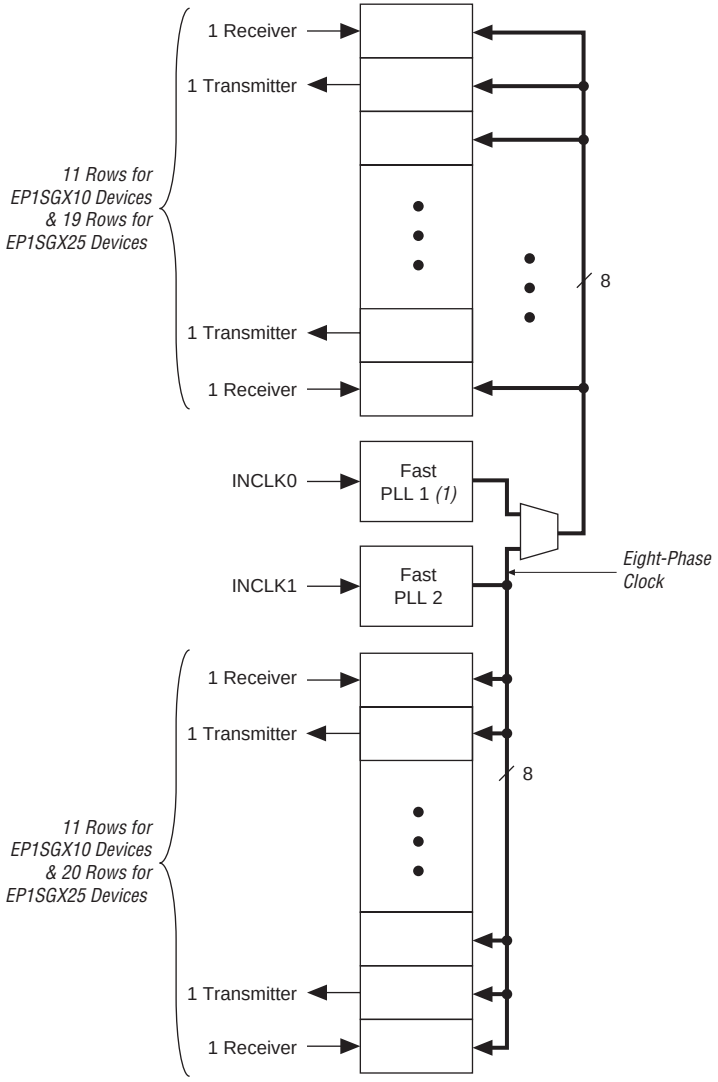
Device	Fast PLLs	Pin Count	Receiver Channels *(1)*	Transmitter Channels *(1)*	Receiver & Transmitter Channel Speed (Gbps) *(2)*	LEs
EP1SGX10C	2 *(3)*	672	22	22	1	10,570
EP1SGX10D	2 *(3)*	672	22	22	1	10,570
EP1SGX25C	2	672	39	39	1	25,660
EP1SGX25D	2	672	39	39	1	25,660
		1,020	39	39	1	25,660
EP1SGX25F	2	1,020	39	39	1	25,660
EP1SGX40D	4 *(4)*	1,020	45	45	1	41,250
EP1SGX40G	4 *(4)*	1,020	45	45	1	41,250

Notes to Table 17–4:

(1) This is the number of receiver or transmitter channels in the source-synchronous (I/O bank 1 and 2) interface of the device.
(2) Receiver channels operate at 1,000 Mbps with DPA. Without DPA, the receiver channels operate at 840 Mbps.
(3) One of the two fast PLLs in EP1SGX10C and EP1SGX10D devices supports DPA.
(4) Two of the four fast PLLs in EP1SGX40D and EP1SGX40G devices support DPA

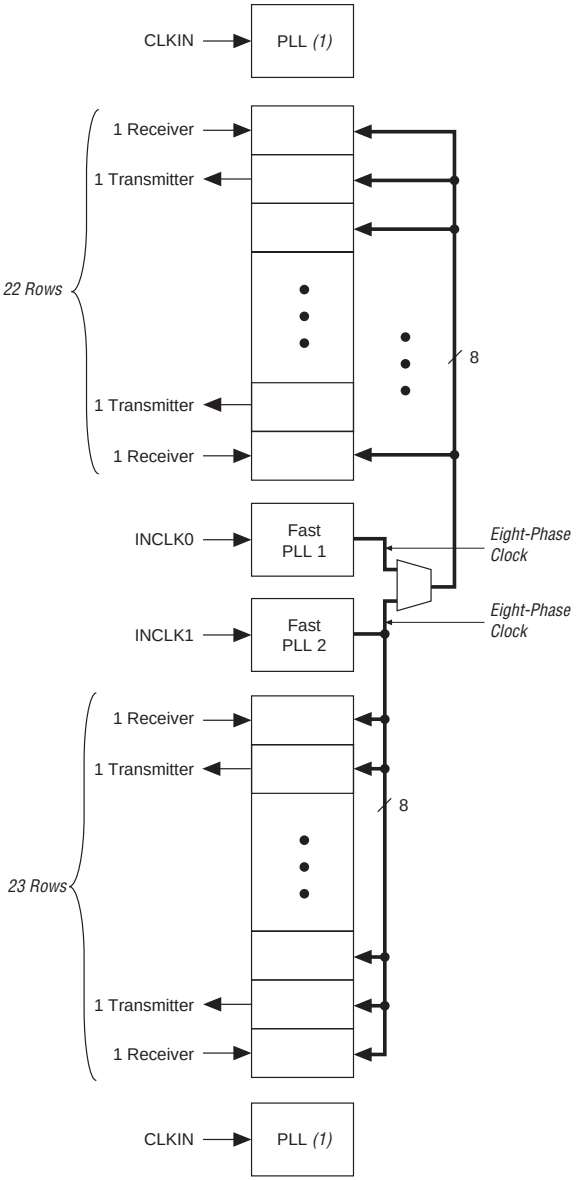
The receiver and transmitter channels are interleaved so that each I/O row in I/O banks 1 and 2 of the device has one receiver channel and one transmitter channel per row. Figures 17–7 and 17–8 show the fast PLL and channels with DPA layout in EP1SGX10, EP1SGX25, and EP1SGX40 devices. In EP1SGX10 devices, only fast PLL 2 supports DPA operations.

Figure 17–7. PLL & Channel Layout in EP1SGX10 & EP1SGX25 Devices



Note to Figure 17–7:
(1) Fast PLL 1 in EP1SGX10 devices does not support DPA.

Figure 17–8. PLL & Channel Layout in EP1SGX40 Devices *Notes (1), (2), (3)*



Notes to Figure 17–8:

(1) Corner PLLs do not support DPA.

(2) Not all eight phases are used by the receiver channel or transmitter channel in non-DPA mode.

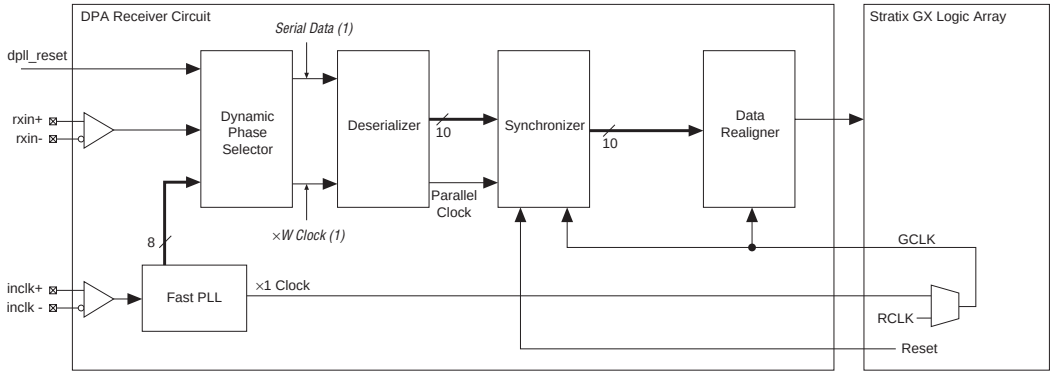
(3) The center PLLs can only clock 20 transceivers in either direction. Using Fast PLL2, you can clock a total of 40 transceivers, 20 in each direction.

DPA Operation

The DPA receiver circuitry contains the dynamic phase selector, the deserializer, the synchronizer, and the data realigner (see Figure 17–9). This section describes the DPA operation, synchronization and data realignment. You can enable or disable DPA operation on a channel-to-channel basis. In the SERDES with DPA mode, the source clock is fed to the fast PLL through the dedicated clock input pins. This clock is multiplied by the multiplication value *W* to match the serial data rate.

For information on the deserializer, see "Dedicated Source-Synchronous Circuitry" on page 17–3.

Figure 17–9. DPA Receiver Circuit

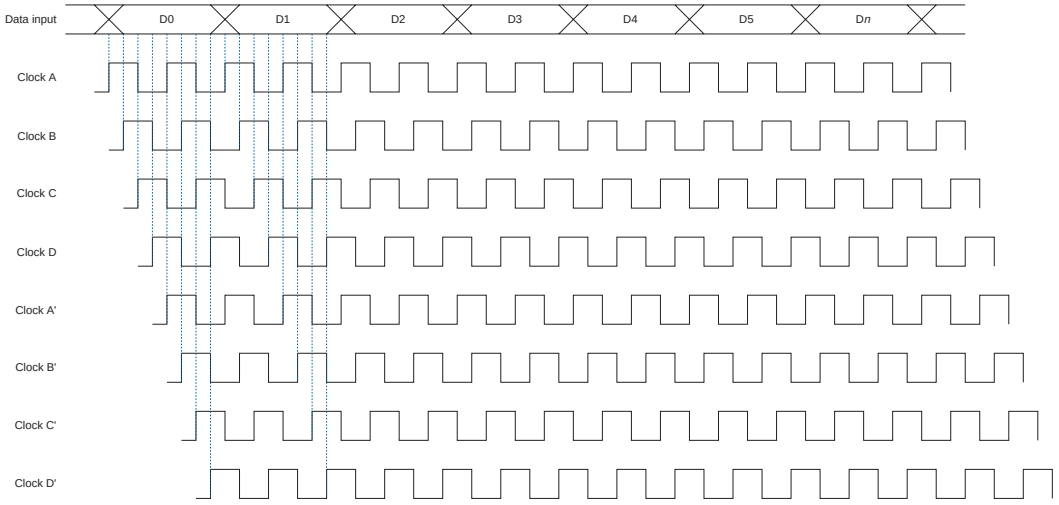


Note to Figure 17–9:
(1) These are phase-matched and retimed high-speed clocks and data.

The dynamic phase selector matches the phase of the high-speed clock and data before sending them to the deserializer.

The fast PLL supplies eight phases of the same clock (each a separate tap from a four-stage differential voltage-controlled oscillator (VCO)) to all the differential channels associated with the selected fast PLL. The DPA circuitry inside each channel locks to a phase closest to the serial data's phase and sends the retimed data and the selected clock to the deserializer. Each channel's DPA circuit can independently choose a different clock phase. The data phase detection and the clock phase selection process is automatic and continuous. The eight phases of clock gives the DPA circuit a granularity of one eighth of the unit interval (UI) or 125 ps at 1 Gbps. Figure 17–10 illustrates the clocks generated by the fast PLL circuitry and their relationship to a data stream.

Figure 17–10. Fast PLL Clocks & Data Input



Protocols, Training Pattern & DPA Lock Time

The dynamic phase aligner uses a fast PLL for clock multiplication, and the dynamic phase selector for the phase detection and alignment. The dynamic phase aligner uses the high-speed clock out of the dynamic phase selector to deserialize high-speed data and the receiver's source synchronous operations.

At each rising edge of the clock, the dynamic phase selector determines the phase difference between the clock and the data and automatically compensates for the phase difference between the data and clock.

The actual lock time for different data patterns varies depending on the data's transition density (how often the data switches between 1 and 0) and jitter characteristic. The DPA circuitry is designed to lock onto any data pattern with sufficient transition density, so the circuitry will work with current and future protocols. Experiments and simulations show that the DPA circuitry locks when the data patterns listed in Table 17–5 are repeated for the specified number of times. There are other suitable patterns not shown in Table 17–5 and/or pattern lengths, but the lock time may vary. The circuit can adjust for any phase variation that may occur during operation.

If the dynamic phase selector loses lock, the DPA circuitry sends a loss-of-lock signal for each channel to the logic array. You can then pull the dynamic phase selector RESET signal low to reset the dynamic phase selector. You can also reset the DPA operation by asserting the DPA RESET node.

Table 17–5. Training Patterns for Different Protocols

Protocols	Training Pattern	Number of Repetitions
SPI-4, NPSI	Ten 0's, ten 1's (0000000000111111111)	256
RapidIO	Four 0's, four 1's (00001111) or one 1, two 0's, one 1, four 0's (10010000)	
Other designs	Eight alternating 1's and 0's (10101010 or 01010101)	
SFI-4, XSBI	Not specified	

Phase Synchronizer

Each receiver has its own dynamic phase synchronizer. The receiver dynamic phase synchronizer aligns the phase of the parallel data from all the receivers to one global clock. The synchronizers in each channel consist of a first-in first-out (FIFO) buffer clocked by the global clock (GCLK) and parallel clock. The global clock (GCLK) and parallel clock input into the synchronizers must have identical frequency and differ only in phase. Therefore, the operation does not require an empty/full flag or read/write enable signals. The dynamic phase selector aligns each data signal with one of the eight phases of the global clock, so each signal has the same frequencies. Each synchronizer is written with a different clock phase, depending on the phase of the received data. The global clock reads all synchronizers, so all data is the same phase for use in the logic array.

Receiver Data Realignment In DPA Mode

While DPA operation aligns the incoming clock phase to the incoming data phase, it does not guarantee the parallelization boundary or byte boundary. When the dynamic phase aligner realigns the data bits, the bits may be shifted out of byte alignment, as shown in Figure 17–11.

Figure 17–11. Misaligned Captured Bit

The dynamic phase selector and synchronizer align the clock and data based on the power-up of both communicating devices, and the channel to channel skew. However, the dynamic phase selector and synchronizer cannot determine the byte boundary, and the data may need to be byte-aligned. The dynamic phase aligner's data realignment circuitry shifts data bits to correct bit misalignments.

The Stratix GX circuitry contains a data-realignment feature controlled by the logic array. Stratix GX devices perform data realignment on the parallel data after the deserialization block. The data realignment can be performed per channel for more flexibility. The data alignment operation requires a state machine to recognize a specific pattern. The procedure requires the bits to be slipped on the data stream to correctly align the incoming data to the start of the byte boundary.

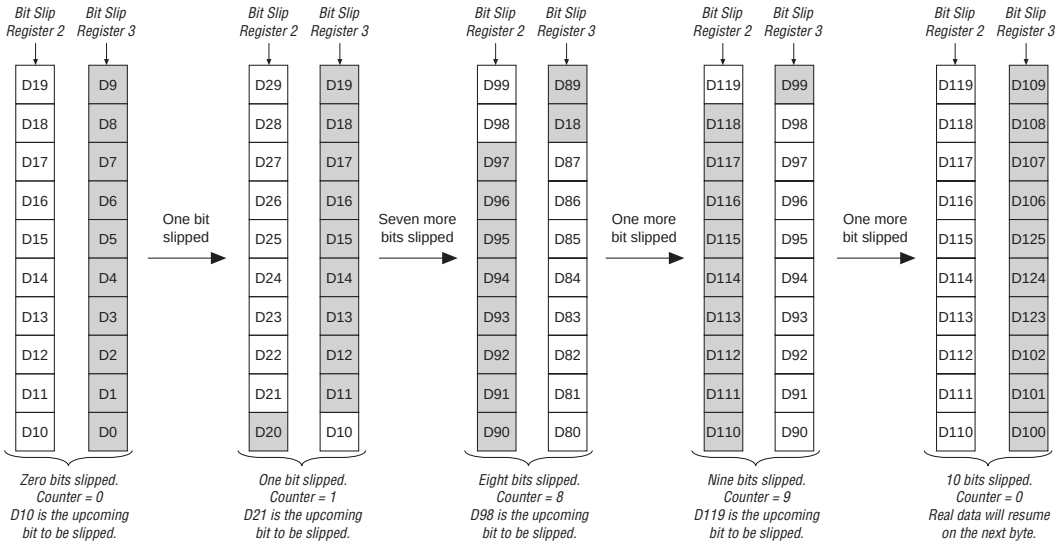
The DPA uses its realignment circuitry and the global clock for data realignment. Either a device pin or the logic array asserts the internal `rx_channel_data_align` node to activate the DPA data-realignment circuitry. Switching this node from low to high activates the realignment circuitry and the data being transferred to the logic array is shifted by one bit.

A state machine and additional logic can monitor the incoming parallel data and compare it against a known pattern. If the incoming data pattern does not match the known pattern, you can activate the `rx_channel_data_align` node again. Repeat this process until the realigner detects the desired match between the known data pattern and incoming parallel data pattern.

The DPA data-realignment circuitry allows further realignment beyond what the *J* multiplication factor allows. You can set the *J* multiplication factor to be 8 or 10. However, since data must be continuously clocked in on each low-speed clock cycle, the upcoming bit to be realigned and previous *n* –1 bits of data will be selected each time the data realignment logic's counter passes *n* –1. At this point the data is selected entirely from bit-slip register 3 (see Figure 17–12) as the counter is reset to 0. The logic

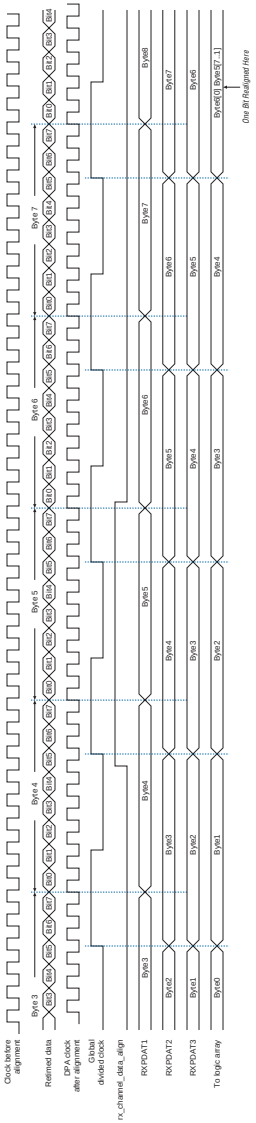
array receives a new valid byte of data on the next divided low-speed clock cycle. Figure 17–12 shows the data realignment logic output selection from data in the data realignment register 2 and data realignment register 3 based on its current counter value upon continuous request of data slipping from the logic array.

Figure 17–12. DPA Data Realigner



Use the rx_channel_data_align signal within the device to activate the data realigner. You can use internal logic or an external pin to control the rx_channel_data_align signal. To ensure the rising edge of the rx_channel_data_align signal is latched into the control logic, the rx_channel_data_align signal should stay high for at least two low-frequency clock cycles. Figure 17–13 shows the timing diagram of the DPA circuit. The byte boundary of the data is shifted by one bit on each rising-edge of the rx_channel_data_align signal. Thus one bit will be lost every time the data is slipped.

Figure 17–13. Data Realignment to Clock Timing Relationship



In order to manage the alignment procedure, a state machine should be built in the FPGA logic array to generate the realignment signal. The following guidelines outline the requirements for this state machine.

- The design must include an input synchronizing register to ensure that data is synchronized to the ×*W*/*J* clock.
- After the state machine, use another synchronizing register to capture the generated `rx_channel_data_align` signal and synchronize it to the ×*W*/*J* clock.
- The skew in the path from the output of this synchronizing register to the PLL is undefined, so the state machine must generate a pulse that is high for two ×*W*/*J* clock periods.
- The `rx_channel_data_align` generator circuitry only generates a single fast clock period pulse for each `rx_channel_data_align` pulse, so you cannot generate additional `rx_channel_data_align` pulses until the signal comparing the incoming data to the alignment pattern is reset low.
- To guarantee the state machine does not incorrectly generate multiple `rx_channel_data_align` pulses to shift a single bit, the state machine must hold the `rx_channel_data_align` signal low for at least three ×1 clock periods between pulses.

Source-Synchronous Circuitry with DPA vs. CDR

The DPA feature and source-synchronous channels are complementary features within Stratix GX devices to be used with high-speed transceiver blocks. The channels on the transceiver side of the device use an embedded circuit dedicated for receiving and transmitting serial data streams to and from the system board at frequencies up to 3.125 Gbps. These channels are clustered in serial transceiver blocks that contain four channels each and handle complex encoding and decoding schemes. If your system requires more than twenty channels, but your data rate is between 0.622 and 1.0 Gbps and you don't require the complex coding or decoding schemes, you can use the channels in banks 1 and 2 to implement the source-synchronous channels with DPA.

Software Support

You can configure the Stratix GX LVDS transmitter and receiver blocks using the MegaWizard® Plug-In Manager in the Quartus® II software. The wizard is a GUI-based ports and parameter selector for the `altlvds` megafunction. This section describes the available options for the Stratix GX LVDS transmitter and receiver.

Figure 17–14 shows the first page of the MegaWizard Plug-In Manager. With this page you can create a new megafunction, edit an existing megafunction, or copy an existing megafunction to create a variant. This section describes how to create a new megafunction.

Figure 17–14. MegaWizard Plug-In Manager (Page 1)

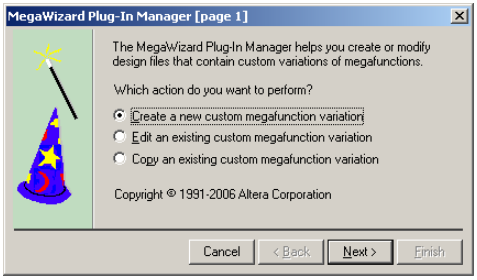
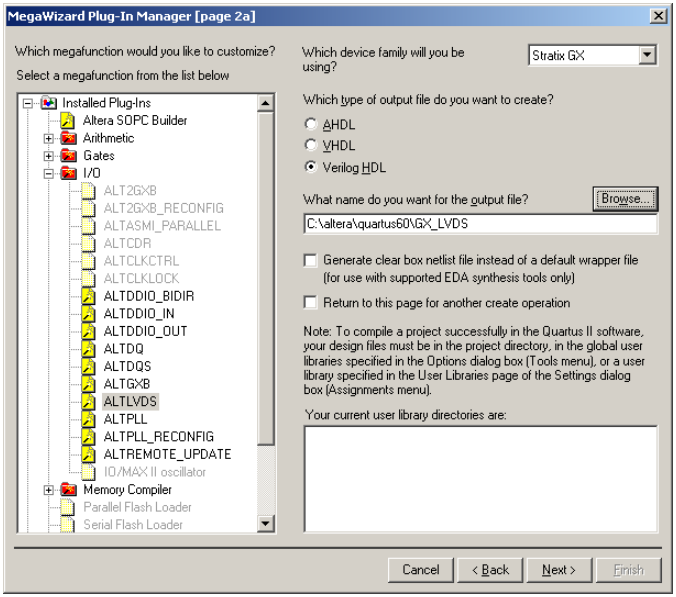


Figure 17–15 allows you to choose the megafunction to configure and the device family. You can also choose the HDL language you want the output file to be compatible with. For schematic entry, any HDL can be selected. You must provide a base name for the output files. Figure 17–15 shows the second page of the wizard.

Figure 17–15. MegaWizard Plug-In Manager (Page 2a)



Stratix GX Transmitter

Stratix GX transmitter setup starts on the page shown in Figure 17–16.

On this page, you select which device the megafunction is for in **Use which device family?** This selection activates available options for each device family. For example, for Stratix GX devices, the DPA option is available, but the Use External PLL option is not.

You can also set the number of channels and the deserialization factor. The deserialization factor determines the parallel clock frequency and the word width in the PLD logic array.

Figure 17–16. MegaWizard Plug-In Manager - altlvds Transmitter

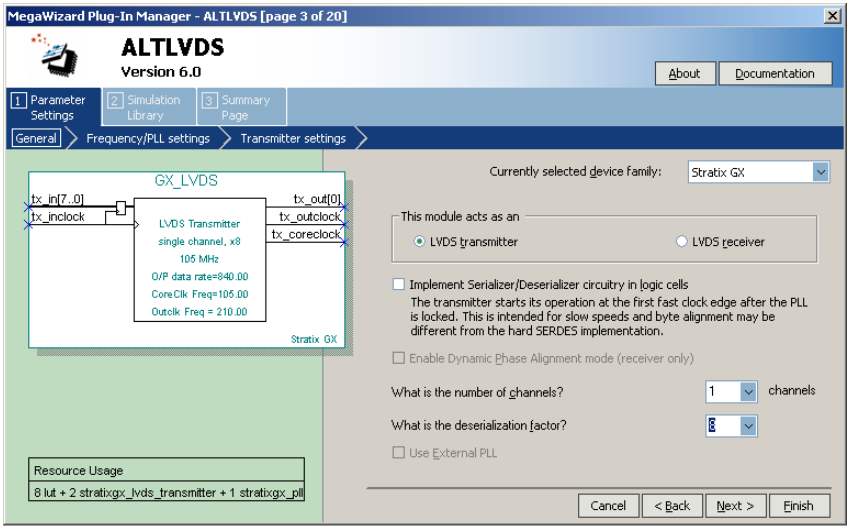


Figure 17–17 shows the `altlvds` MegaWizard Plug-In Manager page where you select the data rate and the transmitter clocking. The maximum input clock frequency is 717 MHz.

You can adjust the phase relation of the incoming data and reference clock in the **What is the phase alignment of data with respect to the rising edge of tx_inclock? (in degrees)** option.

You can enable the `tx_pll_enable` and `pll_areaset` ports. The `tx_pll_enable` port disables or enables the fast PLL used for the current instance. The `pll_areset` port resets all the counters to the fast PLL.

The **Use shared PLL(s) for receiver and transmitter** option allows you to merge the PLL for the receiver and transmitter under the correct conditions (the same data rate, SERDES factor, and input clock frequency).

Use the **Register `tx_in` input port using** option as necessary to transfer data from the PLD to the transmitter. Turn off this option if the design already contains a layer of registers before the PLD to transmitter interface. The clock feeding the register is fed by `tx_inclock` or `tx_coreclock`, depending on what feeds the data path in the PLD logic array.

Figure 17–17. MegaWizard Plug-In Manager - altlvds Transmitter

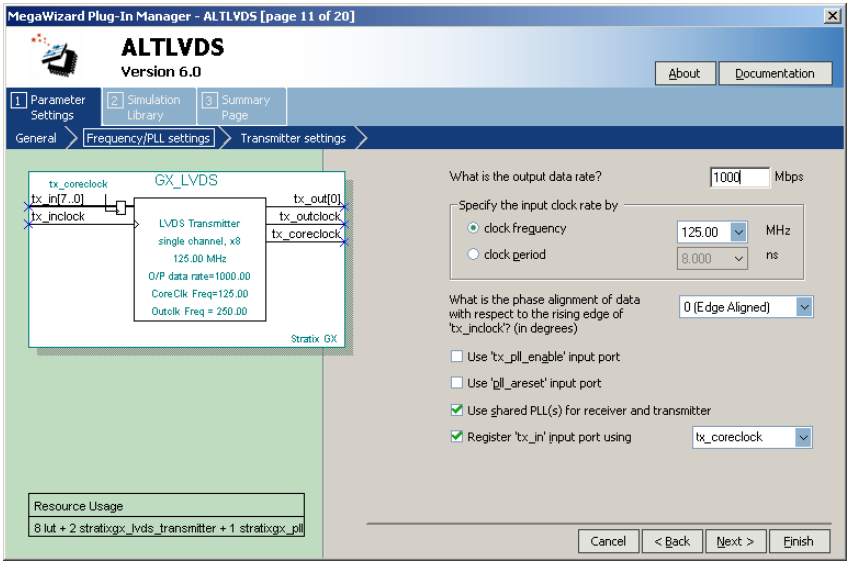
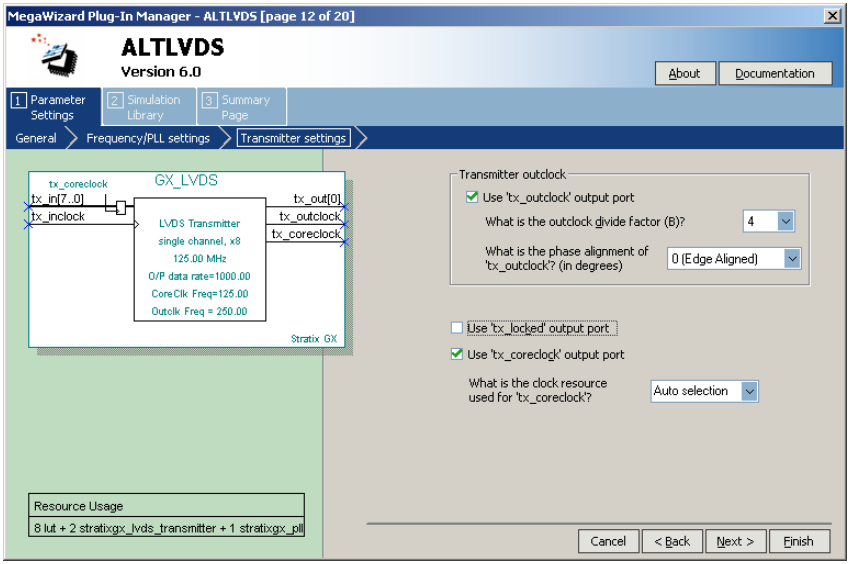


Figure 17–18 shows the last transmitter options page of the wizard. On this page you can enable the `tx_locked` and `tx_coreclock` ports. The `tx_locked` port indicates if the fast PLL is locked to the reference clock. The `tx_coreclock` port supplies the PLD with a clock, and is useful when the frequency of `tx_inclock` does not match the data rate divided by the SERDES factor.

You can set `tx_coreclock` to use a specific clock resource or, if you choose Auto selection, the Quartus II software automatically allocates an available clock resource. You set up the division factor and phase of the output clock independently of the input clock.

Figure 17–18. MegaWizard Plug-In Manager - altlvds Transmitter



Stratix GX Receiver Without DPA

Stratix GX receiver setup without DPA starts on the page shown in Figure 17–19. The number of channels and deserialization factor are similar to those of the transmitter. The DPA option is available for the Stratix GX family. In Figure 17–19, DPA mode is not selected.

Figure 17–19. MegaWizard Plug-In Manager - altlvds Receiver Without DPA

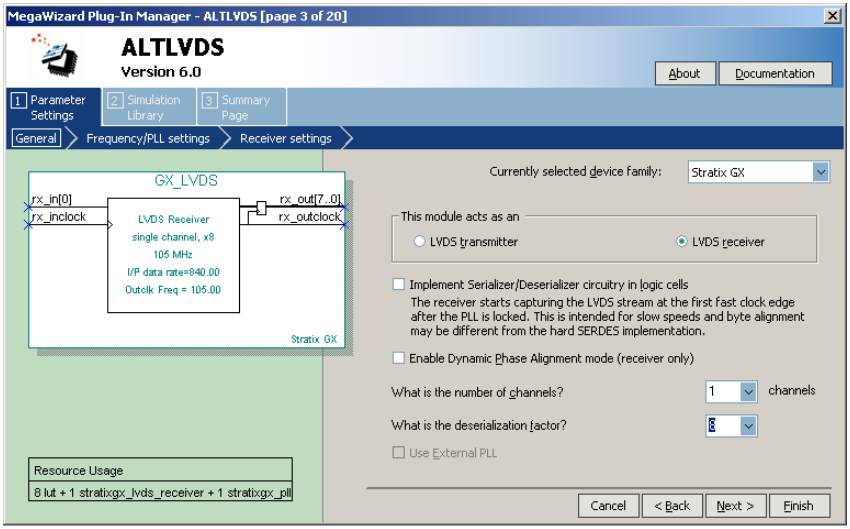


Figure 17–20 shows the page of the wizard where you can select the data rate and the receiver clocking. The maximum input clock frequency is 717 MHz. The maximum data rate for non-DPA operations is 840 Mbps. With DPA, the maximum data rate is 1000 Mbps.

The **Use shared PLL(s) for receiver and transmitter** option allows you to merge the PLL for the receiver and transmitter under the correct conditions (the same data rate, SERDES factor, and input clock frequency).

You can select the phase relationship of `rx_inclock` and `rx_in` using the **What is the phase alignment of data with respect to the rising edge of rx_inclock (in degrees)?** option.

Figure 17–20. MegaWizard Plug-In Manager - altlvds Receiver Without DPA

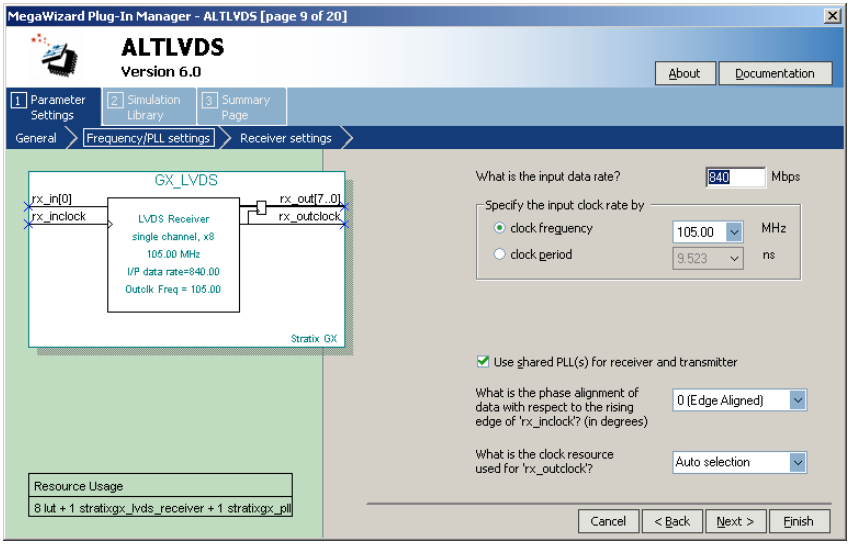
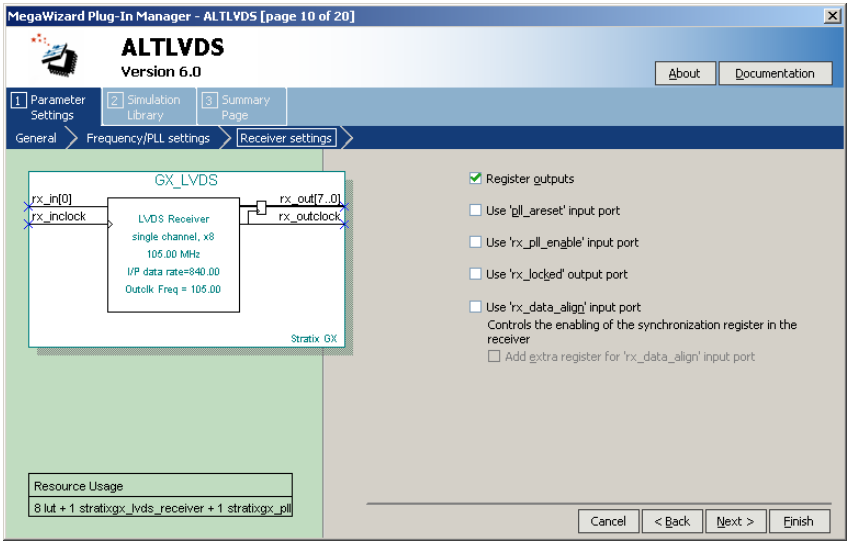


Figure 17–21 shows the last configuration page for the `altlvds` receiver without DPA.

On this page, turn on the **Register outputs** option to facilitate proper SERDES to PLD data transfer. You can turn off this option if there is already a layer of registers before the SERDES to reduce latency.

You can enable the `pll_areset`, `rx_pll_enable`, `rx_locked`, and `rx_data_align` ports on this page. The `pll_areset` port resets the counters in the fast PLL. The `rx_pll_enable` port disables or enables the fast PLL in this receiver instance. The `rx_locked` port indicates when the PLL is locked to the `rx_inclock` frequency and phase. The `rx_data_align` port pauses the fast PLL clock, thereby skipping the reception of the next bit. The `rx_data_align` port affects all channels of the receiver instance at the same time.

Figure 17–21. MegaWizard Plug-In Manager - altlvds Receiver Without DPA



Stratix GX Receiver with DPA

Stratix GX receiver setup with DPA starts on page three. The number of channels and the deserialization factor are similar to those of the transmitter. The DPA option is available for the Stratix GX family. Figure 17–22 shows the page of the `altlvds` MegaWizard Plug-In Manager with DPA selected.

Figure 17–22. MegaWizard Plug-In Manager - altlvds Receiver with DPA

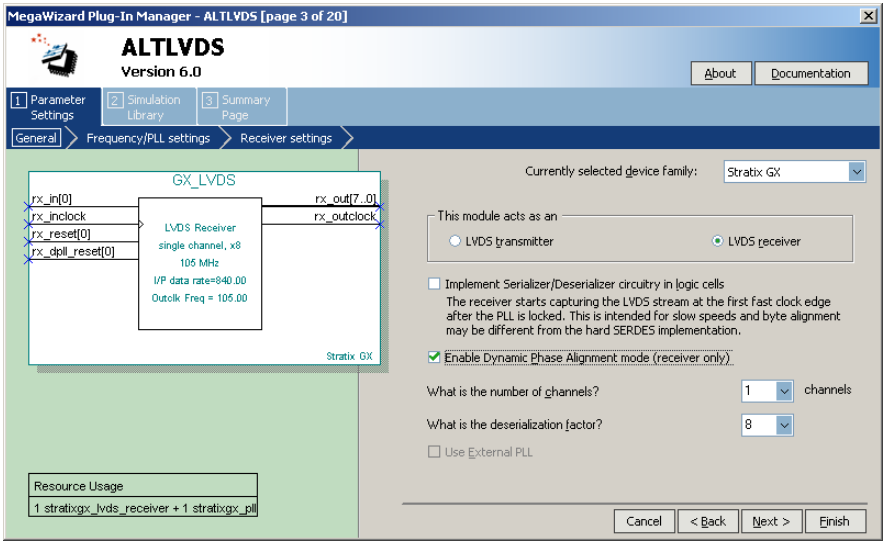


Figure 17–23 shows the page where you select the data rate and input clocking for the receiver. The maximum data rate is 1000 Mbps and the maximum input clock frequency is 717 MHz.

The **Use shared PLL(s) for receiver and transmitter** option allows you to merge the PLL for the receiver and transmitter under the right conditions (the same data rate, SERDES factor, and input clock frequency).

You can set `rx_outclock` to use a specific clock resource or, if you select Auto selection, the Quartus II software automatically allocates an available clock resource.

You must turn on **Enable the FIFO for DPA channels** option when in DPA mode. This FIFO buffer compensates for any phase differences between the selected phase in the DPA block and `rx_outclock`. There might be data errors if this option is turned off.

Figure 17–23. MegaWizard Plug-In Manager - altlvds Receiver with DPA

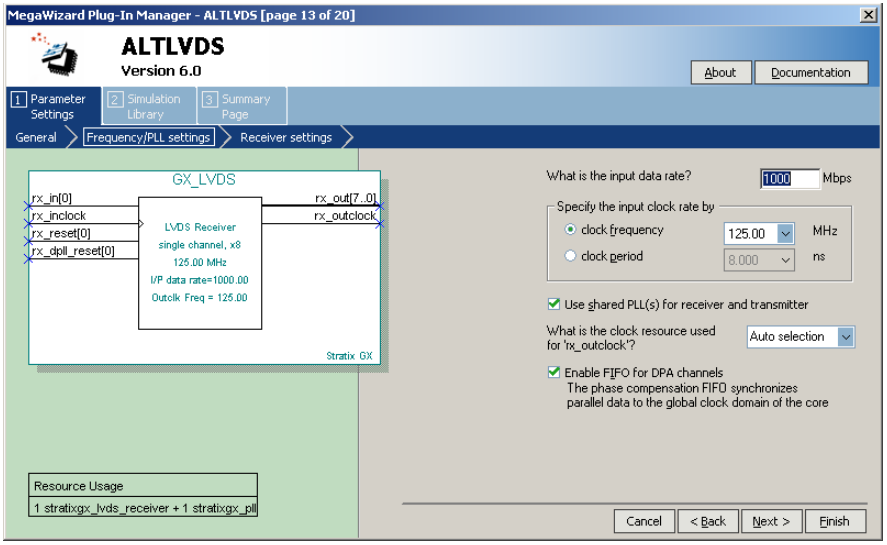


Figure 17–24 shows the last configuration page for the receiver in DPA mode.

Turn on the **Register outputs** option unless there is a layer of register in the user logic right before the SERDES block.

The `pll_areset` port resets the counters in the fast PLL. The `rx_pll_enable` port disables or enables the fast PLL in this receiver instance.

The `rx_channel_data_align` port is a channel-driven port that slips a bit for every rising edge on this port. Each DPA receiver channel has its own `rx_channel_data_align` port that can be used independently of each other.

The `rx_coreclk` and `rx_locked` ports operate the same as in the non-DPA receiver channel. The `rx_locked` port indicates when the PLL is locked to the `rx_inclock` frequency and phase. Turn on the `rx_coreclk` input port option to synchronize the `rx_outdata` to a local PLD clock instead of the parallel clock generated by the fast PLL.

Figure 17–24. MegaWizard Plug-In Manager - altlvds Receiver with DPA

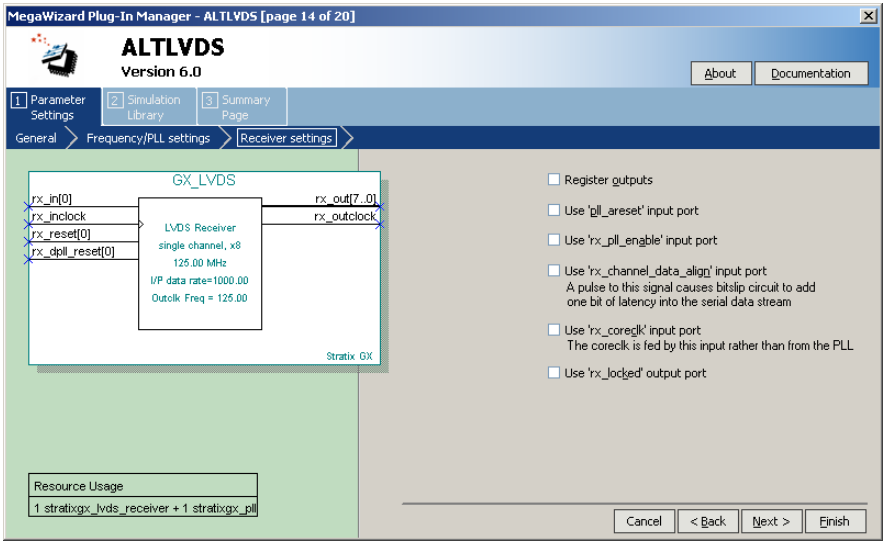


Figure 17–25 shows the Simulation Libraries page of the wizard.

Figure 17–25. MegaWizard Plug-In Manager - altlvds

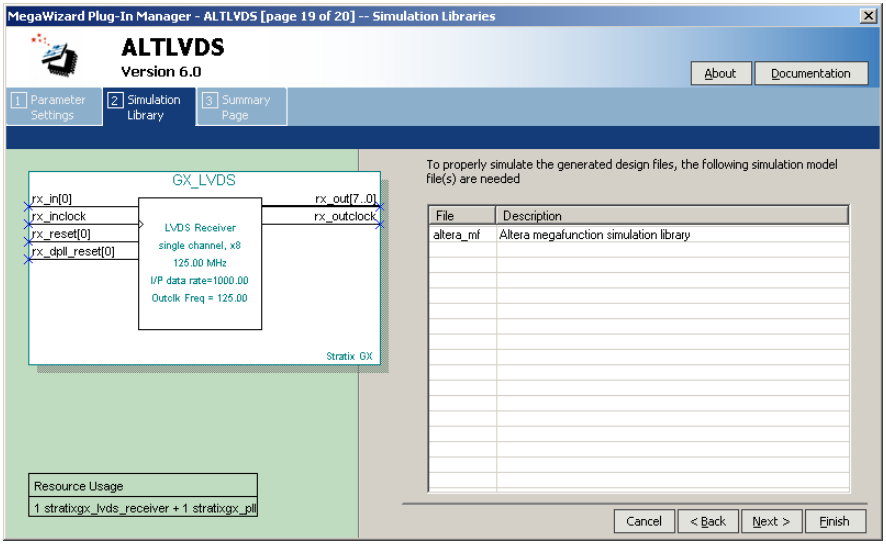
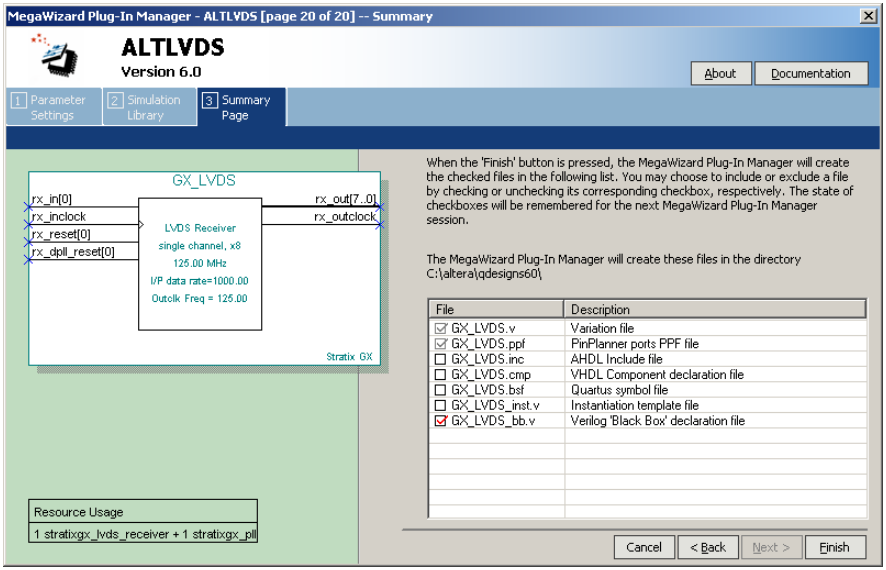


Figure 17–26 shows the last page of the MegaWizard Plug-In Manager. This page shows the files the Quartus II software generates with the options you selected on previous pages.

Figure 17–26. MegaWizard Plug-In Manager - altlvds Receiver



Summary

DPA technology eliminates the restriction of phase-matching the serial data and the source clock at the receiver channels. As a result, DPA eliminates tight board routing and topology restrictions, simplifies channel-to-channel skew calculation, and improves system performance. The combination of DPA technology with 3.125-Gbps transceivers allows Stratix GX devices to address a variety of applications and to effectively implement silicon bridges between protocols.