This chapter discusses power-up options for HardCopy® III devices and provides examples of how to replace FPGAs in the system with HardCopy III devices.

Configuring an FPGA is the process of loading the design data into the device. The Altera® SRAM-based Stratix® III FPGA requires configuration each time the device is powered up. After the device is powered down, the configuration data within the Stratix III device is lost and must be loaded again on power up.

HardCopy III devices are mask-programmed and do not require configuration. One of the advantages of HardCopy III devices is their instant-on capability upon power up. In addition, there are options to increase delay to postpone HardCopy III devices power up.

HardCopy III Power-Up Options

HardCopy III devices feature two power-up modes:

■ Instant On (no added delay)

■ Instant On After 50 ms Delay

The intent of the power-up modes is to give customers the option of choosing between Instant On and Instant On After 50 ms Delay.

Instant On mode is the fastest power-up option on a HardCopy III device. This mode is used when the HardCopy III device powers up independently while other components on the board require initialization and configuration. Therefore, you must verify that all signals which propagate to and from the HardCopy III device (for example, reference clocks and other input pins) are stable and do not interrupt HardCopy III device operation.

Some customers use Instant On After 50 ms Delay mode because the system might require the FPGA and HardCopy III devices to wait until a neighboring processor initializes completely. This mode holds the design in reset for 50 ms prior to startup. In addition to the considerations of the system, the software expects the delay from the FPGA device, which will now be replaced with the HardCopy device, and in these cases, customers choose this option.

☞ You must choose the power-up option when submitting the design database to Altera for HardCopy III devices. After the HardCopy III devices are manufactured, the power-up option cannot be changed.

Instant On mode is the traditional power-up scheme of most ASIC and non-volatile devices. Similar to Stratix III devices, HardCopy III devices go through four phases before transitioning to user mode. However, because HardCopy III devices do not require configuration, the configuration phase is replaced by a delay phase with either no added delay or a 50 ms delay.

The four phases are listed in order:

■ Power-up phase

■ Initialization phase

■ Delay phase (replacing the configuration phase)

■ Start-up phase

Instant On (No Added Delay)

In Instant On mode, after the power supplies ramp up above the HardCopy III device's power-on reset (POR) trip point, the device initiates an internal POR sequence. After t_{POR} (as shown in Figure 4–1 and Figure 4–2), the power-up phase is complete and the HardCopy III device transitions to an initialization phase, which releases the CONF_DONE signal to be pulled high. Pulling the CONF_DONE signal high indicates that the HardCopy III device is nearly ready for normal operation. For more information, refer to Figure 4–1.

During the power-up sequence, weak internal pull-up resistors can pull the user I/O pins high. When the power-up and initialization phases are complete, the I/O pins are released. If the nIO_pullup pin transitions high, the weak pull-up resistors are disabled.

> You can find the value of the internal weak pull-up resistors on the I/O pins in the Operating Conditions table of the specific FPGA's device handbook.

Instant On After 50 ms Delay

The Instant On After 50 ms delay mode is similar to Instant On mode. However, the device waits an additional 50 ms during delay phase before releasing the CONF_DONE pin. This delay is created by an on-chip oscillator. This option is beneficial if other devices on the board (such as a microprocessor) must be initialized prior to the normal operation of the HardCopy III device.

A start-up phase occurs immediately after the internal registers are reset, all PLLs used are initialized, and any I/O pins used are enabled as the device transitions into user mode.

Figure 4–1 shows an Instant On power-up waveform in which the HardCopy III device is powered up and the nCONFIG, nSTATUS, and CONF_DONE pins are driven high externally. The values for these parameters are listed in Table 4–1.

Figure 4–1. Timing Waveform for Instant On Option *(Note 1)*, *(2)*, *(3)*, *(4)*, *(5)*
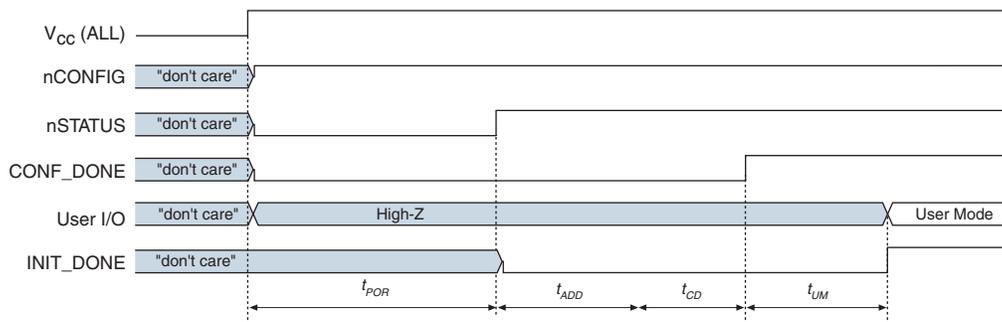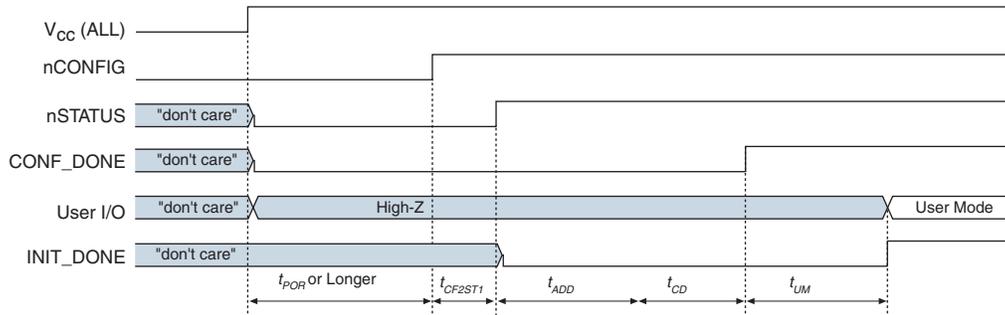

Notes to Figure 4–1:

(1) V_{CC} (ALL) represents either all the power pins or the last power pin powered up to specified operating conditions.

(2) The nCONFIG, nSTATUS, and CONF_DONE pins are weakly pulled high by an external 10 K ohm resistor to V_{CCPGM}; they must be high for this waveform to apply.

(3) User I/O pins may be tri-stated or driven before and during power-up. The nIO_pullup pin can affect the state of the user I/O pins during the initialization phase.

(4) INIT_DONE is an optional pin that can be enabled on the FPGA using the Quartus® II software. HardCopy III devices carry over the INIT_DONE functionality from the prototyped FPGA design.

(5) The nCEO pin is asserted at approximately the same time as the CONF_DONE pin is released. However, the nCE pin must be driven low externally for this waveform to apply.

Figure 4–2 shows an alternative to the power-up waveform shown in Figure 4–1. The nCONFIG pin is externally held low longer than the PORSEL delay. This delays the initialization sequence by a small amount.

In addition, Figure 4–2 shows an Instant On power-up waveform where nCONFIG is momentarily held low and nSTATUS and CONF_DONE are driven high externally. The values for these parameters are listed in Table 4–1.

Figure 4–2. Timing Waveform for Instant On Option Where nCONFIG is Held Low After Power-Up
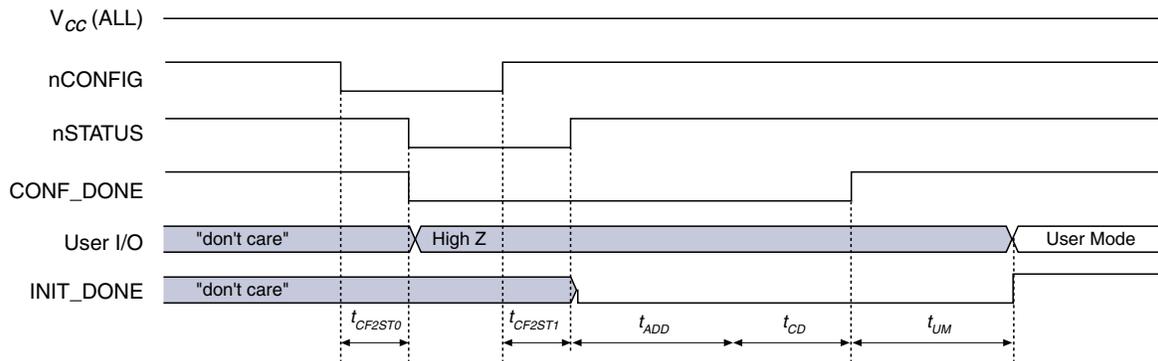

Notes to Figure 4–2:

(1) This waveform applies if nCONFIG is held low longer than t_{POR} delay.

(2) V_{CC} (ALL) represents either all the power pins or the last power pin powered up to specified operating conditions. All HardCopy III power pins must be powered within specifications.

(3) The nCONFIG, nSTATUS, and CONF_DONE pins are weakly pulled high by an external 10 K ohm resistor to V_{CCPGM}; they must be high for this waveform to apply.

(4) User I/O pins may be tri-stated or driven before and during power-up.

(5) INIT_DONE is an optional pin that can be enabled on the FPGA using the Quartus II software. HardCopy III devices carry over the INIT_DONE functionality from the prototype FPGA design.

(6) The nCEO pin is asserted at approximately the same time as the CONF_DONE pin is released. However, the nCE pin must be driven low externally for this waveform to apply. Pulsing the nCONFIG signal on an FPGA re-initializes the configuration sequence. The nCONFIG signal on a HardCopy III device also restarts the initialization sequence.

Pulsing the nCONFIG signal on an FPGA re-initializes the configuration sequence. This is the same for HardCopy ASIC devices; users pulse the nCONFIG signal on a HardCopy ASIC device and this also restarts the POR sequence. Figure 4–3 shows the Instant On behavior of the configuration signals and user I/O pins if the nCONFIG pin is pulsed while the VCC supplies are already powered up and stable. The values for these parameters are listed in Table 4–1.

Figure 4–3. Timing Waveform for the Instant-On Option When Pulsing the nCONFIG Signal *(Note 1)*, *(2)*, *(3)*, *(4)*, *(5)*

Notes to Figure 4–3:

(1) V_{CC} (ALL) represents either all the power pins or the last power pin powered up to specified operating conditions. All HardCopy III power pins must be powered within specifications as described in *Hot Socketing* sections.

(2) The nSTATUS and CONF_DONE pins must not be driven low externally for this waveform to apply.

(3) The nIO_pullup pin can affect the state of the user I/O pins during the initialization phase.

(4) INIT_DONE is an optional pin that can be enabled on the FPGA using the Quartus II software. HardCopy III devices carry over the INIT_DONE functionality from the prototyped FPGA design.

(5) The nCEO pin is asserted at approximately the same time as the CONF_DONE pin is released. However, the nCE pin must be driven low externally for this waveform to apply.

For more information about HardCopy III configuration specifications, refer to the *DC and Switching Characteristics* chapter in volume 3 of the *HardCopy III Device Handbook* and the *Hot Socketing and Power-On Reset* chapter in volume 1 of the *HardCopy III Device Handbook*.

Table 4–1 lists the timing parameters and their conditions during the power-up sequence for Figure 4–1 through Figure 4–3.

Table 4–1. Power-up Timing Parameters for HardCopy III Devices

Symbol	Parameter		Min	Typ	Max	Units
t_{POR}	PORSEL delay	PORSEL = H	12	—	—	ms
		PORSEL = L	100	—	—	ms
t_{CF2ST0}	nCONFIG low to nSTATUS low		—	—	0.8	μs
t_{CF2ST1}	nCONFIG high to nSTATUS high		—	—	270	μs
t_{ADD}	Additional delay	Instant on	50	—	90	μs
		After 50 ms delay	50	—	90	ms
t_{CD}	CONF_DONE delay		0.6	—	1.1	μs
t_{UM}	User mode delay		50	—	110	μs

☞ HardCopy III devices power up to user mode instantly, while a Stratix III device requires configuration after power up. If you are designing a board in which a HardCopy III device will replace the Stratix III device, ensure that all signals important to the HardCopy III device are ready before the HardCopy III device enters user mode. Examples of these signals are clocks, resets, and control signals. If these signals are not ready, system operation may be erratic until a proper reset and initialization of your design is performed.

Configuration Pin Compatibility

When designing a board for both a Stratix III prototype device and its companion HardCopy III device, most configuration pins required by the Stratix III device are not required by the HardCopy III device. The programmable capabilities of these configuration pins in Stratix III devices cannot carry over to the HardCopy III companion device because the HardCopy III device is not programmable. To simplify the board connection for these configuration pins, Altera recommends minimizing the power-up and configuration pins that do not carry over from the Stratix III device to the HardCopy III device.

Table 4–2 lists the dedicated and optional configuration pins for Stratix III and HardCopy III devices. If the HardCopy III device uses the pins' optional function found in Stratix III devices, the Quartus II software allows you to set these pins as dual-purpose pins. As dual-purpose pins, they have I/O functionality after power up and initialization. These pins only switch to their I/O designation when the device enters user mode (when INIT_DONE is asserted). The design may require that some signals be present when the device transitions into user mode; therefore, it is important to consider the state of these pins after power up and after the device is in user mode when designing the board and selecting the state of dual-purpose pins.

Table 4–2. Configuration Pin Compatibility (Part 1 of 2) *(Note 1)*, *(2)*, *(3)*

Stratix III		HardCopy III
Pin Name	**Function**	**Board Connection**
MSEL [2..0]	Dedicated	No connect on board
nCONFIG *(5)*	Dedicated	Required connection
DATA [7..0]	Dual-Purpose	DATA[0] retains both user I/O and optional EPCS access functions. DATA[7..1] retains user I/O functions only
DCLK	Dedicated	No connect on board, except when EPCS access is required in user mode
INIT_DONE *(6)*	Dual-Purpose (Optional)	Retains the same I/O functions from the Stratix III device
CLKUSR	Dual-Purpose (Optional)	Retains the same I/O functions from the Stratix III device
nSTATUS *(5)*	Dedicated	Required connection
CONF_DONE *(5)*	Dedicated	Required connection
nCE	Dedicated	Required connection
nCEO	Dedicated	Not required
PORSEL *(5)*	Dedicated	Required connection
ASDO	Dedicated	No connect on board, except when EPCS access is required in user mode

Table 4–2. Configuration Pin Compatibility (Part 2 of 2) *(Note 1)*, *(2)*, *(3)*

Stratix III		HardCopy III
Pin Name	Function	Board Connection
nCSO	Dedicated	No connect on board, except when EPCS access is required in user mode
nIO_PULLUP	Dedicated	Required connection
CRC_ERROR *(4)*	Dual-Purpose (Optional)	Retains the same I/O functions from the Stratix III device, but not CRC_ERROR because no device programming is needed.
DEV_CLRn	Dual-Purpose (Optional)	Retains the same I/O functions from Stratix III
DEV_OE	Dual-Purpose (Optional)	Retains the same I/O functions from Stratix III

Notes to Table 4–2:

(1) For correct operation of the HardCopy III device, pull the nSTATUS, nCONFIG, and CONF_DONE pins to V_{CCPGM}. In HardCopy III devices, these pins are designed with weak internal resistors pulled up to V_{CCPGM}. Stratix III configuration schemes require pull-up resistors on these I/O pins, so they may already be present on the board. You can remove these external pull-up resistors if doing so does not affect other FPGAs on the board.

(2) HardCopy III devices have a maximum V_{CCIO} voltage of 3.0 V, but the input I/O pin can tolerate a 3.3-V level. This applies to V_{CCPGM} voltage and all dedicated and dual-purpose pins.

(3) For HardCopy III devices, there is weak pull-up on the nSTATUS, CONF_DONE, nCONFIG, and DCLK pins. Therefore, these pins can be left floating or remain connected to external pull-up resistors. If you use Erasable Programmable Configurable Serial (EPCS) in user mode as a boot-up RAM or data access for a Nios® II processor, DCLK, DATA[0], ASDO, and nCSO need to be connected to the EPCS device.

(4) In HardCopy III devices, CRC_ERROR is hard-wired to logic 0 if the CRC feature is enabled in Stratix III devices.

(5) The PORSEL pin setting delays the POR sequence similar to the prototyping FPGA.

(6) The INIT_DONE settings option is mask-programmed into the device. You must submit these settings to Altera with the final design prior to mapping to a HardCopy III device. Using the INIT_DONE option and other dual-purpose pins (for example, the DEV_CLRn device-wide reset and DEV_OE device-wide output enable) are available in the Fitter Device Options section of the Quartus II report file.

For more information about PORSEL settings for the FPGA, refer to the *Configuration Handbook*.

Most optional configuration pins listed in Table 4–2 on page 4–6 support the various configuration schemes available in Stratix III FPGAs. Parallel programming and remote update configuration modes use most of the pins in Table 4–2 on page 4–6. HardCopy III devices are not configurable and do not support configuration emulation mode. Therefore, Altera recommends that you minimize using the optional functionality of the configuration pin in the Stratix III design by using another mode such as passive serial configuration mode.

If some of these dual-purpose pins are needed to configure the Stratix III FPGA, but will be unused after configuration, these pins remain unused on the HardCopy III device. Therefore, use caution when designing for these pins on the Stratix III and HardCopy III boards. The removal of the Stratix III device and its corresponding configuration device may leave these pins floating on the HardCopy III device if you assign them as inputs without any external means of driving them to a stable level. When selecting a Stratix III device and its device options, consider the after-configuration requirements of these pins and set them appropriately in the Quartus II software.

Examples of Mapping a Stratix FPGA Configuration to a HardCopy ASIC

This section provides examples of how HardCopy III devices replace Stratix III FPGAs using different configuration schemes.

HardCopy III Device Replacing a Stand-Alone Stratix III Device

Figure 4–4 shows the Stratix III device before it is replaced with the HardCopy III device. The example in Figure 4–5 shows the single HardCopy III device replacing a stand-alone Stratix III device. The configuration device, now redundant, is removed, and no further board changes are necessary. You can remove he pull-up resistors on the nCONFIG, nSTATUS, and CONF_DONE pins.

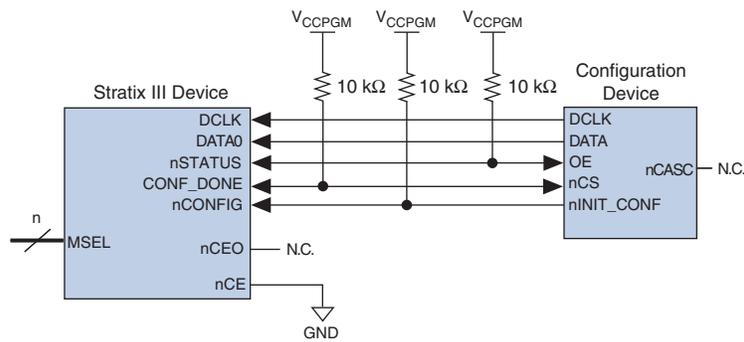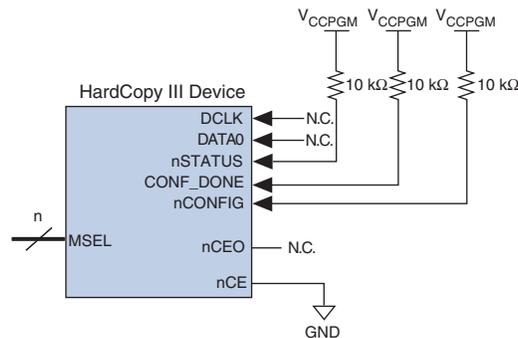**Figure 4–4. Configuration of a Stand-Alone Stratix III Device**

Figure 4–5. HardCopy III Device Replacing Stand-Alone Stratix III Device

HardCopy III Device Replacing a Stratix III Device in a Cascaded Configuration Chain

Figure 4–6 shows a design where the configuration data for the FPGAs is stored in a single configuration device and the Stratix III devices are connected in a multiple-device configuration chain. The second device in the chain is replaced with a HardCopy III device.

Figure 4–6. Configuration of Multiple FPGAs in a Cascade Chain
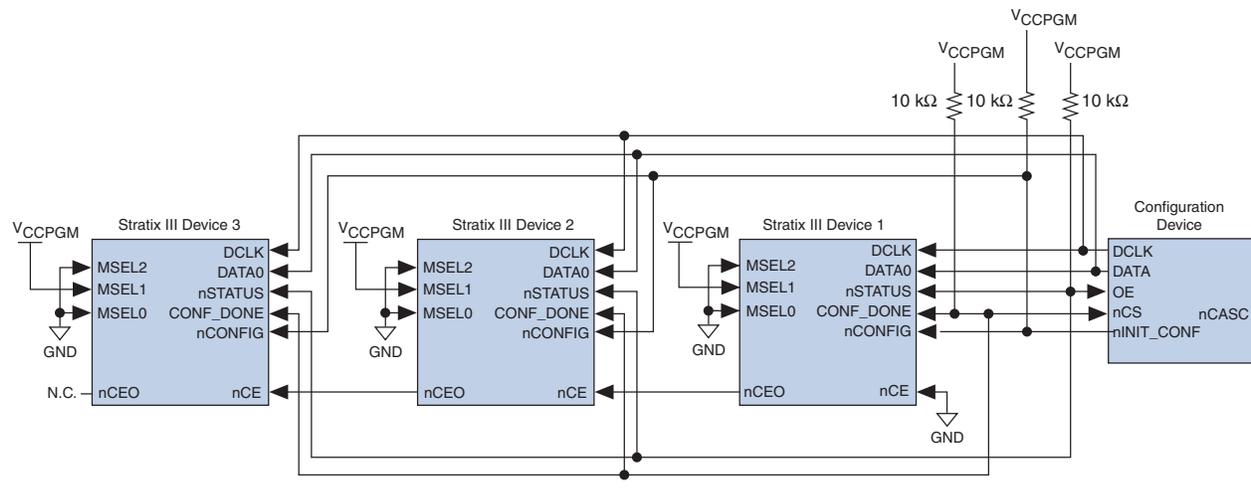
To configure FPGAs on a board with both HardCopy III devices and FPGAs, you must remove the HardCopy III device from the cascade chain. Figure 4–7 shows how the devices are connected with the HardCopy III device removed from the chain. The data in the configuration device must be modified to exclude the HardCopy III device configuration data.

Figure 4–7. Configuration with the HardCopy III Device Removed from the Cascade Chain
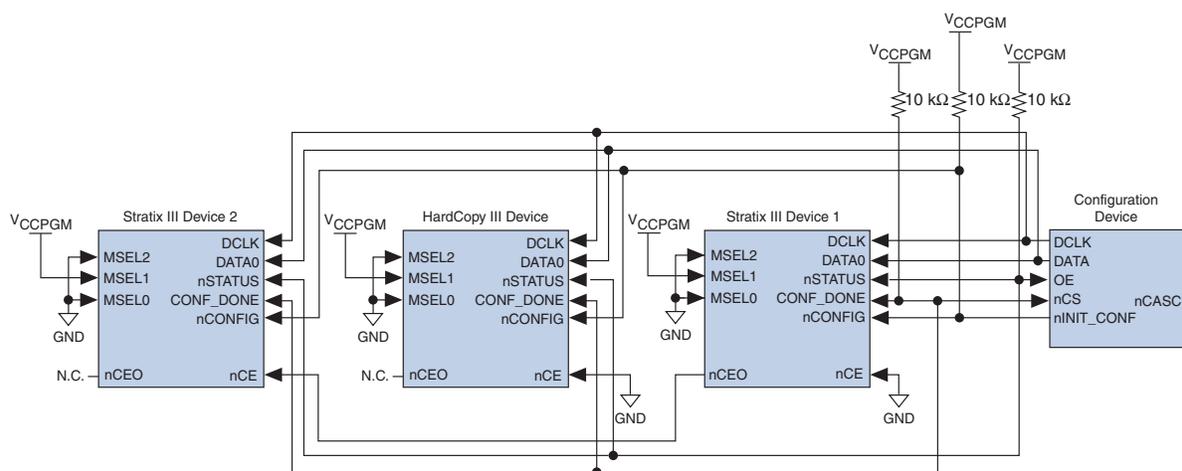
Note to Figure 4–7:

(1) The `MSEL[2:0]` pins are not used on the HardCopy III device, but they preserve the pin assignment and direction from the Stratix III device, allowing drop-in replacement.

Eliminating the HardCopy III device from the configuration chain requires the following changes:

- The configuration data stored in the configuration device must be updated to exclude the configuration data for the HardCopy III device.

- The nCE pin of the HardCopy III device must be tied to GND.

- The nCE pin of the FPGA that was driven by the HardCopy III nCEO pin must now be driven by the nCEO pin of the FPGA that precedes the HardCopy III device in the chain.

- The connections of the MSEL[2:0] pins are not required.

HardCopy III Device Replacing a Stratix III Device Configured with a Microprocessor

When you replace a Stratix III FPGA with a HardCopy III device, the microprocessor code must be modified to treat the HardCopy III device as a non-configurable device. Figure 4–8 shows an example with two Stratix III devices configured using a microprocessor or MAX® II device and the FPP configuration scheme. This example does not require changes to the board.

Figure 4–8. Multiple-Device FPP Configuration Using a Microprocessor or MAX II Device *(Note 1)*
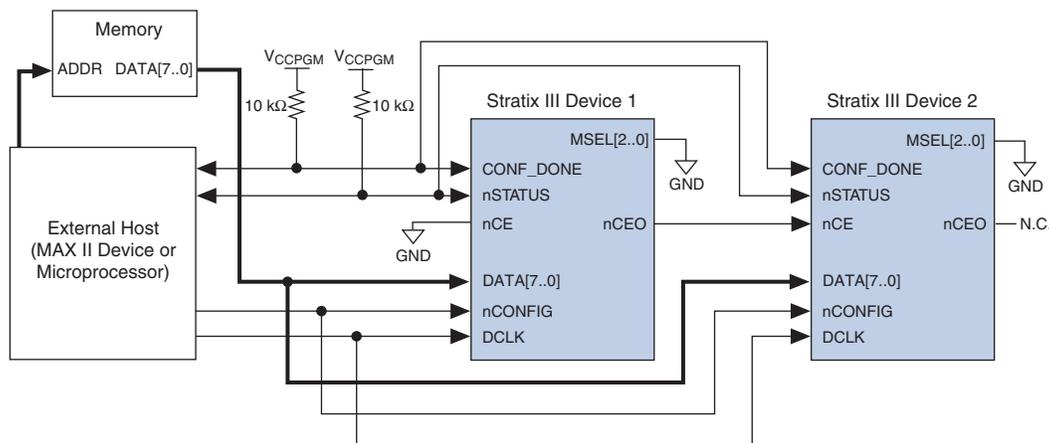
Note to Figure 4–8:

(1) Connect the pull-up resistor to a supply that provides an acceptable input signal for all devices in the chain. The V_{CCPGM} voltage meets the I/O standard's V_{IH} specification on the device and the external host.

Figure 4–9 shows how the first Stratix III device is replaced by a HardCopy III device. In this case, the microprocessor code must be modified to send configuration data only to the second device (the Stratix III device) of the configuration chain. The microprocessor can only send this data after its `nCE` pin is asserted by the first device (the HardCopy III device).

Figure 4–9. Replacement of the First FPGA in the FPP Configuration Chain with a HardCopy III Device
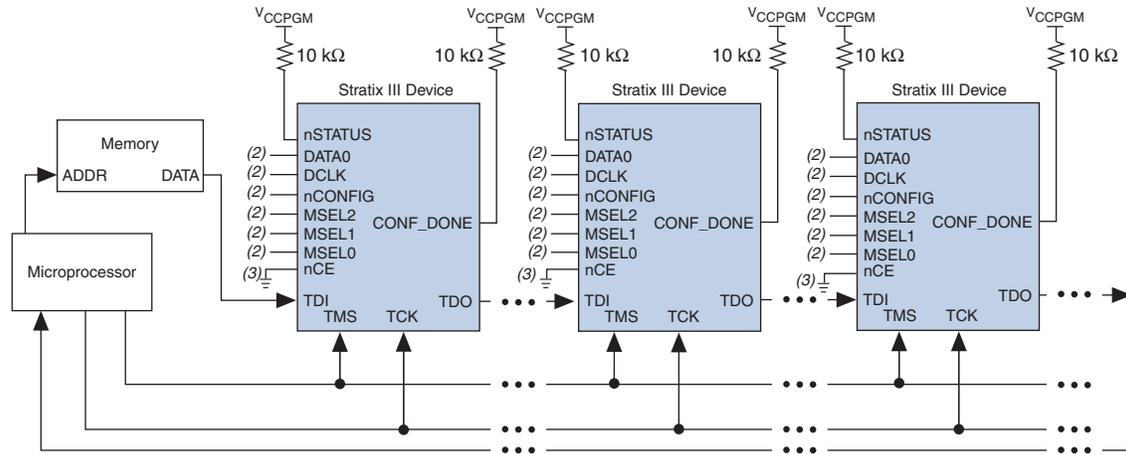

Notes to Figure 4–9:

(1) Connect the pull-up resistor to a supply that provides an acceptable input signal for all devices in the chain. The V_{CCPGM} voltage meets the I/O standard's V_{IH} specification on the device and the external host.

(2) The `DATA[7..0]` and `MSEL[2:0]` pins are not used on the HardCopy III device, but they preserve the pin assignment and direction from the Stratix III device, allowing drop-in replacement.

HardCopy III Device Replacing an FPGA Configured in a JTAG Chain

In this example, the circuit connectivity is maintained and there are no changes made to the board. You must modify the microprocessor code so that it treats the HardCopy III device as a non-configurable device. The microprocessor can achieve this by issuing a `BYPASS` instruction to the HardCopy III device. With the HardCopy III device in BYPASS mode, the configuration data passes through it to the downstream FPGAs.

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Chapter 4: Matching Stratix III Power and Configuration Requirements with HardCopy III Devices
Examples of Mapping a Stratix FPGA Configuration to a HardCopy ASIC

Figure 4–10 shows an example where there are multiple FPGAs. These devices are connected using the JTAG I/O pins for each device and programmed using the JTAG port. An on-board microprocessor generates the configuration data.

Figure 4–10. Configuring FPGAs in a JTAG Chain Using a Microprocessor
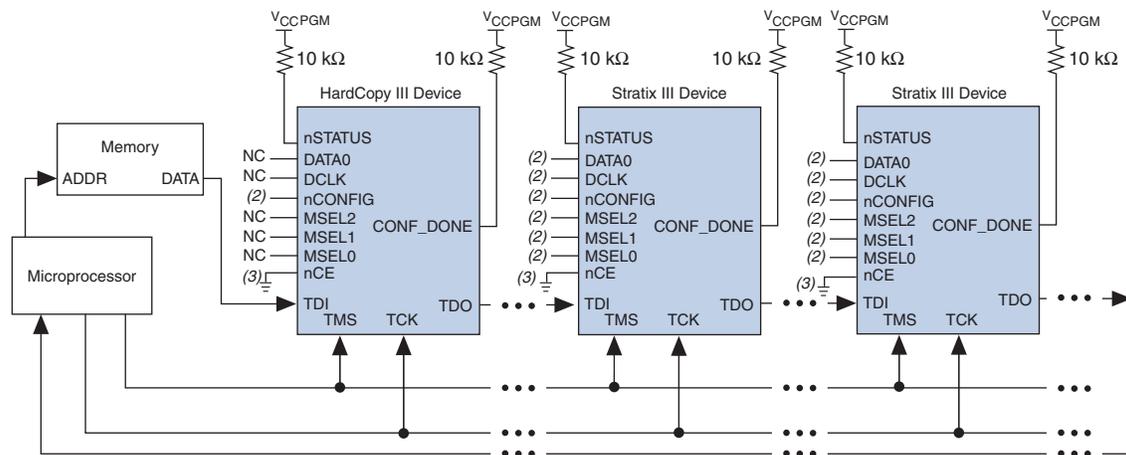

Notes to Figure 4–10:

(1) Stratix III, Stratix II, Stratix, Cyclone® III, Cyclone II, and Cyclone devices can be placed within the same JTAG chain for device programming and configuration.

(2) Connect the nCONFIG, MSEL0, MSEL1, and MSEL2 pins to support a non-JTAG configuration scheme. If only JTAG configuration is used, connect nCONFIG to V_CCPGM, and MSEL0, MSEL1, and MSEL2 to GND. Pull DATA0 and DCLK to either high or low.

(3) nCE must be connected to GND or driven low for successful JTAG configuration.

Figure 4–11 shows an example where the first Stratix III device in the JTAG chain is replaced by a HardCopy III device.

Figure 4–11. Replacement of the First FPGA in the JTAG Chain with a HardCopy III Device

Notes to Figure 4–11:

(1) Stratix III, Stratix II, Stratix, Cyclone III, Cyclone II, and Cyclone devices can be placed within the same JTAG chain for device programming configuration.

(2) Connect the nCONFIG, MSEL0, MSEL1, and MSEL2 pins to support a non-JTAG configuration scheme. If only JTAG configuration is used, connect nCONFIG to V_CCPGM, and MSEL0, MSEL1, and MSEL2 to GND. Pull DATA0 and DCLK to either high or low.

(3) nCE must be connected to GND or driven low for successful JTAG configuration.

Document Revision History

Table 4–3 shows the revision history for this chapter.

Table 4–3. Document Revision History

Date	Version	Changes
March 2012	3.2	Updated ted nCEO Board Connection in Table 4–2.
January 2011	3.1	Added Table 4–1.
June 2009	3.0	Minor updates.
December 2008	2.0	Minor text edits.
May 2008	1.0	Initial release.