2. HardCopy Design Center Implementation Process

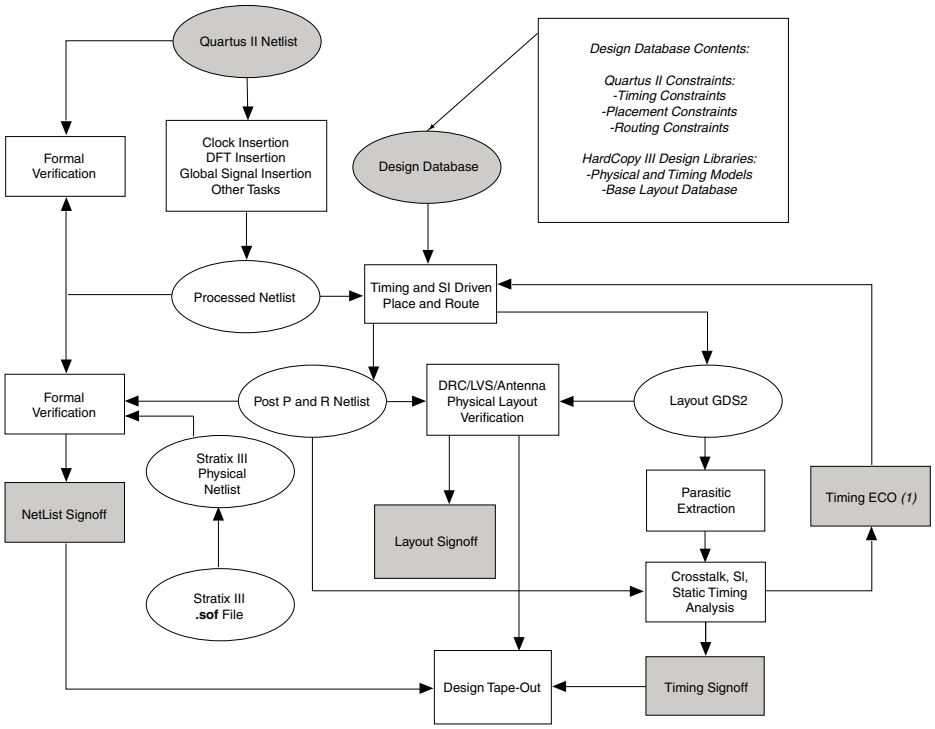
HIII53002-2.1

This chapter discusses the HardCopy® III back-end design flow executed by the Altera® HardCopy Design Center when developing your HardCopy III device.

HardCopy III Back-End Design Flow

This section outlines the back-end design process for HardCopy III devices. Figure 2–1 illustrates these steps. The design process uses both proprietary and third-party EDA tools.

Figure 2–1. HardCopy III Back-End Design Flow



Note to Figure 2–1:

(1) Refer to Figure 2–2 for more information about the timing ECO.

Design Netlist Generation

For HardCopy III designs, the Quartus® II software generates a complete Verilog gate-level netlist of your design. The HardCopy Design Center uses the netlist to start the back-end process. In addition to the Verilog gate-level netlist, the Quartus II software generates information as part of the design database submitted by you to the Altera HardCopy Design Center. This information includes timing constraints, placement constraints, and global routing information. Generation of this database provides the HardCopy Design Center with the necessary information to complete the design of your HardCopy III device.

Design for Testability

The HardCopy Design Center inserts the necessary test structures into the HardCopy III Verilog netlist. These test structures include full-scan capable registers and scan chains, JTAG, and memory testing. After adding the test structures, the modified netlist is verified using third-party EDA formal verification software against the original Verilog netlist to ensure that the test structures have not broken your netlist functionality. "Formal Verification of the Processed Netlist" explains the formal verification process.

Clock Tree and Global Signal Insertion

Along with test insertion, the HardCopy Design Center adds a local layer of clock tree buffering to connect the global clock resources to the locally placed registers in the design. Global signals with high fan-out can also use dedicated global clock resources built into the base layers of all HardCopy III devices. The HardCopy Design Center does local buffering.

Tie-Off Connections for Unused Resources

If an unused resource in a customer design still exists in the HardCopy III database, the HardCopy Design Center uses special handling on the tie-off connections for these resources. I/O ports of unused resources are connected to power or ground so that the resources are in a lower power state. This is achieved by using the same metal layers that are used to configure and connect all resources used in the design.

Formal Verification of the Processed Netlist

After all design-for-testability logic, clock tree buffering, global signal buffering, and tie-off connection are added to the processed netlist, the HardCopy Design Center uses third-party EDA formal verification software to compare the processed netlist with your submitted Verilog netlist generated by the Quartus II software. Added test structures are constrained to bypass mode during formal verification to verify that your design's intended functionality is unchanged.

Timing and Signal Integrity Driven Place and Route

Placement and global signal routing is principally done in the Quartus II software before submitting the HardCopy III design to the HardCopy Design Center. With the Quartus II software, you control the placement and timing driven placement optimization of your design. The Quartus II software also does global routing of your signal nets, and passes this information in the design database to the HardCopy Design Center to do the final routing. After the design is submitted, Altera engineers use the placement and global routing information provided in the design database to do final routing and timing closure, and to perform signal integrity and crosstalk analysis. This may require buffer and delay cell insertion in the design through an engineering change order (ECO). The resulting post place and route netlist is verified again with the source netlist and the processed netlist to guarantee that functionality was not altered in the process. For more details about back-end timing closure and timing ECOs, refer to "Back-End Timing Closure" and "Timing ECOs".

Parasitic Extraction and Timing Analysis

After the HardCopy Design Center places and routes your design, a **.gds2** design file is generated. Parasitic extraction uses the physical layout of the design stored in the **database** to extract the resistance and capacitance values for all signal nets in the design. The HardCopy Design Center uses these parasitic values to calculate the path delays through the design for static timing analysis and crosstalk analysis.

Back-End Timing Closure

The Quartus II software provides a pre-layout estimation of your HardCopy III design performance. The Altera HardCopy Design Center then uses industry leading EDA software to complete the back-end layout and extract the final timing results prior to tape-out. Altera performs rigorous timing analysis on the HardCopy III design during its back-end implementation, ensuring that it meets the required timing constraints. After generating the customized metal interconnect for the HardCopy III device, Altera checks the design timing with a static timing analysis tool. The static timing analysis tool may report timing violations, which are reviewed with the customer.

The critical timing paths of the HardCopy III device may be different from the corresponding paths in the Stratix III FPGA revision; these differences can exist for several reasons. While maintaining the same set of features as the corresponding Stratix III FPGA, HardCopy III devices have a highly optimized die size to make them as small as possible. Because of the customized interconnect structure that makes this optimization possible, the delay through each signal path is different from the original Stratix III FPGA design. Therefore, it is important to constrain the Stratix III FPGA and HardCopy III devices to the exact, system-level timing requirements that need to be achieved. Timing violations seen in the Quartus II project or in the HardCopy Design Center back-end process must be fixed or waived prior to the design tape-out.

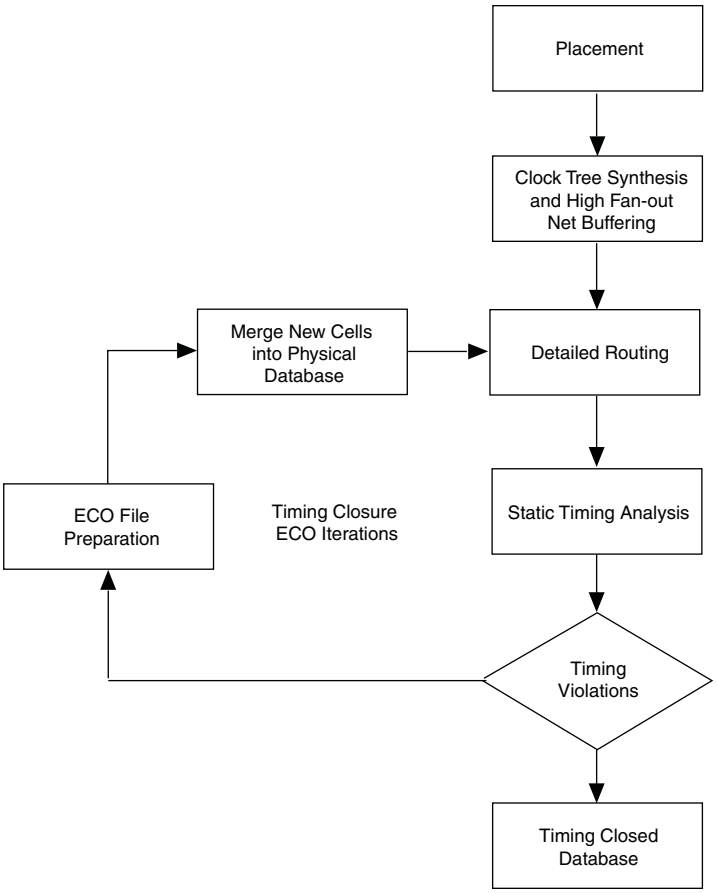
Timing ECOs

In an ASIC design, small incremental changes to a design database are termed ECOs. In the HardCopy III design flow, timing closure ECOs are performed by Altera's HardCopy Design Center after the initial post-layout timing data is available.

The Altera HardCopy Design Center runs static timing analysis on the design. This analysis may show that the place and route tool was not able to close timing automatically on some paths. The HardCopy Design Center engineer will determine the best way to fix the timing on these paths (for example, by adding delay cells to fix a hold time violation). This list of changes is fed back into the place and route tool which subsequently implements the changes. The impact to the place and route database is minimized by maintaining all of the pre-existing placement and routing, and only changing the paths that need improvement.

The parasitic resistances and capacitances of the customized interconnect are extracted, and are used in conjunction with the static timing analysis tool to re-check the timing of the design. Detected crosstalk violations on signals are fixed by adding additional buffering to increase the setup or hold margin on victim signals. In-line buffering and small buffer tree insertion is done for signals with high fan-out, high transition times, or high capacitive loading. Figure 2–2 shows this flow in more detail.

Figure 2–2. Timing Closure ECO Flow Diagram



The back-end flow produces the final signoff timing for your HardCopy III device. The Quartus II software produces the timing report for HardCopy III based on global routing and does not factor in the exact physical parasitic of the routed nets. The Quartus II software also does not factor in the crosstalk effect that neighboring nets can have on interconnect capacitance.

Formal Verification of the Post-Layout Netlist

In addition to the **.gds2** file and parasitic files that are generated by the HardCopy Design Center, the post-layout netlist is also generated for formal verification with Stratix III FPGAs. The HardCopy Design Center checks the functional equivalence between the Stratix III FPGA prototype and HardCopy III device according to the Stratix III **.sof** file and HardCopy III post-layout netlist.

Layout Verification

When the Timing Analysis reports that all timing requirements are met, the design layout goes into the final stage of verification for manufacturability. The HardCopy Design Center performs physical Design Rule Checking (DRC), antenna checking of long traces of signals in the layout, and a comparison of layout to the design netlist, commonly referred to as Layout Versus Schematic (LVS). These tasks guarantee that the layout contains the exact logic represented in the place-and-route netlist and the physical layout.

Design Signoff

The Altera HardCopy III back-end design methodology has a thorough verification and signoff process, guaranteeing your design's functionality. Signoff occurs after completing the final place-and-route netlist functional verification, layout verification for manufacturability, and timing analysis. After achieving all three signoff points, Altera begins the manufacturing of the HardCopy III devices.

Conclusion

Altera's back-end design methodology ensures that your design converts successfully from your Stratix III FPGA prototype to the HardCopy III ASIC. Altera's unique system development methodology offers an excellent way for you to benefit from using a Stratix III FPGA for design prototyping and debugging, and using a HardCopy III ASIC for volume production.

Document Revision History

Table 2–1 shows the revision history for this document.

Table 2–1. Document Revision History

Date	Version	Changes
January 2011	2.1	Minor text edits.
December 2008	2.0	■ Minor text edits. ■ Chapter listed as p/n 52001 in ADoQS for this version release.
May 2008	1.0	Initial release.