2. Extended Temperature Range for HardCopy III Devices

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As part of the Altera® initiative to provide enhanced commercial off-the-shelf (COTS) devices for wider applications, the temperature range for the HardCopy® III device families has been extended to enable operation across the extended temperature range (–40°C to 125°C). This extension allows design engineers who are working on systems with stringent temperature requirements to benefit from the cost savings by using commercially available HardCopy III ASICs.

HardCopy III ASICs are extremely robust and capable of operating across a wide temperature range with excellent reliability. This chapter describes the Altera support for HardCopy III extended temperature range operation with the appropriate background information. It also explains how to use HardCopy III devices across the extended temperature range operation, along with any limitations in operation that affect the HardCopy III datasheet specifications.

These guidelines have been determined through additional characterization of HardCopy III devices on samples of production silicon across the extended temperature ranges (125°C and –40°C). While characterizations demonstrate correct operation across extended temperatures by design, production testing of industrial grade devices for extended temperature range operation is performed at 100°C.

Extended Temperature Support

Extended temperature operation requires additional timing margin over industrial temperature operation to compensate for the potentially increased variation of f_{MAX} across temperature. For the Stratix® III FPGA prototype devices, the increased timing margin is achieved by compiling the design using an industrial I4 part and setting the temperature range from –40°C to 125°C in the Quartus® II software. The Quartus II software provides separate timing models at 125°C for slow corner and –40°C for fast corner. By selecting a HardCopy III companion device and extended temperature range (–40°C min and 125°C max) in the operating temperature condition, the Quartus II software uses the appropriate timing models to ensure that the constraints of extended temperature range operation are met.

The extended temperature range support design flow is the same as that for commercial and industrial devices. Use the Quartus II HardCopy III Advisor to help guide you through the flow to ensure your design is ready for submission to the Altera HardCopy Design Center.

Table 2–1 lists the HardCopy III device part numbers that support the extended temperature operation.

Table 2–1. HardCopy III Extended Temperature Support

HardCopy Family	Device	Package	Extended Temperature Support
HardCopy III	HC325	All	Yes
	HC335	All	Yes

Software Support

The HardCopy III extended temperature grade device models are supported in the following versions of these tools:

- The PowerPlay Early Power Estimator (EPE) or the PowerPlay Power Analyzer software, version 11.1 or later. Download these tools from: www.altera.com/support/devices/estimator/pow-powerplay.html
- The Quartus II software, version 11.1 or later. Download the software from: www.altera.com/products/software/quartus-ii/subscription-edition/qts-se-index.html

Limitations to Datasheet Specifications

This section describes the limitations to the HardCopy III datasheet specifications when operating HardCopy III devices at extended temperature range. Characterization results show that HardCopy III device operation across the extended temperature range is bounded by the industrial grade of the datasheet specifications and any relevant errata, except where noted below.

DSP Block Specifications

Table 2–2 lists the HardCopy III DSP block performance specifications.

Table 2–2. HardCopy III DSP Block Performance Specifications ***(Note 1)***

Mode	Number of Multipliers	Maximum Frequency		Unit
		Flipchip	Wirebond	
9 x 9-bit multiplier (a, c, e, g) *(2)*	1	315	252	MHz
9 x 9-bit multiplier (b, d, f, h) *(2)*	1	375	300	MHz
12 x 12-bit multiplier (a, e) *(3)*	1	315	252	MHz
12 x 12-bit multiplier (b, d, f, h) *(3)*	1	375	300	MHz
18 x 18-bit multiplier	1	400	320	MHz
36 x 36-bit multiplier	1	315	252	MHz
Double mode	1	315	252	MHz
18 x 18-bit multiply accumulator	4	330	264	MHz
18 x 18-bit multiply adder	4	345	276	MHz
18 x 18-bit multiply adder-signed full precision	2	345	276	MHz
18 x 18-bit multiply adder with loopback *(4)*	2	300	240	MHz
36-bit shift (32-bit data)	1	330	264	MHz

Notes to Table 2–2:

(1) The maximum is for a fully pipelined block with **round** and **saturation** disabled.

(2) The DSP block implements eight independent 9 x 9-bit multipliers using a, b, c, and d for the top half of the DSP block; and e, f, g, and h for the bottom half of the DSP block multipliers.

(3) The DSP block implements six independent 12 x 12-bit multipliers using a, b, and d for the top half of the DSP block; and e, f, and h for the bottom half of the DSP block multipliers.

(4) The maximum for a non-pipelined block with loopback input registers disabled with **round** and **saturation** disabled.

TriMatrix Memory Block Specifications

Table 2–3 lists the HardCopy III TriMatrix memory block specifications.

Table 2–3. HardCopy III TriMatrix Memory Block Performance Specifications (Part 1 of 2)

Memory	Mode	TriMatrix Memory	Maximum Frequency		Unit
			Flipchip	Wirebond	
MLAB	Single port 16 × 10	1	450	338	MHz
	Simple dual-port 16 × 20	1	450	338	MHz
	ROM 64 × 10	1	450	338	MHz
	ROM 32 × 20	1	450	338	MHz
M9K	Single-port 8K × 1	1	405	304	MHz
	Single-port 4K × 2 or 2K × 4	1	405	304	MHz
	Single-port 1K × 9, 512 × 18, or 256 × 36	1	460	345	MHz
	Simple dual-port, 8K × 1	1	400	300	MHz
	Simple dual-port, 4K × 2 or 2K × 4	1	400	300	MHz
	Simple dual-port, 1K × 9, 512 × 18, or 256 × 36	1	400	300	MHz
	Simple dual-port, 8K × 1, 4K × 2, or 2K × 4 with the read-during-write option set to “Old Data”	1	265	199	MHz
	Simple dual-port, 1K × 9, 512 × 18, or 256 × 36 with the read-during-write option set to “Old Data”	1	265	199	MHz
	True dual-port, 8K × 1	1	435	326	MHz
M9K	True dual-port, 4K × 2 or 2K × 4	1	370	278	MHz
	True dual-port, 1K × 9 or 512 × 18	1	370	278	MHz
	True dual-port, 8K × 1, 4K × 2, or 2K × 4 with the read-during-write option set to “Old Data”	1	245	184	MHz
	True dual-port, 1K × 9 or 512 × 18 with the read-during-write option set to “Old Data”	1	245	184	MHz
	ROM 1P, 8K × 1, 4K × 2, or 2K × 4	1	405	304	MHz
	ROM 1P, 1K × 9, 512 × 18, or 256 × 36	1	405	304	MHz
	ROM 2P, 8K × 1, 4K × 2, or 2K × 4	1	405	304	MHz
	ROM 2P, 1K × 9, or 512 × 18	1	405	304	MHz
	Min Pulse Width (Clock High Time)	—	800	1067	ps
	Min Pulse Width (Clock Low Time)	—	625	831	ps

Table 2–3. HardCopy III TriMatrix Memory Block Performance Specifications (Part 2 of 2)

Memory	Mode	TriMatrix Memory	Maximum Frequency		Unit
			Flipchip	Wirebond	
M144K	True dual-port 16K × 9 or 8K × 18	1	310	233	MHz
	True dual-port 4K × 36	1	310	233	MHz
	Simple dual-port 16K × 9 or 8K × 18	1	325	244	MHz
	Simple dual-port 4K × 36 or 2K × 72	1	325	244	MHz
	ROM 1 Port	1	420	315	MHz
	ROM 2 Port	1	380	285	MHz
	Single-port 16K × 9 or 8K × 18	1	350	263	MHz
	Single-port 4K × 36	1	350	263	MHz
	True dual-port 16K × 9, 8K × 18, or 4K × 36 with the read-during-write option set to “Old Data”	1	200	150	MHz
M144K	Simple dual-port 16K × 9, 8K × 18, 4K × 36, or 2K × 72 with the read-during-write option set to “Old Data”	1	200	150	MHz
	Simple dual-port 2K × 64 (with ECC)	1	245	171	MHz
	Min Pulse Width (Clock High Time)	—	1382	1843	ps
	Min Pulse Width (Clock Low Time)	—	690	920	ps

Transceiver Performance Specifications

Transceiver performance is supported up to 3Gbps protocols only.

For additional information about extended temperature support, refer to the *Stratix III Military Temperature Range Support Technical Brief*.

Document Revision History

Table 2–4 lists the revision history for this document.

Table 2–4. Document Revision History

Date	Version	Changes
March 2012	1.0	Initial release.