10. IEEE 1149.1 (JTAG) Boundary Scan Testing in HardCopy III Devices

HIII51010-3.1

All HardCopy® III ASICs provide Joint Test Action Group (JTAG) boundary-scan test (BST) circuitry that complies with the IEEE Std. 1149.1 specification. The BST architecture offers the capability to efficiently test components on PCBs with tight lead spacing. Pin connections can be tested without using physical test probes, and functional data can be captured while a device is in normal operation. Boundary-scan cells in a device can force signals onto pins, or capture data from pin or core logic signals. Forced test data is serially shifted into the boundary-scan cells. Captured data is serially shifted out and externally compared to expected results.

A device using the JTAG interface uses four required pins: `TDI`, `TDO`, `TMS`, and `TCK`, and one optional pin, `TRST`. The `TCK` pin has an internal weak pull-down resistor, and the `TDI`, `TMS`, and `TRST` pins have internal weak pull-up resistors. The `TDO` output pin and all the JTAG input pins are powered by the 2.5-V/3.0-V V_{CCPD} supply of I/O bank 1A.

For more information about the BST architecture and JTAG instructions supported in Stratix III devices, refer to the *IEEE 1149.1 (JTAG) Boundary-Scan Testing in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*.

For more information about the JTAG pin description, refer to the *IEEE 1149.1 (JTAG) Boundary-Scan Testing in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*.

HardCopy III devices only support a maximum I/O voltage of 3.0 V. Consider this when designing your Stratix® III FPGA prototypes and your board so you can successfully map the HardCopy III device.

JTAG Instructions

Table 10–1 shows the JTAG instructions supported in HardCopy III devices for boundary-scan testing (BST). These 10-bit instructions are also supported in Stratix III devices. However, HardCopy III devices do not support the Stratix III JTAG instructions used for in-circuit reconfiguration (ICR), because HardCopy III devices do not require configuration.

For more information about the BST architecture and JTAG instructions supported in Stratix III devices, refer to the *IEEE 1149.1 (JTAG) Boundary-Scan Testing in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*.

Table 10–1. HardCopy III JTAG Instructions

JTAG Instruction	Instruction Code	Description
SAMPLE/PRELOAD	00 0000 0101	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins.
EXTEST *(1)*	00 0000 1111	Allows the external circuitry and board-level interconnects to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	11 1111 1111	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.
USERCODE	00 0000 0111	Loads the 32-bit user code into the device identification register and places the register between the TDI and TDO pins, allowing the user code to be serially shifted out of TDO.
IDCODE	00 0000 0110	Loads the 32-bit ID code into the device identification register and places the register between the TDI and TDO pins, allowing the ID code to be serially shifted out of TDO.
HIGHZ *(1)*	00 0000 1011	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation while tri-stating all of the I/O pins.
CLAMP *(1)*	00 0000 1010	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation while holding I/O pins to a state defined by the data in the boundary-scan register.

Note to Table 10–1:

(1) The bus hold and weak pull-up resistor features override the high-impedance state of HIGHZ, CLAMP, and EXTEST.

Similar to Stratix III devices, HardCopy III devices support the SignalTap® II Embedded Logic Analyzer, which monitors design operation over a period of time through the JTAG interface. The SignalTap II Embedded Logic Analyzer is a useful feature during the device prototyping phase, but should be removed if not required after you map the design to a HardCopy III device. HardCopy III devices are mask programmed, and the SignalTap II logic cannot be removed after the HardCopy III device is fabricated.

IDCODE and USERCODE

The IDCODE instruction gives you the ability to shift out a 32-bit identification (ID) code from HardCopy III devices. ID codes are different in Stratix III devices and unique for each HardCopy III device. The ID code can be used to determine the correct device during BST. When the IDCODE instruction is issued, the ID code is loaded into a 32-bit device identification register for shifting out. Table 10–2 shows the ID codes for the HardCopy III devices.

Table 10–2. 32-Bit HardCopy III Device IDCODE *(Note 1)*, *(2)*

Device	IDCODE (32 Bits)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	LSB (1 Bit)
HC325	0000	0010 0010 0010 0101	000 0110 1110	1
HC335	0000	0010 0010 0011 0101	000 0110 1110	1

Notes to Table 10–2:

(1) The most significant bit (MSB) is on the left.

(2) The least significant bit (LSB) of IDCODE is always 1.

You can use the USERCODE instruction to shift out a 32-bit user code, which can also be used to uniquely identify the device. Unlike Stratix III devices, the user code in HardCopy III devices is mask programmed and cannot be changed after the silicon is fabricated. If the designer does not select a user code, the user code is mask programmed to the default values. When the USERCODE instruction is issued, the 32-bit user code is loaded into the same 32-bit device identification register used for the IDCODE instruction. The user code can then be serially shifted out.

Boundary-Scan Register

The boundary-scan register length for HardCopy III devices differs from Stratix III devices. The length also varies for each HardCopy III device depending on the device density and available I/O pin count. Table 10–3 lists the boundary-scan register length for HardCopy III devices.

Table 10–3. HardCopy III Boundary-Scan Register Length

Device	Boundary-Scan Register Length
HC325	1524
HC335	2670

Boundary-Scan Testing on HardCopy III Devices

The boundary-scan description language (BSDL), a subset of VHDL, provides a syntax that allows you to describe the features of an IEEE Std. 1149.1 BST-capable device that can be tested.

There are two versions of the BSDL Customizer tool that you can use. The pre-configuration version generates a BSDL file for use before the device enters user mode, and the post-configuration version generates a BSDL file for use after the device enters user mode.

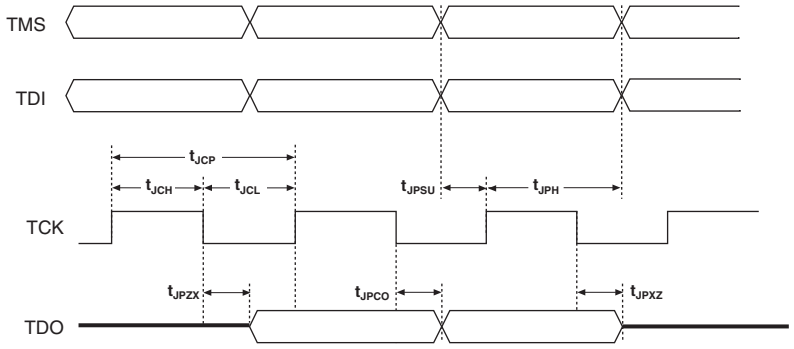
BSDL files for IEEE Std. 1149.1-compliant HardCopy III devices can also be generated using the Quartus software version 8.1 or later. Visit the Altera website at www.altera.com for the procedure to generate the BSDL files using the Quartus II software.

For more information about BSDL files for IEEE Std. 1149.1-compliant HardCopy III devices and the BSDL Customizer script, visit the Altera website at www.altera.com.

JTAG Timing

Figure 10–1 shows the JTAG timing waveforms for the HardCopy III devices.

Figure 10–1. JTAG Timing Waveforms for HardCopy III Devices



For JTAG timing parameters and values, refer to the *DC and Switching Characteristics of HardCopy III Devices* chapter in volume 3 of the *HardCopy III Device Handbook*.

Document Revision History

Table 10–4 shows the revision history for this document.

Table 10–4. Document Revision History

Date	Version	Changes
January 2011	3.1	Updated for Quartus II software 10.1.
June 2009	3.0	■ Updated Table 10–2 and Table 10–3.
December 2008	2.0	■ Updated Table 10–3. ■ Minor editorial changes made.
May 2008	1.0	Initial release.