8. High-Speed Differential I/O Interfaces and DPA in HardCopy III Devices

HIII51008-3.2

The HardCopy® III device family offers up to 1.25-Gbps differential I/O capabilities to support source-synchronous communication protocols such as Utopia, RapidIO®, XSBI, SGMII, SFI, and SPI. HardCopy III and Stratix® III devices have identical circuitry for high-speed differential I/O interfaces and dynamic phase alignment (DPA). HardCopy III high-speed I/Os support the same I/O standards and implementation guidelines as Stratix III devices. You can prototype high-speed interfaces with Stratix III devices and map the design to HardCopy III devices.

Because of differences in resource availability, you must set the **HardCopy III companion device** option in the Quartus® II software to map your Stratix III project to a HardCopy III device.

HardCopy III devices have the same dedicated circuitry as Stratix III devices for high-speed differential I/O support:

- Differential I/O buffer
- Transmitter serializer
- Receiver deserializer
- Data realignment
- DPA
- Synchronizer (FIFO buffer)
- Analog phase-locked looks (PLLs) located on the left and right sides of the device

For high-speed differential interfaces, HardCopy III devices support the following differential I/O standards:

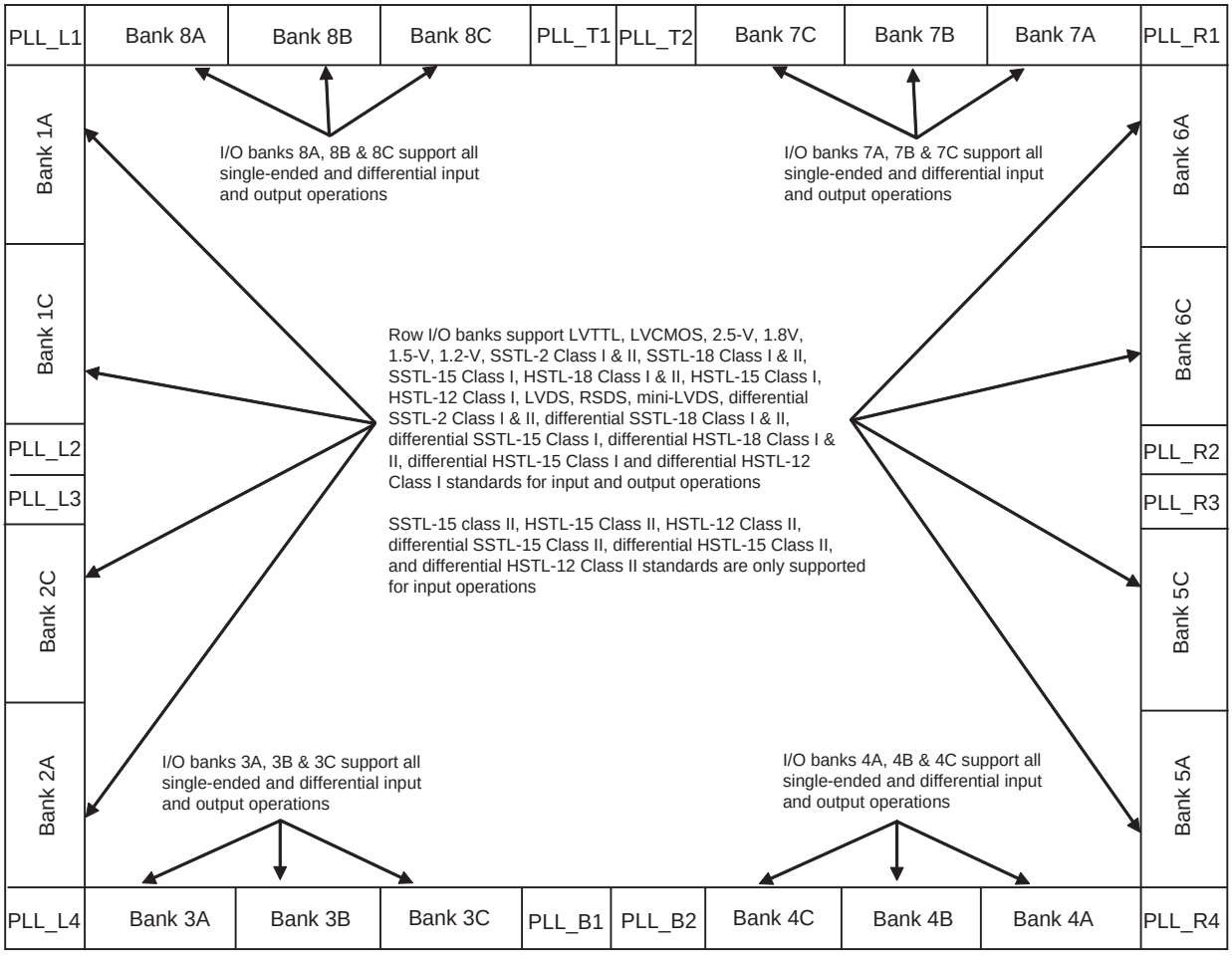
- Low voltage differential signaling (LVDS)
- Mini-LVDS
- Reduced swing differential signaling (RSDS)
- Differential HSTL
- Differential SSTL

You can use HSTL and SSTL I/O standards only for PLL clock inputs and outputs in differential mode.

I/O Banks

HardCopy III I/Os are divided into 12 to 20 I/O banks. The dedicated circuitry that supports high-speed differential I/Os is located in the left and right (row) I/O banks of the device. Figure 8–1 shows the different banks and the I/O standards supported by the banks.

Figure 8–1. I/O Banks in HardCopy III Devices *(Note 1), (2), (3), (4), (5), (6)*



Notes to Figure 8–1:

(1) The 1152- and 1517-pin packages have 20 I/O banks. The 780-pin package has 16 I/O banks. The 484-pin package has 12 I/O banks.

(2) Figure 8–1 is a top view of the silicon die that corresponds to a reverse view for flip-chip packages. It is a graphical representation only. For exact locations, refer to the pin list and Quartus II software.

(3) Differential HSTL and SSTL I/Os use two single-ended outputs with the second output programmed as inverted for the transmitter and uses a true SSTL/HSTL differential input buffer for the receiver.

(4) Top and bottom I/O differential HSTL and SSTL inputs use LVDS differential input buffers without on-chip differential termination support.

(5) Top and bottom I/O supports LVDS outputs using single-ended buffers and external resistor networks.

(6) The PLL blocks are shown for location purposes only and are not considered additional banks. The PLL input and output uses the I/Os in adjacent banks.

LVDS Channels

HardCopy III devices support LVDS on both row I/O banks and column I/O banks. There are true LVDS input and output buffers on row I/O banks. On column I/O banks, there are true LVDS input buffers but neither true LVDS output buffers nor dedicated high-speed circuitry. However, you can configure all column user I/Os, including I/Os with true LVDS input buffers, as emulated LVDS output buffers. Table 8–1 lists the LVDS channels supported in HardCopy III device row I/O banks.

Table 8–1. LVDS Channels Supported in HardCopy III Device Left and Right (Row) I/O Banks *(Note 1)*, *(2)*, *(3)*

HardCopy III Device	484 - Pin FineLine BGA	780 - Pin FineLine BGA	1152-Pin FineLine BGA	1517-Pin FineLine BGA *(4)*
HC325W	48Rx + 48Tx	48Rx + 48Tx	—	—
HC325F	48Rx + 48Tx	56Rx + 56Tx	—	—
HC335L	—	—	88Rx + 88Tx	88Rx + 88Tx *(5)*
HC335F	—	—	88Rx + 88Tx	88Rx + 88Tx *(5)*

Notes to Table 8–1:

(1) The LVDS channel count does not include dedicated clock input pins.

(2) The HardCopy III device family does not offer a 1760-pin package.

(3) Rx = true LVDS input buffers with OCT RD, Tx = true LVDS output buffers, and eTx = emulated LVDS output buffers (either LVDS_E_1R or LVDS_E_3R).

(4) The HardCopy III device family does not offer a 1517-pin package for Stratix III EP3SL110 and EP3SL150 prototype devices.

(5) Stratix III devices EP3SL340F1517 and EP3SE260F1517 offer 112Rx + 112Tx or 224eTx channels, and thus have more transceiver channels than HardCopy III devices.

Table 8–2 lists the LVDS channels supported in HardCopy III device column I/O banks.

Table 8–2. LVDS Channels Supported in HardCopy III Device Top and Bottom (Column) I/O Banks *(Note 1)*, *(2)*, *(3)* (Part 1 of 2)

HardCopy III Device	484 - Pin FineLine BGA	780 - Pin FineLine BGA	1152-Pin FineLine BGA	1517-Pin FineLine BGA
HC325W	24Rx + 24eTx or 48eTx	48Rx + 48eTx or 96eTx	—	—
HC325F	24Rx + 24eTx or 48eTx	64Rx + 64eTx or 128eTx	—	—
HC335L	—	—	96Rx + 96eTx or 192eTx	128Rx + 128eTx or 256eTx *(4)*

Table 8–2. LVDS Channels Supported in HardCopy III Device Top and Bottom (Column) I/O Banks *(Note 1)*, *(2)*, *(3)* (Part 2 of 2)

HardCopy III Device	484 - Pin FineLine BGA	780 - Pin FineLine BGA	1152-Pin FineLine BGA	1517-Pin FineLine BGA
HC335F	—	—	96Rx + 96eTx or 192eTx	128Rx + 128eTx or 256eTx *(4)*

Notes to Table 8–2:

(1) The LVDS channel count does not include dedicated clock input pins.

(2) LVDS input buffers at top and bottom I/O banks are true LVDS input buffers. All user I/Os, including I/Os with true LVDS input buffers, can be configured as emulated LVDS output buffers.

(3) Rx = true LVDS input buffers with OCT RD, Tx = true LVDS output buffers, and eTx = emulated LVDS output buffers (either LVDS_E_1R or LVDS_E_3R).

(4) The HardCopy III device family does not offer a 1517-pin package for Stratix III EP3SL110 and EP3SL150 prototype devices.

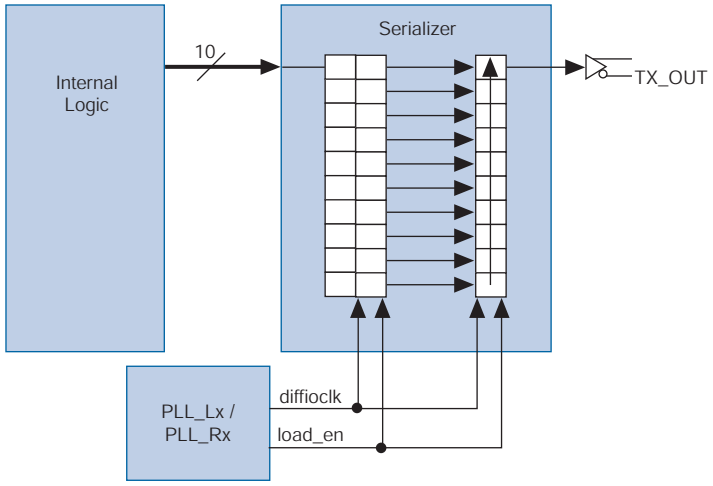
For more information about high-speed differential I/O interfaces and DPA, refer to "Design Recommendations" on page 8–22 and "Differences Between Stratix III and HardCopy III Devices" on page 8–23.

Differential Transmitter

The HardCopy III transmitter has dedicated circuitry to provide support for LVDS signaling. The dedicated circuitry consists of a differential buffer, a serializer, and a shared analog PLL (left or right PLL). The differential buffer can drive out LVDS, mini-LVDS, and RSDS signaling levels. The serializer takes up to 10 bits-wide parallel data from the FPGA core, clocks it into the load registers, and serializes it using shift registers clocked by the left or right PLL before sending the data to the differential buffer. The MSB of the parallel data is transmitted first.

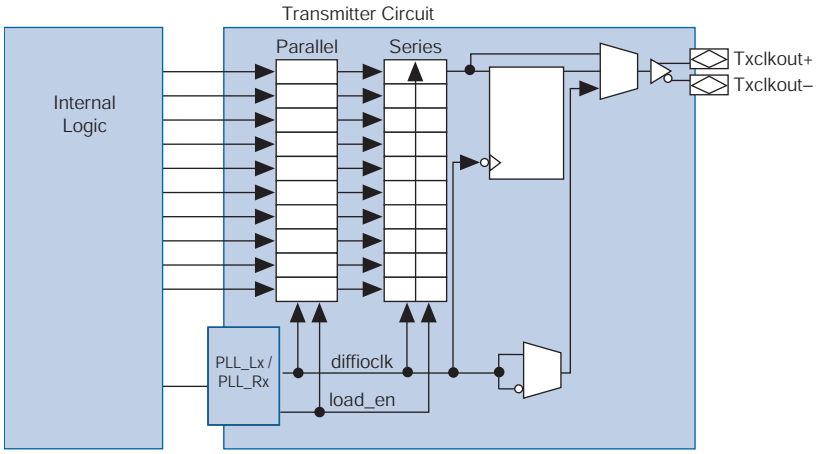
The load and shift registers are clocked by the load enable (`load_en`) signal and the `diffioclk` (clock running at serial data rate) signal generated from `PLL_Lx` (left PLL) or `PLL_Rx` (right PLL). You can statically set the serialization factor to ×4, ×6, ×7, ×8, or ×10 by using the Quartus II software. The load enable signal is derived from the serialization factor setting. Figure 8–2 is a block diagram of the HardCopy III transmitter.

Figure 8–2. Transmitter for HardCopy III Devices



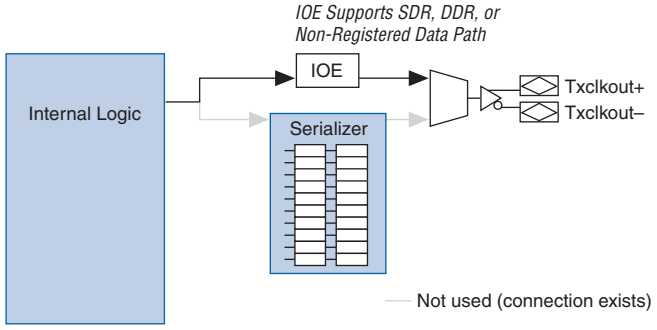
You can configure the HardCopy III transmitter data channel to generate a source synchronous transmitter clock output, allowing you to place the output clock near the data outputs to simplify board layout and reduce clock-to-data skew. Different applications often require specific clock-to-data alignments or specific data rate to clock rate factors. The transmitter can output a clock signal at the same rate as the data. Depending on the serialization factor, the output clock can also be divided by a factor of 2, 4, 8, or 10. You can set the phase of the clock in relation to the data at 0° or 180° (edge or center aligned). The left and right PLLs (PLL_Lx and PLL_Rx) provide additional support for other phase shifts in 45° increments. These settings are made statically in the Quartus II MegaWizard™ Plug-In Manager. Figure 8–3 shows the HardCopy III transmitter in clock output mode.

Figure 8–3. Transmitter in Clock Output Mode for HardCopy III Devices



You can bypass the HardCopy III serializer to support double data rate (DDR) (×2) and single data rate (SDR) (×1) operations to achieve a serialization factor of 2 and 1, respectively. The I/O element (IOE) contains two data output registers that can each operate in either DDR or SDR mode. The clock source for the registers in the IOE can come from any routing resource, from the left or right PLL (PLL_Lx/PLL_Rx), or from the top or bottom (PLL_Tx/PLL_Bx) PLL. Figure 8–4 shows the serializer bypass path.

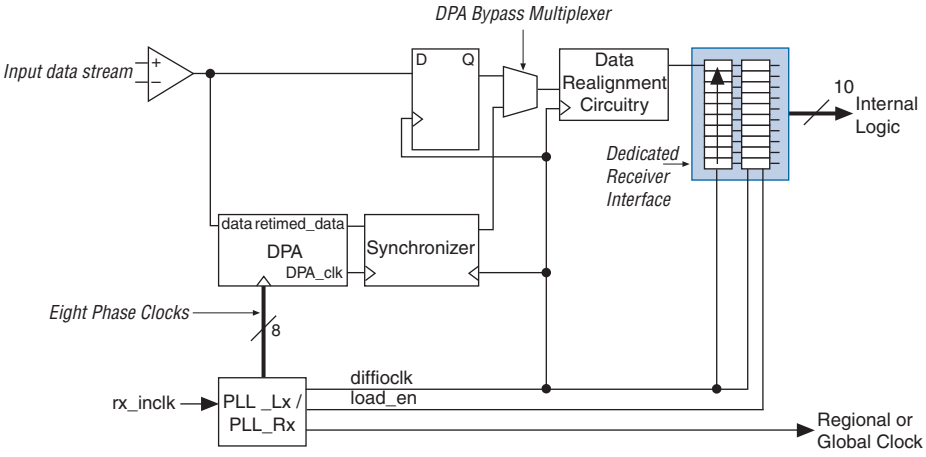
Figure 8–4. Serializer Bypass for HardCopy III Devices



Differential Receiver

HardCopy III devices have dedicated circuitry for receiving high-speed differential signals. Figure 8–5 shows a HardCopy III receiver block diagram. The receiver has a differential buffer, a shared PLL_Lx/PLL_Rx, DPA, synchronization FIFO buffer, data realignment block, and a deserializer. The differential buffer can receive LVDS, mini-LVDS, and RSDS signal levels, which are statically set in the Quartus II software Assignment Editor. The PLL receives the external source clock input that is transmitted with the data and generates different phases of the same clock. The DPA block chooses one of the clocks from the left or right PLL and aligns the incoming data on each channel.

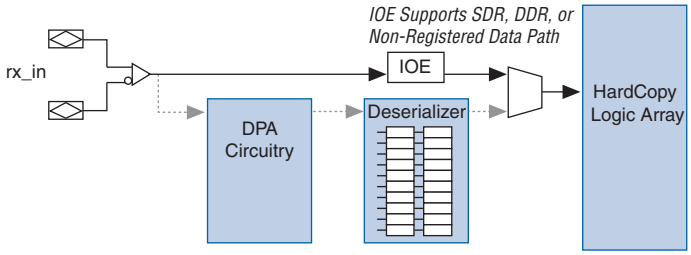
Figure 8–5. Receiver Block Diagram for HardCopy III Devices



The synchronizer circuit is a 1-bit wide by 6-bit deep FIFO buffer that compensates for any phase difference between the DPA clock and the data realignment block. If necessary, the data realignment circuit inserts a single bit of latency in the serial bit stream to align to the word boundary. The deserializer includes shift registers and parallel load registers and sends a maximum of 10 bits to the internal logic. The data path in the HardCopy III receiver is clocked by either a `diffioclk` signal or the DPA recovered clock. You can statically set the deserialization factor to 4, 6, 7, 8, or 10 by using the Quartus II software. The left or right PLLs (`PLL_Lx`/`PLL_Rx`) generate the load enable signal, which is derived from the deserialization factor setting.

You can bypass the HardCopy III deserializer in the Quartus II MegaWizard Plug-In Manager to support DDR (×2) or SDR (×1) operations. You cannot use the DPA and the data realignment circuit when you bypass the deserializer. The IOE contains two data input registers that can operate in DDR or SDR mode. The clock source for the registers in the IOE can come from any routing resource, from the left or right PLLs, or from the top or bottom PLLs. Figure 8–6 shows the deserializer bypass data path.

Figure 8–6. Deserializer Bypass



Receiver Data Realignment Circuit (Bit Slip)

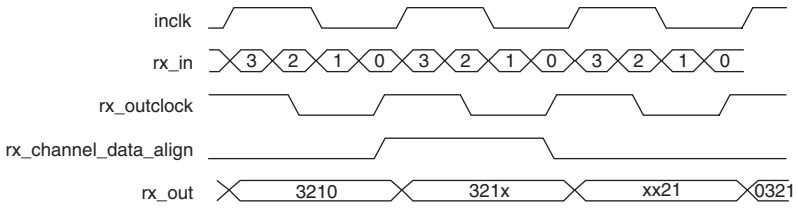
Skew in the transmitted data, along with skew added by the link, causes channel-to-channel skew on the received serial data streams. If the DPA is enabled, the received data is captured with different clock phases on each channel. This may cause the received data to be misaligned from channel to channel. To compensate for this channel-to-channel skew and establish the correct received word boundary at each channel, each receiver channel has a dedicated data realignment circuit that realigns the data by inserting bit latencies into the serial stream.

An optional `RX_CHANNEL_DATA_ALIGN` port controls the bit insertion of each receiver independently controlled from the internal logic. The data slips one bit for every pulse on `RX_CHANNEL_DATA_ALIGN`. The following conditions are required for the `RX_CHANNEL_DATA_ALIGN` signal:

- The minimum pulse width is one period of the parallel clock in the logic array
- The minimum low time between pulses is one period of the parallel clock
- There is no maximum high or low time
- Valid data is available two parallel clock cycles after the rising edge of `RX_CHANNEL_DATA_ALIGN`

Figure 8–7 shows the receiver output (rx_out) after one bit slip pulse with the serialization factor set to 4.

Figure 8–7. Data Realignment Timing

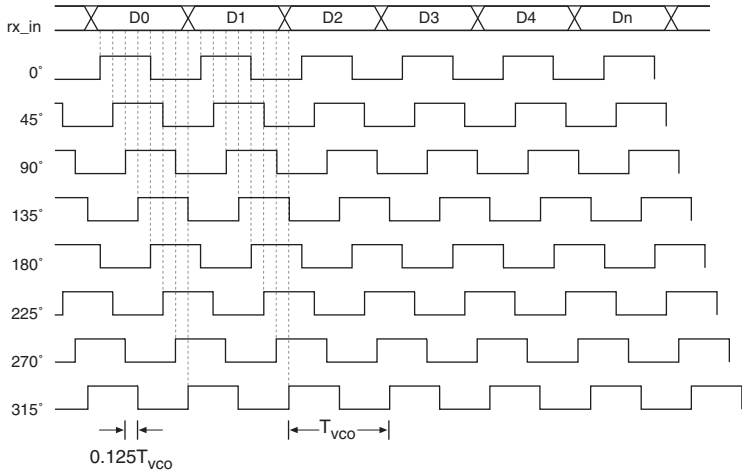


The data realignment circuit can have up to 11 bit-times of insertion before a rollover occurs. The bit rollover point can be from 1 to 11 bit-times, independent of the deserialization factor. An optional status port, rx_cda_max, is available to the FPGA from each channel to indicate when the preset rollover point is reached.

Dynamic Phase Aligner

The dynamic phase aligner (DPA) block takes in high-speed serial data from the differential input buffer and selects one of the eight phase clocks from the left or right PLL to sample the data. The DPA chooses a phase closest to the phase of the serial data. The maximum phase offset between the received data and the selected phase is 1/8 unit interval (UI), which is the maximum quantization error of the DPA. The eight phases of the clock are equally divided, giving a 45° resolution. Figure 8–8 shows the possible phase relationships between the DPA clocks and the incoming serial data.

Figure 8–8. DPA Clock Phase to Serial Data Timing Relationship



The DPA block continuously monitors the phase of the incoming serial data and selects a new clock phase if required. You can prevent the DPA from selecting a new clock phase by asserting the optional rx_dpll_hold port, which is available for each channel.

The DPA block requires a training pattern and a training sequence of at least 256 repetitions. The training pattern is not fixed, so you can use any training pattern with at least one transition on each channel. An optional output port (rx_dpa_locked) is available to the internal logic to indicate when the DPA block has settled on the closest phase to the incoming data phase. The DPA block de-asserts rx_dpa_locked depending on the option selected in the Quartus II MegaWizard Plug-In Manager, when either a new phase is selected, or when the DPA has moved two phases in the same direction. The rx_dpa_locked signal is synchronized to the DPA clock domain and should be considered as the initial indicator for the lock condition. Use data checkers to validate the data integrity.

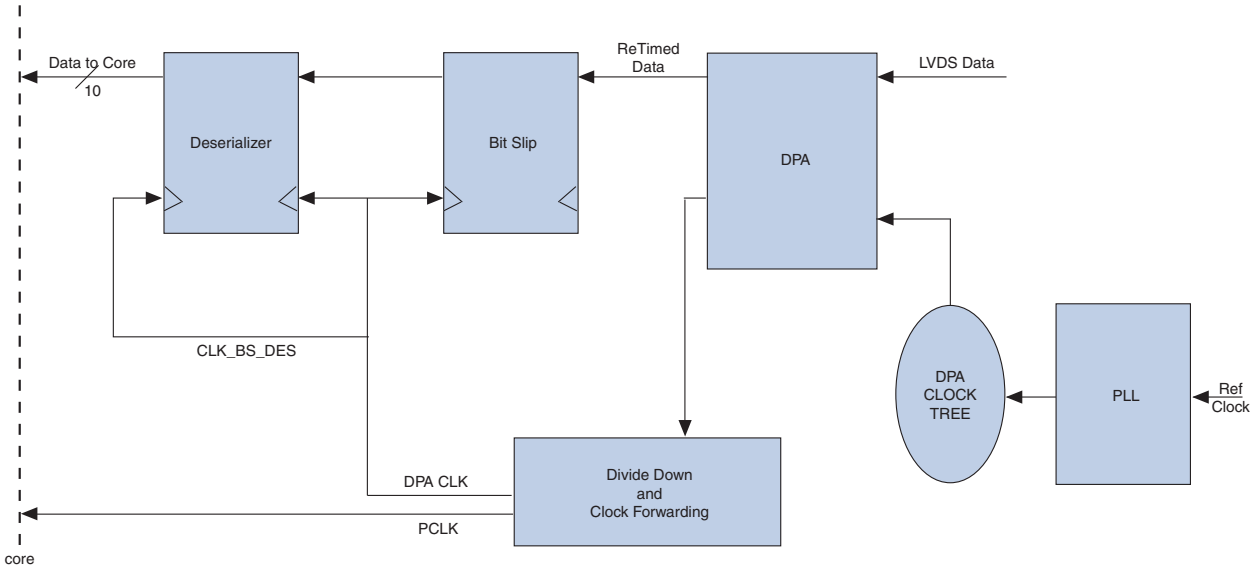
An independent reset port (rx_reset) is available to reset the DPA circuitry. The DPA circuitry must be retrained after reset.

Soft-CDR Mode

The HardCopy III LVDS channel offers soft-CDR mode to support the Gigabit Ethernet/SGMII protocols. Clock-data recovery (CDR) is required to extract the clock out of the clock-embedded data to support SGMII. In HardCopy III devices, the CDR circuit is implemented in HCells.

In soft-CDR mode, the DPA circuitry selects an optimal DPA clock phase to sample the data and carry on the bit-slip operation and deserialization. The selected DPA clock is also divided down by the deserialization factor and then forwarded to the PLD core along with the de-serialized data. The LVDS block has an output called divclkout for the forwarded clock signal. This signal is put on the periphery clock network. In HardCopy III devices, you can use every LVDS channel in soft-CDR mode and can drive the core using the periphery network. Figure 8–9 shows the path enabled in soft-CDR mode.

Figure 8–9. Soft-CDR Mode Data and Clock Path ***(Note 1)***



Note to Figure 8–9:

(1) The synchronizer FIFO is bypassed in soft-CDR mode. The reference clock frequency must be suitable for the PLL to generate a clock that matches the data rate of the interface. The DPA circuitry can track parts per million (PPM) differences between the reference clock and the data stream.

Synchronizer

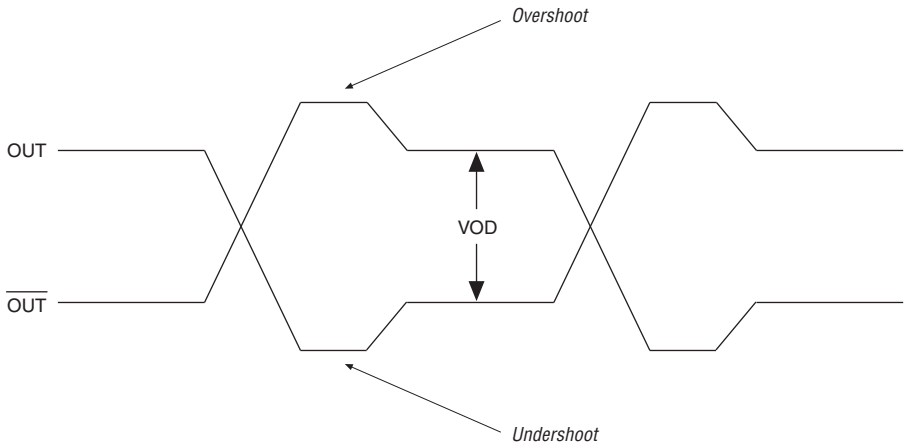
The synchronizer is a 1-bit × 6-bit deep FIFO buffer that compensates for the phase difference between the recovered clock from the DPA circuit and the `diffioclk` that clocks the rest of the logic in the receiver. The synchronizer can only compensate for phase differences, not frequency differences between the data and the receiver's `inclk`.

An optional port (`rx_fifo_reset`) is available to the internal logic to reset the synchronizer. The synchronizer is automatically reset when the DPA first locks to the incoming data. Altera recommends using `rx_fifo_reset` to reset the synchronizer when the DPA signals a loss-of-lock condition beyond the initial locking condition.

Pre-Emphasis and Output Differential Voltage

HardCopy III LVDS transmitters support four pre-emphasis and four output differential voltage (VOD) settings. Pre-emphasis increases the amplitude of the high frequency component of the output signal and helps compensate for the frequency dependent attenuation along the transmission line. Figure 8–10 shows an LVDS output with pre-emphasis. The overshoot is produced by pre-emphasis. This overshoot must not be included in the VOD voltage. The definition of VOD is also shown in Figure 8–10.

Figure 8–10. Output Differential Voltage



Pre-emphasis is an important feature for high-speed transmission. Without pre-emphasis, the output current is limited by the VOD setting and the output impedance of the driver. At high frequency, the slew rate might not be fast enough to reach the full VOD before the next edge, producing a pattern dependent jitter.

With pre-emphasis, the output current is boosted momentarily during switching to increase the output slew rate. The overshoot introduced by the extra current happens only during switching and does not ring, unlike the overshoot caused by signal reflection. The amount of pre-emphasis required depends on the attenuation of the high-frequency component along the transmission line.

You can adjust pre-emphasis in HardCopy III devices to create the right amount of overshoot at different transmission conditions. There are four settings for pre-emphasis: zero, low, medium, and high. The default setting is low. For a particular design, you can use simulation with an LVDS buffer and transmission line to determine the best pre-emphasis setting. You can also fix the VOD to any of the four settings: low, medium low, medium high, and high. The default setting is medium low.

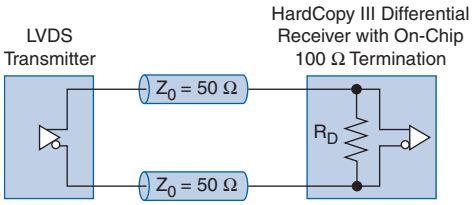
A re-compile is required for each new setting.

Differential I/O Termination

HardCopy III devices provide a 100-Ω, on-chip differential termination option on each differential receiver channel for LVDS standards. On-chip termination (OCT) saves board space by eliminating the need to add external resistors on the board. You can enable OCT in the Quartus II Assignment Editor.

On-chip differential termination is supported on all row I/O pins and serial/deserializer (SERDES) block clock pins: `clk[0,2,9,11]`. It is not supported for column I/O pins, high speed clock pins `clk[1,3,8,10]`, or the corner PLL clock inputs. Figure 8–11 shows device OCT.

Figure 8–11. On-Chip Differential OCT

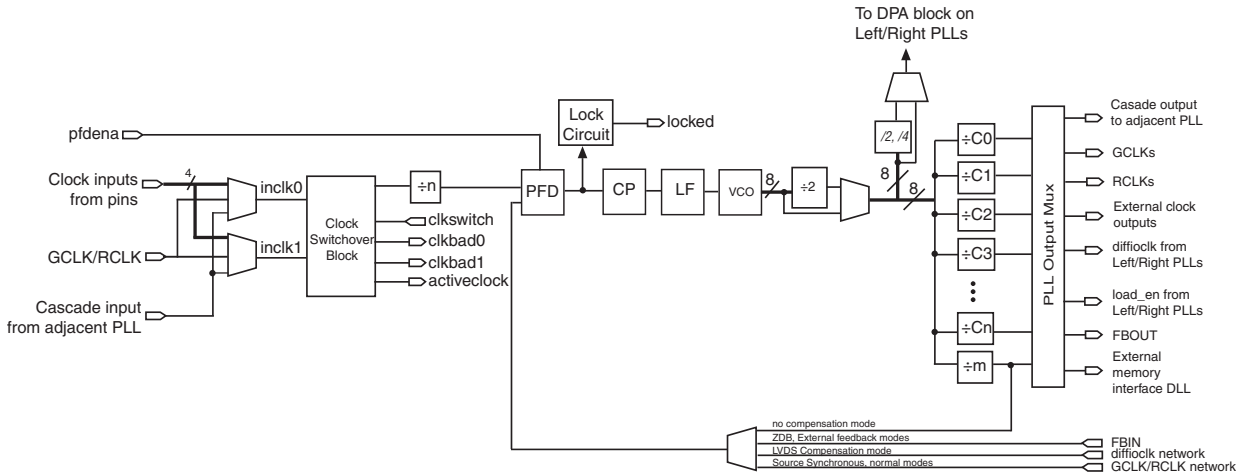


Left and Right PLLs (PLL_Lx and PLL_Rx)

HardCopy III devices contain a maximum of eight left or right PLLs with up to four PLLs located on the left side (`PLL_L1`, `PLL_L2`, `PLL_L3`, and `PLL_L4`) and four on the right side (`PLL_R1`, `PLL_R2`, `PLL_R3`, and `PLL_R4`) of the device. The left PLLs can support high-speed differential I/O banks on the left side; the right PLLs can support banks only on the right side of the device. The high-speed differential I/O receiver and transmitter channels use these left and right PLLs to generate the parallel clocks (`rx_outclock` and `tx_outclock`) and high-speed clocks (`diffioclk`). Figure 8–1 on page 8–2 show the locations of the left/right PLLs for HardCopy III devices. The PLL VCO operates at the clock frequency of the data rate. Each left or right PLL offers a single serial data rate support, but up to two separate serialization or deserialization factors (from the `C0` and `C1` of left or right PLL clock outputs), or both. Clock switchover and dynamic left and right PLL reconfiguration are available in high-speed differential I/O support mode.

Figure 8–12 shows a simplified diagram of the major components of a HardCopy III PLL.

Figure 8–12. PLL for HardCopy III Devices



Clocking

The left and right PLLs feed into the differential transmitter and receiver channels through the LVDS and DPA clock networks. Figure 8–13 and Figure 8–14 show the corner and center PLL clock in HardCopy III devices. Each left or right I/O bank consists of one LVDS clock network, for a total of four clock trees on the device. The center left and right PLLs can drive the LVDS clock network, therefore, clocking the transmitter and receiver channels above and below them. The corner left and right PLLs can drive the adjacent row-I/O banks only. For example, corner `PLL_L1` can drive the LVDS clock network only in I/O bank 1A and bank 1C. Therefore, with corner PLLs, each LVDS clock network can be driven by three PLLs: two center PLLs and one corner PLL. For HardCopy III devices without a corner PLL, each clock tree

can be driven by two center PLLs. Each clock network supports two full-duplex transceiver channels. However, Altera recommends sharing the `diffioclk` and `load_en` signals between the transmitting and the receiving channels in the same I/O bank whenever possible. For more information about PLL clocking restrictions, refer to "Differential Pin Placement Guidelines" on page 8–15.

Figure 8–13. LVDS/DPA Clocks in HardCopy III and Stratix III Devices with Center PLLs

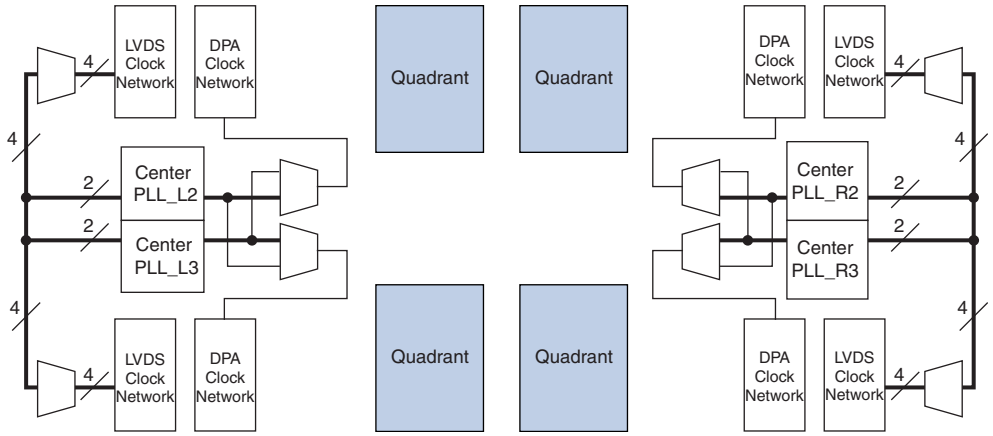
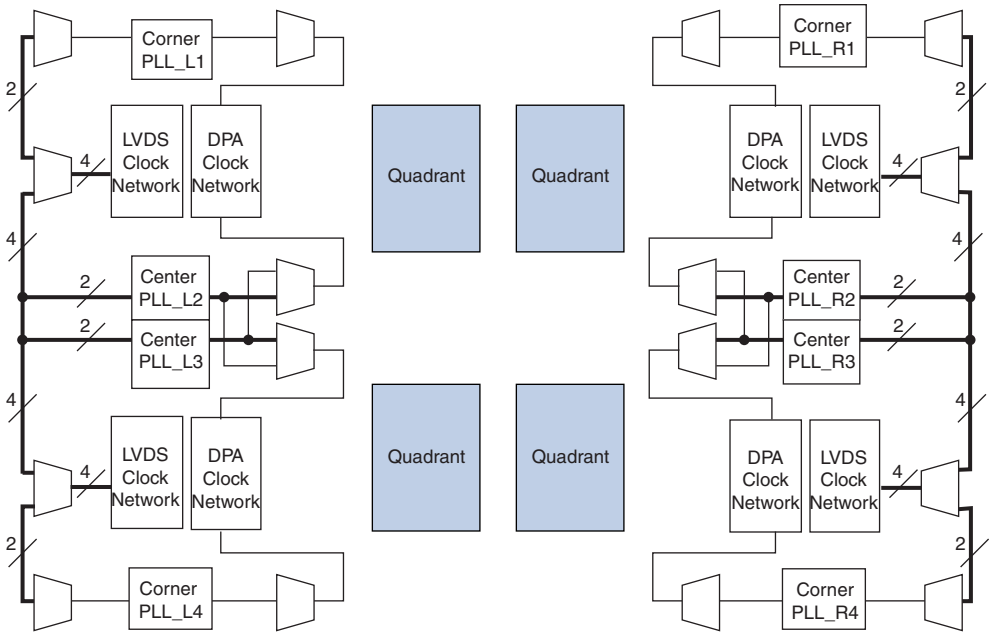


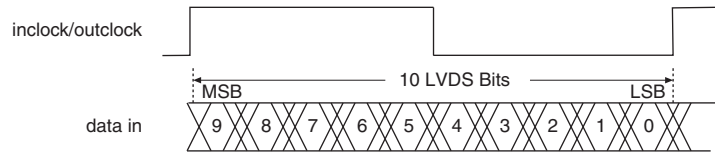
Figure 8–14. Clocks in HardCopy III and Stratix III Devices with Center and Corner PLLs



High-Speed Differential I/O Interfaces and DPA in HardCopy III Devices Differential Data Orientation

There is a set relationship between an external clock and the incoming data. For operation at 1 Gbps with a SERDES factor of 10, the external clock is multiplied by 10, and phase-alignment is set in the PLL to coincide with the sampling window of each data bit. The data is sampled on the falling edge of the multiplied clock. Figure 8–15 shows the data bit orientation of the ×10 mode.

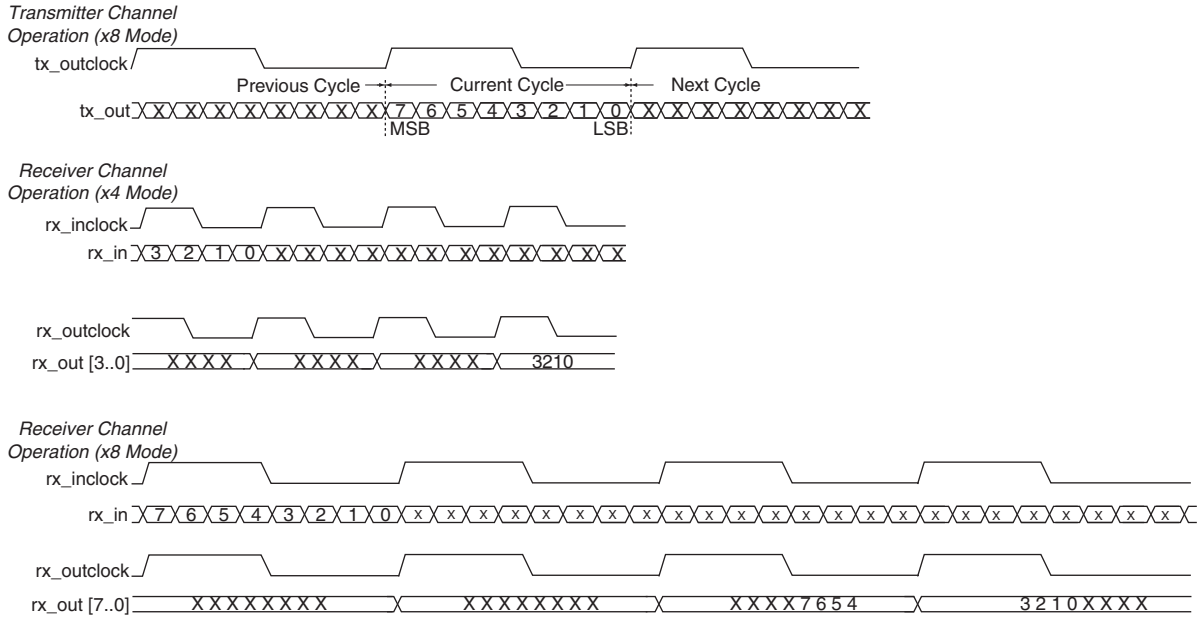
Figure 8–15. Bit Orientation in Quartus II Software Differential I/O Bit Position



Data synchronization is necessary for successful data transmission at high frequencies. Figure 8–16 shows the data bit orientation for a channel operation. This figure is based on the following:

- SERDES factor equals clock multiplication factor
- Edge alignment is selected for phase alignment
- Implemented in hard SERDES

Figure 8–16. Bit-Order and Word Boundary for One Differential Channel ***(Note 1)***



Note to Figure 8–16:

(1) These are only functional waveforms and are not intended to convey timing information.

For other serialization factors, use the Quartus II software tools and find the bit position within the word. The bit positions after deserialization are listed in Table 8–3.

Table 8–3 shows the conventions for differential bit naming for eight differential channels. The MSB and LSB positions increase with the number of channels used in a system.

Table 8–3. LVDS Channels Supported in HardCopy III Device Left and Right (Row) I/O Banks

Receiver Channel Number	Internal 8-Bit Parallel Data	
	MSB Position	LSB Position
1	7	0
2	15	8
3	23	16
4	31	24
5	39	32
6	47	40
7	55	48
8	63	56

Differential Pin Placement Guidelines

To ensure proper high-speed operation, differential pin placement guidelines have been established. Also, the Quartus II compiler automatically verifies these guidelines and issues an error message if they are not met.

Because DPA usage adds some constraints on the placement of high-speed differential channels, this section is divided into pin placement guidelines with and without DPA usage.

If you want to place both single-ended and differential I/Os in the same row or column I/O bank, refer to *the HardCopy III Device I/O Features* chapter.

Guidelines for DPA-Enabled Differential Channels

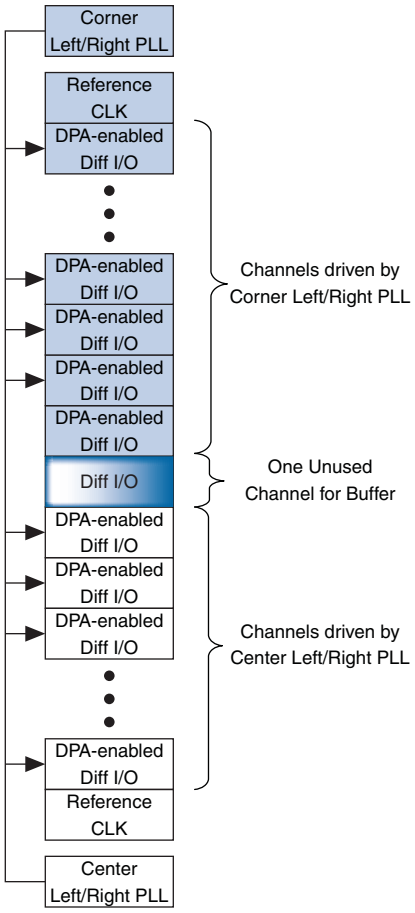
HardCopy III devices have differential receivers and transmitters in I/O banks on the left and right sides of the device. Each receiver has a dedicated DPA circuit to align the phase of the clock to the data phase of its associated channel. When you use DPA-enabled channels in differential banks, you must adhere to the guidelines listed in the following sections.

Using Corner and Center Left/Right PLLs

If a differential bank is being driven by two left or right PLLs, and the corner left or right PLL is driving one group and the center left or right PLL is driving another group, there must be at least one row of separation between the two groups of DPA-enabled channels (refer to Figure 8–17). The two groups can operate at independent frequencies.

No separation is necessary if a single left or right PLL is driving DPA-enabled channels as well as DPA-disabled channels.

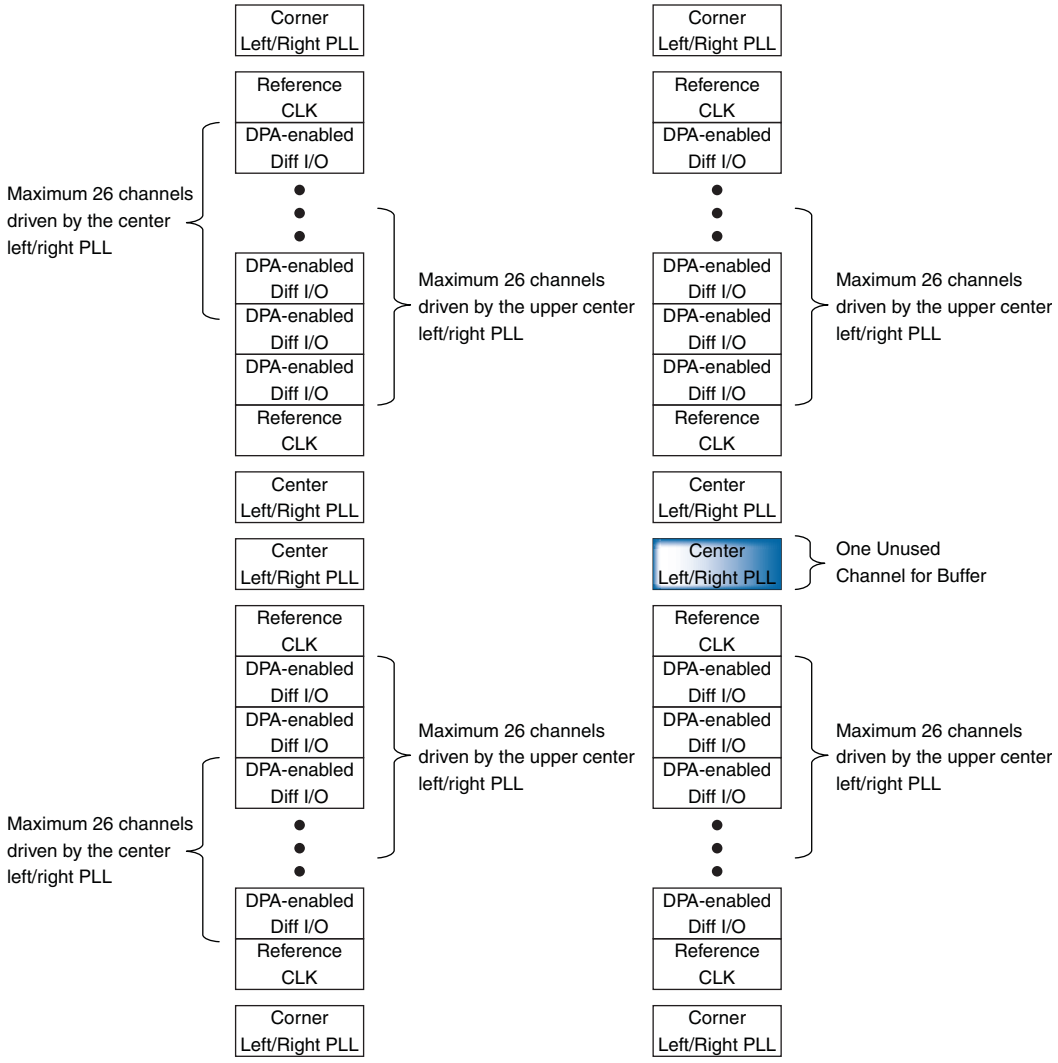
Figure 8–17. Corner and Center Left/Right PLLs Driving DPA-Enabled Differential I/Os in the Same Bank Using Both Center Left/Right PLLs



You can use center left or right PLLs to drive DPA-enabled channels simultaneously, as long as they drive these channels in their adjacent banks only, as shown in Figure 8–18.

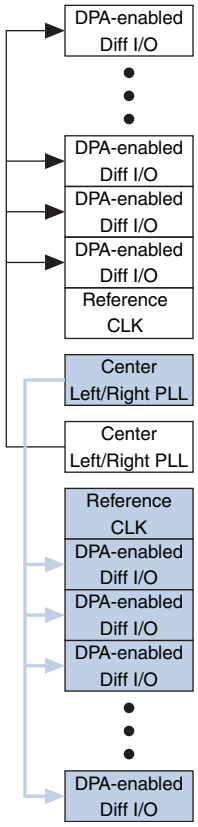
If one of the center left or right PLLs drives the top and bottom banks, you cannot use the other center left or right PLL to drive differential channels, as shown in Figure 8–18.

Figure 8–18. Center Left/Right PLLs Driving DPA-Enabled Differential I/Os



If the top PLL_L2/PLL_R2 drives the DPA-enabled channels in the lower differential bank, the PLL_L3/PLL_R3 cannot drive the DPA-enabled channels in the upper differential banks and vice versa. In other words, the center left or right PLLs cannot drive cross-banks simultaneously, as shown in Figure 8–19.

Figure 8–19. Invalid Placement of DPA-Enabled Differential I/Os Driven by Both Center Left/Right PLLs



Guidelines for DPA-Disabled Differential Channels

When you use DPA-disabled channels in the left and right banks of a HardCopy III device, you must adhere to the guidelines in the following sections.

DPA-Disabled Channel Driving Distance

Each left or right PLL can drive all the DPA-disabled channels in the entire bank.

Using Corner and Center Left and Right PLLs

The following guidelines show how you can use corner and center left and right PLLs:

- You can use a corner left or right PLL (PLL_L1, PLL_L4, PLL_R1, and PLL_R4) to drive all the transmitter channels and a center left or right PLL (PLL_L2, PLL_L3, PLL_R2, and PLL_R3) to drive all DPA-disabled receiver channels within the same differential bank. A transmitter channel and a receiver channel in the same LAB row can be driven by two different PLLs, as shown in Figure 8–20.

- A corner left or right PLL and a center left or right PLL can drive duplex channels in the same differential bank as long as the channels driven by each PLL are not interleaved. No separation is necessary between the group of channels driven by the corner and center left or right PLLs. Refer to Figure 8–20 and Figure 8–21.

Figure 8–20. Corner and Center Left and Right PLLs Driving DPA-Disabled Differential I/Os in the Same Bank

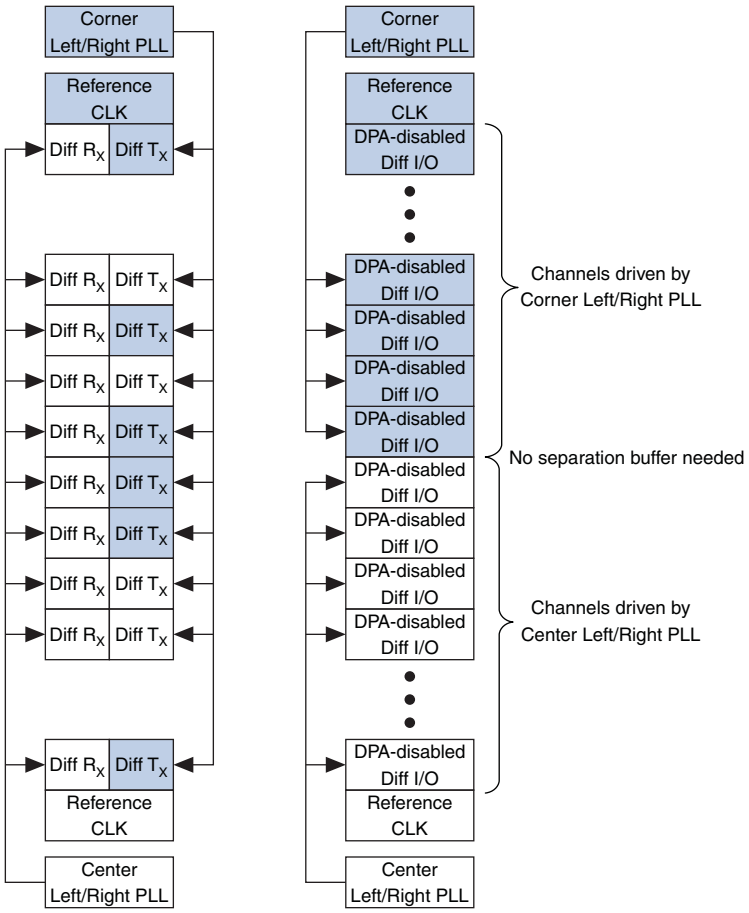
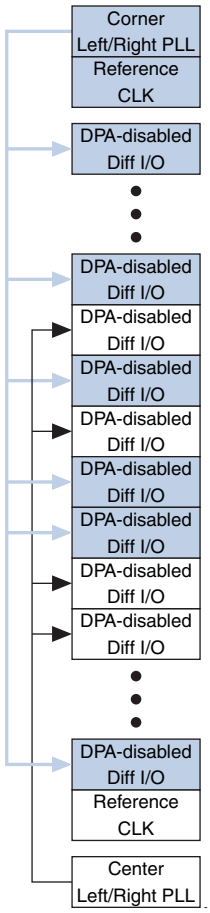


Figure 8–21. Invalid Placement of DPA-Disabled Differential I/Os Due to Interleaving of Channels Driven by the Corner and Center Left and Right PLLs



Using Both Center Left and Right PLLs

You can use both center left and right PLLs simultaneously to drive DPA-disabled channels on upper and lower differential banks, as shown in Figure 8–22. Unlike DPA-enabled channels, the center left and right PLLs can drive cross-banks. For example, the upper center left or right PLL can drive the lower differential bank while the lower center left or right PLL is driving the upper differential bank and vice versa, as shown in Figure 8–23.

Figure 8–22. Both Center Left and Right PLLs Simultaneously Driving DPA-Disabled Upper and Lower Bank Channels

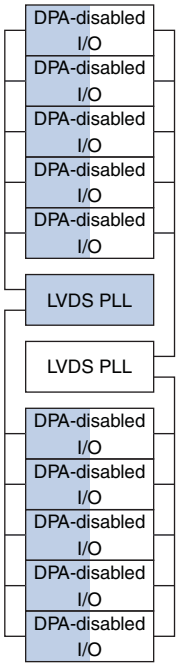
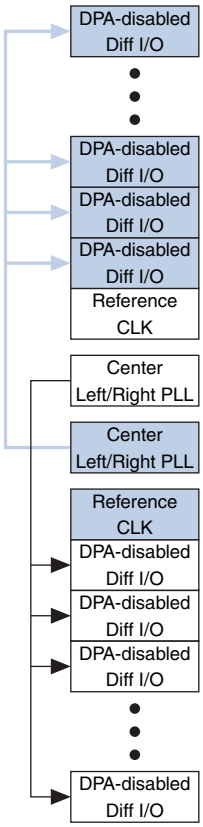


Figure 8–23. Both Center Left/Right PLLs Driving Cross-Bank DPA-Disabled Channels Simultaneously



Design Recommendations

To implement the high-speed differential interface successfully, Altera recommends following these design guidelines:

1. Altera provides HardCopy III IBIS models to verify I/O timing and characteristics. Altera strongly recommends verifying the I/O interfaces with simulation before you submit the design to the HardCopy Design Center.

For more information about signal integrity simulations with third-party tools, refer to the *Signal Integrity Analysis with Third-Party Tools* chapter in volume 3 of the *Quartus II Handbook*.

2. You can use center PLLs for both Tx and Rx, but corner PLLs are preferred for Tx applications over Rx applications.
3. Altera recommends sharing the `lvdsclk` and `load_en` signals between transmitting and receiving channels in the same I/O bank whenever possible.

Differences Between Stratix III and HardCopy III Devices

The HardCopy III device family supports full high-speed differential I/O and DPA mapping from the Stratix III family. Both families are designed with identical dedicated circuitry and thus support the same I/O standard, implementation guidelines, and performance. Table 8–4 shows the LVDS channels supported in Stratix III and HardCopy III devices.

Table 8–4. LVDS Channels Supported in Stratix III and HardCopy III Devices *(Note 1), (2)*

HardCopy III Device	Package *(3)*	LVDS Channels	Stratix III Devices	Package	LVDS Channels
HC325W	F484	48Rx + 48Tx	EP3SL150	F780	56Rx + 56Tx
HC325F			EP3SE110		
HC325W	F780		EP3SL200	H780	
HC325F		56Rx + 56Tx	EP3SE260		
HC335L	F1152	88Rx + 88Tx	EP3SL150	F1152	88Rx + 88Tx
			EP3SL200		
HC335F			EP3SE110		
			EP3SE260		
			EP3SL340	H1152	
HC335L	F1517	88Rx + 88Tx	EP3SL200	F1517	112Rx + 112Tx
HC335F			EP3SL340		
			EP3SE260		

Notes to Table 8–4:

(1) The HardCopy III family does not offer a 1760-pin package.

(2) LVDS channels supported in HardCopy III and Stratix III devices left and right (row) I/O banks.

(3) There is no socket-replacement to the F484-package HardCopy from the F780-package FPGA.

Document Revision History

Table 8–5 lists the revision history for this chapter.

Table 8–5. Document Revision History

Date	Version	Changes
January 2011	3.2	■ Removed the note before Table 8–1. ■ Updated Table 8–1, Table 8–2, and Table 8–4. ■ Updated the "Pre-Emphasis and Output Differential Voltage" section. ■ Minor text edits.
January 2010	3.1	■ Updated Table 8–1 and Table 8–3. ■ Minor text edits.
June 2009	3.0	Updated tables for device part number updates.
December 2008	2.0	Made minor editorial changes.
May 2008	1.0	Initial release.