5. Clock Networks and PLLs in HardCopy III Devices

HIII51005-3.1

This chapter provides a general description of clock networks and phase-locked loops (PLLs) in HardCopy® III devices.

HardCopy III devices support a hierarchical clock structure and multiple PLLs with advanced features equivalent to Stratix® III devices. The large number of clocking resources in combination with clock synthesis precision offered by the PLLs provides a complete clock management solution for your designs. HardCopy III devices provide dedicated global clock networks (GCLKs), regional clock networks (RCLKs), and periphery clock networks (PCLKs). These clocks are organized into a hierarchical clock structure that provides up to 192 unique clock domains for the entire device, and up to 60 unique clock sources per device quadrant. Altera's Quartus® II software compiler automatically turns off clock networks not used in the design, thereby reducing overall power consumption of the device.

HardCopy III devices deliver abundant PLL resources with up to 12 PLLs per device and up to 10 outputs per PLL. These PLLs are feature rich, supporting advanced capabilities such as clock switchover, dynamic phase shifting, PLL reconfiguration, and reconfigurable bandwidth. HardCopy III PLLs also support external feedback mode, spread-spectrum tracking, and post-scale counter cascading features. The Quartus II software enables the PLLs and their features without requiring any external devices.

All Stratix III PLL features are supported by HardCopy III PLLs.

For detailed information about clock networks and PLLs, refer to the *Clock Networks and PLLs in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*.

Clock Networks in HardCopy III Devices

HardCopy III devices offer the same clock network resources and features as Stratix III devices. Clock resources that are used in Stratix III devices are mapped to equivalent clock resources in HardCopy III devices, preserving the clocking functions. Unused clock resources are powered down to reduce power consumption.

Clock Network Resources

Similar to Stratix III devices, HardCopy III devices have up to 32 dedicated single-ended clock pins or 16 dedicated differential clock pins (`CLK[0:15]p` and `CLK[0:15]n`) that can drive either the GCLK or RCLK networks. These clock pins are arranged in the middle of the four sides of the HardCopy III device.

You can drive the 16 GCLKs in HardCopy III devices throughout the entire device, serving as low-skew clock sources for the core fabric and PLLs. You can also drive the GCLKs from the device I/O elements (IOEs) and internal logic to generate global clocks and other high fan-out control signals.

The RCLKs provide the lowest clock delay and skew for logic contained within a single device quadrant. You can drive RCLKs from IOEs and internal logic within a given quadrant.

The PCLKs are a collection of individual clock networks driven from the periphery of the HardCopy III device. Clock outputs from the dynamic phase alignment (DPA) block, horizontal I/O pins, and internal logic can drive the PCLK networks. These PCLKs have higher skew when compared with the GCLK and RCLK networks and can be used instead of general purpose routing to drive signals into and out of the HardCopy III device.

The GCLKs, RCLKs, and PCLKs available in HardCopy III devices are organized into hierarchical clock structures that provide up to 192 unique clock domains (16 GCLK + 88 RCLK + 88 PCLK) across the entire device. HardCopy III devices also allow up to 60 unique GCLK, RCLK, and PCLK clock sources (16 GCLK + 22 RCLK + 22 PCLK) per device quadrant.

Table 5–1 lists the clock resources available in HardCopy III devices.

Table 5–1. Clock Resources in HardCopy III Devices

Clock Resource	Number of Resources Available	Source of Clock Resource
Clock input pins	32 Single-ended (16 Differential)	`CLK[0..15]p` and `CLK[0..15]n` pins
Global clock networks	16	`CLK[0..15]p/n` pins, PLL clock outputs, and logic array
Regional clock networks	88	`CLK[0..15]p/n` pins, PLL clock outputs, and logic array
Peripheral clock networks	88 (22 per device quadrant) *(1)*	DPA clock outputs, horizontal I/O pins, and logic array
GCLKs/RCLKs per quadrant	38	16 GCLKs + 22 RCLKs
GCLKs/RCLKs per device	104	16 GCLKs + 88 RCLKs

Note to Table 5–1:

(1) There are 56 PCLKs in HC325 devices and 88 PCLKs in HC335 devices.

Clocking Regions

HardCopy III devices can implement the four different types of Stratix III clocking regions using GCLK and RCLK networks. These types of clocking regions include the following:

- Entire device clock region
- Regional clock region
- Dual-regional clock region
- Sub-regional clock region

Clock Control Block

HardCopy III devices also support the same features as the Stratix III clock control block, which is available for each GCKL and RCLK network. The clock control block provides the following features:

- Clock source selection (dynamic selection for GCLKs)

  You can statically or dynamically select the GCLK source. The RCLK source can only be statically selected. Static selection involves mask programming the clock multiplexer select inputs. The clock selection is fixed and cannot be changed when the HardCopy III device is in user mode. Dynamic selection for the GCLK source uses internal logic to control the clock multiplexer select inputs when the device is in user mode. For dynamic clock source selection, you can either select two PLL outputs (such as `CLK0` or `CLK1`) or a combination of clock pins or PLL outputs.

- Clock power-down (static or dynamic clock enable or disable)

  You can statically or dynamically power-down the GCLK and RCLK networks, reducing overall power consumption of the device. Unused GCLK and RCLK networks are powered down through static settings that are automatically generated by the Quartus II software and mask programmed into the device. The dynamic clock enable or disable feature allows internal logic to synchronously control power-up or power-down on GCLK and RCLK networks, including dual-regional clock regions.

PLLs in HardCopy III Devices

HardCopy III devices offer up to 12 PLLs that support the same features as the Stratix III PLLs. These PLLs provide robust clock management and synthesis for device clock management, external system clock management, and high-speed I/O interfaces. The nomenclature for the PLLs follows their geographical location in the device floorplan. The PLLs that reside on the top and bottom sides of the device are named PLL_T1, PLL_T2, PLL_B1, and PLL_B2

The PLLs that reside on the left and right sides of the device are named PLL_L1, PLL_L2, PLL_L3, PLL_L4, PLL_R1, PLL_R2, PLL_R3, and PLL_R4, respectively.

Table 5–2 lists the number of PLLs available in the HardCopy III device family.

Table 5–2. HardCopy III Device PLL Availability (Part 1 of 2)

HardCopy III Device	Stratix III Prototype Device	L1	L2	L3	L4	T1	T2	B1	B2	R1	R2	R3	R4
HC325WF484	EP3SL110--F780 *(1)*	—	✓	—	—	✓	—	✓	—	—	✓	—	—
	EP3SL150--F780 *(1)*	—	✓	—	—	✓	—	✓	—	—	✓	—	—
	EP3SE110--F780 *(1)*	—	✓	—	—	✓	—	✓	—	—	✓	—	—
	EP3SL200--H780 *(1)*	—	✓	—	—	✓	—	✓	—	—	✓	—	—
	EP3SE260--H780 *(1)*	—	✓	—	—	✓	—	✓	—	—	✓	—	—
	EP3SL340--H1152 *(1) (2)*	—	✓	(✓)	—	✓	(✓)	✓	(✓)	—	✓	(✓)	—
HC325FF484	EP3SL110--F780 *(1)*	—	✓	—	—	✓	✓	✓	—	—	✓	—	—
	EP3SL150--F780 *(1)*	—	✓	—	—	✓	✓	✓	—	—	✓	—	—
	EP3SE110--F780 *(1)*	—	✓	—	—	✓	✓	✓	—	—	✓	—	—
	EP3SL200--H780 *(1)*	—	✓	—	—	✓	✓	✓	—	—	✓	—	—
	EP3SE260--H780 *(1)*	—	✓	—	—	✓	✓	✓	—	—	✓	—	—
	EP3SL340--H1152 *(1) (2)*	—	✓	(✓)	—	✓	(✓)	✓	(✓)	—	✓	(✓)	—
HC325WF780	EP3SL110--F780	—	✓	—	—	✓	✓	✓	—	—	✓	—	—
	EP3SL150--F780	—	✓	—	—	✓	✓	✓	—	—	✓	—	—
	EP3SE110--F780	—	✓	—	—	✓	✓	✓	—	—	✓	—	—
	EP3SL200--H780	—	✓	—	—	✓	✓	✓	—	—	✓	—	—
	EP3SE260--H780	—	✓	—	—	✓	✓	✓	—	—	✓	—	—
	EP3SL340--H1152 *(1) (2)*	—	✓	(✓)	—	✓	(✓)	✓	(✓)	—	✓	(✓)	—
HC325FF780	EP3SL110--F780	—	✓	—	—	✓	✓	✓	—	—	✓	—	—
	EP3SL150--F780	—	✓	—	—	✓	✓	✓	—	—	✓	—	—
	EP3SE110--F780	—	✓	—	—	✓	✓	✓	—	—	✓	—	—
	EP3SL200--H780	—	✓	—	—	✓	✓	✓	—	—	✓	—	—
	EP3SE260--H780	—	✓	—	—	✓	✓	✓	—	—	✓	—	—
	EP3SL340--H1152 *(1) (2)*	—	✓	(✓)	—	✓	(✓)	✓	(✓)	—	✓	(✓)	—
HC335LF1152	EP3SL150--F1152	—	✓	✓	—	✓	✓	✓	✓	—	✓	✓	—
	EP3SE110--F1152	—	✓	✓	—	✓	✓	✓	✓	—	✓	✓	—
	EP3SL200--F1152	—	✓	✓	—	✓	✓	✓	✓	—	✓	✓	—
	EP3SE260--F1152	—	✓	✓	—	✓	✓	✓	✓	—	✓	✓	—
	EP3SL340--H1152	—	✓	✓	—	✓	✓	✓	✓	—	✓	✓	—

Table 5–2. HardCopy III Device PLL Availability (Part 2 of 2)

HardCopy III Device	Stratix III Prototype Device	L1	L2	L3	L4	T1	T2	B1	B2	R1	R2	R3	R4
HC335FF1152	EP3SL150--F1152	—	✓	✓	—	✓	✓	✓	✓	—	✓	✓	—
	EP3SE110--F1152	—	✓	✓	—	✓	✓	✓	✓	—	✓	✓	—
	EP3SL200--F1152	—	✓	✓	—	✓	✓	✓	✓	—	✓	✓	—
	EP3SE260--F1152	—	✓	✓	—	✓	✓	✓	✓	—	✓	✓	—
	EP3SL340--H1152	—	✓	✓	—	✓	✓	✓	✓	—	✓	✓	—
HC335LF1517	EP3SL200--F1517	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	EP3SE260--F1517	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	EP3SL340--F1517	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
HC335FF1517	EP3SL200--F1517	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	EP3SE260--F1517	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	EP3SL340--F1517	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

NOTE: to Table 5–2

(1) These are non-socket replacement devices. A board redesign is required.

(2) The HardCopy device has four PLLs, whereas the FPGA prototype device has eight PLLs. The additional PLLs available only in the FPGA prototype device are marked (✓).

The PLL functionality in HardCopy III devices remains the same as in Stratix III PLLs. Therefore, HardCopy III PLLs also support features such as PLL reconfiguration, where you can dynamically configure the PLL in user mode.

All HardCopy III PLLs have the same core analog structure with only minor differences in features that are supported. Table 5–3 lists the features of the top/bottom and left/right PLLs in HardCopy III devices.

For more information about Stratix III PLL features, refer to the *Clock Networks and PLLs in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*.

Table 5–3. HardCopy III PLL Features (Part 1 of 2)

Feature	HardCopy III Top/Bottom PLLs	HardCopy III Left/Right PLLs
C (output) counters	10	7
M, N, C counter sizes	1 to 512	1 to 512
Dedicated clock outputs	6 single-ended or 4 single-ended and 1 differential pair	2 single-ended or 1 differential pair
Clock input pins	8 single-ended or 4 differential pin pairs	8 single-ended or 4 differential pin pairs
External feedback input pin	Single-ended or differential	Single-ended only
Spread-spectrum input clock tracking	Yes *(1)*	Yes *(1)*
PLL cascading	Through GCLK and RCLK, and dedicated path between adjacent PLLs	Through GCLK and RCLK, and dedicated path between adjacent PLLs *(2)*
Compensation modes	All except LVDS clock network compensation	All except external feedback mode when using differential I/Os

Table 5–3. HardCopy III PLL Features (Part 2 of 2)

Feature	HardCopy III Top/Bottom PLLs	HardCopy III Left/Right PLLs
PLL drives LVDSCLK and LOADEN	No	Yes
VCO output drives DPA clock	No	Yes
Phase shift resolution	Down to 96.125ps *(3)*	Down to 96.125ps *(3)*
Programmable duty cycle	Yes	Yes
Output counter cascading	Yes	Yes
Input clock switchover	Yes	Yes

Notes to Table 5–3:

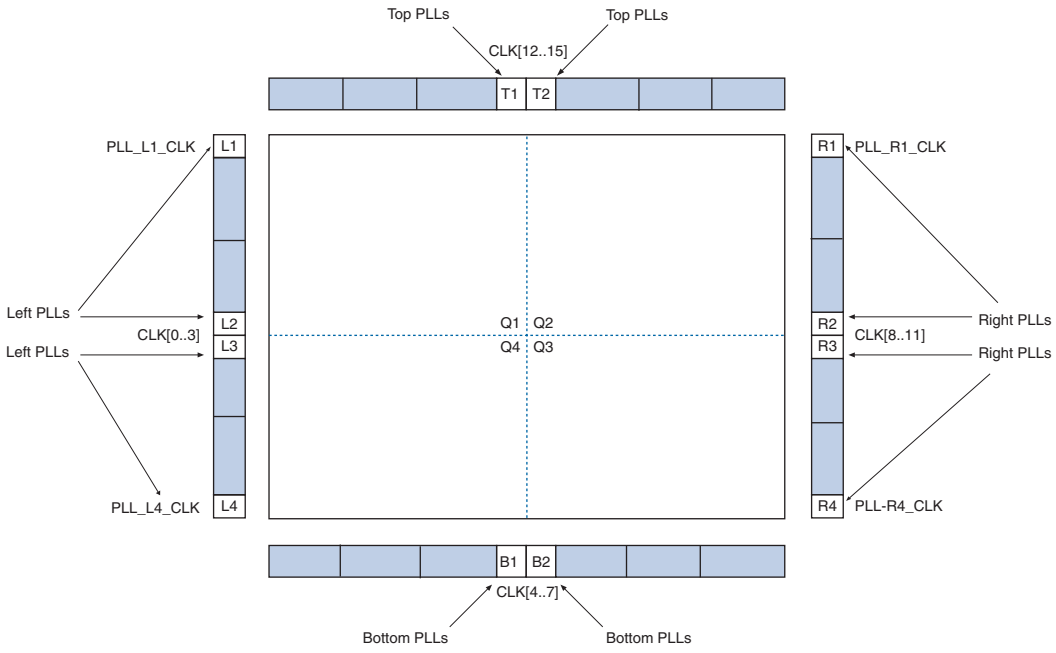
(1) Provided input clock jitter is within input jitter tolerance specifications.

(2) The dedicated path between adjacent PLLs is not available on L1, L4, R1, *and* R4 PLLs.

(3) The smallest phase shift is determined by the voltage-control oscillator (VCO) period divided by eight. For degree increments, the HardCopy III device can shift all output frequencies in increments of at least 45°. Smaller degree increments are possible depending on the frequency and divide parameters.

Figure 5–1 shows the PLL locations in HardCopy III devices. Some PLLs are not available depending on the density and package of the HardCopy III device.

Figure 5–1. HardCopy III PLL Locations



Design Considerations

To ensure that your Stratix III design can be successfully mapped to the HardCopy III design, follow these general guidelines when implementing your design. These guidelines help make your design robust, ensuring it meets timing closure and achieves the performance you need:

- Match the PLL resources used in HardCopy III devices and Stratix III devices in order to successfully map your design from the FPGA design to the ASIC design, or vice-versa. This is necessary to ensure that all the resources used and the functions implemented in both designs match. Make sure to select the companion device during device selection in the Quartus II software. Doing this restricts the Quartus II software to resources that are common to both the FPGA and ASIC devices, and ensures that the design can map successfully. Refer to Table 5–2 for the available PLLs in the HardCopy III series devices for non-socket migration.
- For non-socket migration from an FPGA to HardCopy III (Table 5–4), you must select a companion device so that the Quartus II design software can restrict the usage of the available PLLs in the HardCopy III device. For example, when you migrate from a Stratix III EP3SL340-H1152 to a HC325WF484 package, the FPGA has eight PLLs, whereas the HardCopy III device has four PLLs.
- Enable PLL reconfiguration for your design if it uses PLLs. The PLL settings in HardCopy III devices may require different settings from the Stratix III PLLs because of the different clock tree lengths and PLL compensations. By enabling PLL reconfiguration, you can adjust your PLL settings on the HardCopy III device after the silicon has been fabricated. This allows you to fine tune and further optimize your system performance.
- Use dedicated clock input pins to drive the PLL reference clock inputs, particularly if your design is interfacing with an external memory. This minimizes reference clock input jitter to the PLLs, providing more margin for your design.

When you cascade PLLs for the ALTMEMPHY, ensure that:

- The input clock to the ALTMEMPHY PLL is fed by a dedicated input
- If the ALTMEMPHY PLL is fed by another PLL, the source PLL
  - input must be fed by a dedicated input pin
  - must be in no compensation mode
- If the input clock to the ALTMEMPHY is fed by another PLL, the ALTMEMPHY PLL's input clock must be from a dedicated clock output from the source PLL.

Table 5–4. Non-Socket Migration for HardCopy III and PLL Resource Availability (Part 1 of 2)

HardCopy III Device	Stratix III Prototype Device	L1	L2	L3	L4	T1	T2	B1	B2	R1	R2	R3	R4
HC325WF484	EP3SL110--F780 *(1)*	—	✓	—	—	✓	—	✓	—	—	✓	—	—
	EP3SL150--F780 *(1)*	—	✓	—	—	✓	—	✓	—	—	✓	—	—
	EP3SE110--F780 *(1)*	—	✓	—	—	✓	—	✓	—	—	✓	—	—
	EP3SL200--H780 *(1)*	—	✓	—	—	✓	—	✓	—	—	✓	—	—
	EP3SE260--H780 *(1)*	—	✓	—	—	✓	—	✓	—	—	✓	—	—
	EP3SL340--H1152 *(1)*, *(2)*	—	✓	(✓)	—	✓	(✓)	✓	(✓)	—	✓	(✓)	—

Table 5–4. Non-Socket Migration for HardCopy III and PLL Resource Availability (Part 2 of 2)

HardCopy III Device	Stratix III Prototype Device	L1	L2	L3	L4	T1	T2	B1	B2	R1	R2	R3	R4
HC325FF484	EP3SL110--F780 *(1)*	—	✓	—	—	✓	—	✓	—	—	✓	—	—
	EP3SL150--F780 *(1)*	—	✓	—	—	✓	—	✓	—	—	✓	—	—
	EP3SE110--F780 *(1)*	—	✓	—	—	✓	—	✓	—	—	✓	—	—
	EP3SL200--H780 *(1)*	—	✓	—	—	✓	—	✓	—	—	✓	—	—
	EP3SE260--H780 *(1)*	—	✓	—	—	✓	—	✓	—	—	✓	—	—
	EP3SL340--H1152 *(1)*, *(2)*	—	✓	(✓)	—	✓	(✓)	✓	(✓)	—	✓	(✓)	—
HC325WF780	EP3SL340--H1152 *(1)*, *(2)*	—	✓	(✓)	—	✓	(✓)	✓	(✓)	—	✓	(✓)	—
HC325FF780	EP3SL340--H1152 *(1)*, *(2)*	—	✓	(✓)	—	✓	(✓)	✓	(✓)	—	✓	(✓)	—

Notes to Table 5–4

(1) These are non-socket replacement devices. A board re-design is required.

(2) The FPGA has eight available PLLs and the HardCopy III device has four available PLLs.

Document Revision History

Table 5–5 lists the revision history for this chapter.

Table 5–5. Document Revision History

Date	Version	Changes
January 2011	3.1	■ Updated Table 5–2 and Table 5–4. Removed device HC315WF484. ■ Used new document template. ■ Minor text edits.
June 2009	3.0	Added non-socket information and new part numbers.
December 2008	2.0	Made minor editorial changes.
May 2008	1.0	Initial release.