External Memory Interface Handbook Volume 1

Section III. Selecting Device, Memory Components, and IP

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1. Selecting a Device

This chapter discusses the planning stage, to ensure that you know what to look for when selecting the right Altera® FPGA device for your memory interface.

Memory controllers in Altera devices require access to dedicated I/O element (IOE) features, PLLs, and several clock networks. Altera devices are feature rich in all these areas, so you must consider detailed resource and pin planning whenever implementing complex IP or multiple IP cores. This chapter provides an overview of what to consider in such instances.

Use the Altera Product Selector to find and compare specifications and features of Altera devices.

For information about the terms used in this document, refer to the *Glossary* chapter in volume 1 of the *External Memory Interface Handbook*.

For more information about supported memory types and configurations, refer to the *External Memory Interface System Specifications* section in volume 1 of the *External Memory Interface Handbook*.

When selecting the optimal Altera device for your memory interface, consider the following topics:

- "Device Pin Count" on page 1–2
- "External Memory Interface Features of Altera Devices" on page 1–3

Memory Standards and Configurations

There are two common types of high-speed memories that are supported by Altera devices: DRAM and SRAM. The commonly used DRAM devices include DDR, DDR2, and DDR3 SDRAM, and RDRAM II. SRAM devices include QDR II and QDR II+ SRAM.

Different Altera FPGA devices support different memory types; not all Altera devices support all memory types and configurations. Before you start your design, you must select an Altera device, which supports the memory standard and configurations you plan to use.

In addition, Altera's FPGA devices support various data widths for different memory interfaces. The memory interface support between density and package combinations differs, so you must determine which FPGA device density and package combination suits your application.

For more information about these memory standards, refer to the *Memory Standard Overviews* section in volume 1 of the *External Memory Interface Handbook*.

Device Pin Count

To meet the growing demand for memory bandwidth and memory data rates, memory interface systems use parallel memory channels and multiple controller interfaces. However, the number of memory channels is limited by the package pin count of the Altera devices. Hence, you must consider device pin count when you select a device; you must select a device with enough I/O pins for your memory interface requirement.

The number of device pins depends on the memory standard, the number of memory interfaces, and the memory data width. For example, a ×72 DDR3 SDRAM single-rank interface requires 125 I/O pins:

- 72 DQ pins (including ECC)
- 9 DM pins
- 9 DQS, DQSn differential pin pairs
- 17 address pins (address and bank address)
- 7 command pins (CAS, RAS, WE, CKE, ODT, reset, and CS)
- 1 CK, CK# differential pin pair

For the available number of DQS groups and the maximum number of controllers that is supported by the FPGAs for different memory types, refer to the *External Memory Interface System Specifications* section in volume 1 of the *External Memory Interface Handbook*.

Altera devices do not limit the interface widths beyond the following requirements:

- DQS, DQ, clock, and address signals of the entire interface should reside within the same bank or side of the device if possible, to achieve better performance. Although wraparound interfaces are also supported at limited frequencies.
- The maximum possible interface width in any particular device is limited by the number of DQS and DQ groups available within that bank or side.
- Sufficient regional clock networks are available to the interface PLL to allow implementation within the required number of quadrants.
- Sufficient spare pins exist within the chosen bank or side of the device to include all other clock, address, and command pin placement requirements.
- The greater the number of banks, the greater the skew. Altera recommends that you always compile a test project of your desired configuration and confirm that it meets timing requirement.

There is a constraint in Arria® II GX devices when assigning DQS and DQ pins. You are only allowed to use twelve of the sixteen I/O pins in an I/O module for DQ pin. The remaining four pins can only be used as input pin.

For DQS groups pin-out restriction format, refer to *Arria II GX Pin Connection Guidelines*.

Your pin count calculation also determines which device side to use (top or bottom, left or right, and wraparound).

Top or Bottom and Left or Right Interfaces

Ideally any interface should wholly reside in a single bank. However, interfaces that span across multiple adjacent banks or the entire side of a device are also fully supported. For Stratix III and Stratix IV devices, although vertical and horizontal I/O timing parameters are not identical, timing closure can be achieved on all sides of the FPGA for the maximum interface frequency.

Arria II GX, Cyclone® III, and Cyclone IV devices support interfaces spanning the top and bottom sides. In addition, Cyclone III and Cyclone IV E devices also support interfaces spanning left and right sides. Interfaces that span across sides (top and bottom, or left and right) and wraparound interfaces provide the same level of performance.

Arria II GX, Cyclone IV, and Stratix V devices do not support the left interface. There are no user I/O pins, other than the transceiver pins available in these devices.

Wraparound Interfaces

For maximum performance, Altera recommends that data groups for external memory interfaces should always be within the same side of a device, ideally reside within a single bank. High-speed memory interfaces using top or bottom I/O bank versus left or right IO bank have different timing characteristics, so the timing margins are also different. However, Altera can support interfaces with wraparound data groups that wraparound a corner of the device between vertical and horizontal I/O banks at some speeds. Some devices wraparound interfaces are same speed as row or column interfaces.

Arria II GX, Cyclone III and Cyclone IV devices can support wraparound interface across all sides of devices that are not used for transceivers. Other Altera devices only support interfaces with data groups that wraparound a corner of the device.

External Memory Interface Features of Altera Devices

This topic describes features from the Altera device families that enable external memory interfaces.

For more information on the external memory interface circuitry in an Altera FPGA device family, refer to the *External Memory Interfaces* chapter in the relevant device family handbook.

IOE Dedicated Features

When selecting an Altera device for your external memory system, you must select a device that is equipped with the features that suit your memory system requirements and configurations.

Altera devices have enhanced upon the IOE DDR capabilities by including the feature functionality availability directly in the IOE.

Table 1–1 shows which device families support these features.

Table 1–1. Device IOE Dedicated Features ***(Note 1)***

Features	Device Family			
	Arria II GX	Cyclone III and Cyclone IV	Arria II GZ, Stratix III, and Stratix IV	Stratix V
DDR input register	✓	— *(2)*	✓	✓
DDR output register	✓	✓	✓	✓
Synchronization registers	✓	— *(2)*	✓	✓ *(4)*
Alignment registers	—	—	✓ *(3)*	✓ *(4)*
Half-rate data registers	— *(2)*	— *(2)*	✓	✓
DQS phase-shift circuitry	✓	—	✓	✓
DQS postamble circuitry	✓	—	✓	✓
Differential DQS signaling	✓	—	✓	✓
Read and write leveling circuitry	—	—	✓ *(3)*	✓
Dynamic on-chip termination (OCT) control	—	—	✓	✓
Clock divider	—	—	✓	✓
Programmable delay	✓	✓	✓	✓
PLL	✓	✓	✓	✓
DLL	✓	—	✓	✓
Read FIFO	—	—	—	✓

Notes to Table 1–1:

(1) For more information, refer to the *Device I/O Features* chapter in the relevant device handbook.
(2) Implemented in the FPGA core fabric.
(3) This circuitry is not applicable for Arria II GZ devices.
(4) This register is not available for Altera megafunctions that use Stratix V devices.

To use these features implement one of the Altera high-performance controllers (a complete solution) or Altera PHY IP.

Alternatively, you may access these IOE features directly using the following low-level megafunctions:

- ALTDQ_DQS and ALTDQ_DQS2 megafunctions—allow you to parameterize the following features:
  - DDR I/O registers
  - Alignment and synchronization registers
  - Half data rate registers
  - DQS bus mode
- ALTDLL megafunction—allows you to parameterize the DQS phase-shift circuitry
- ALTOCT megafunction—allows you to parameterize the IOE OCT features.
- ALTPLL megafunction—allows you to parameterize the device PLL

- ALTIOBUF megafunction—allows you to parameterize the device IO features

Altera offers no support using these low-level megafunctions as an external memory PHY to implement your memory interfaces. If you use low-level megafunctions, you are solely responsible in creating every aspect of the interface, including timing analysis and debugging.

DDR Input and Output Registers

Arria II GZ, Stratix III, and Stratix IV devices provide DDR input and output registers on all sides. In Arria II GX, Cyclone IV, and Stratix V devices, the left side of the device is not available for interfacing. The DDR I/O structures can be directly implemented in the IOE in these devices, thus saving core logic and ensuring tight skew is easily maintained, which eases timing.

For Cyclone III and Cyclone IV devices, the DDR input registers are implemented in the core of the device. For Cyclone III and Cyclone IV devices, the read capture clock is derived from the PHY and is generated by the PLL to clock the DDR capture registers instead of using DQS read clock strobe from the memory device.

Synchronization and Alignment Registers

Resynchronization registers resynchronize the data from memory clock domain to the memory controller system clock domain. Alignment registers align the data after read resynchronization or write leveling process.

Altera IPs using Stratix V devices do not need synchronization and alignment registers.

In some devices, the synchronization registers are located in the core of the device, which makes the placement of these registers with respect to the DDR IOE critical to ensure that timing is achieved. Stratix III and Stratix IV devices have been enhanced to include the alignment and synchronization registers directly within the IOE, hence timing is now significantly improved and you are no longer concerned with ensuring critical register placement with respect to the DDR IOE. Typically, the resynchronization register is clocked via a dedicated output from the PLL. However, it may also be clocked directly from the read-leveling delay chain. The output alignment registers are typically clocked from the PLL.

If the resynchronization clock is sourced from the leveling delay chain, it may be cascaded from bank to bank, say 1A to 1B. In this configuration, memory controllers must form a single contiguous block of DQS groups that are not staggered or interleaved with another memory controller. Additionally, two PHYs cannot share the same subbank as only one leveling delay chain exists per subbank.

Arria II, Cyclone III, and Cyclone IV devices do not have leveling circuitry, so there is no need for alignment registers. Synchronization registers for Arria II devices are implemented in the IOE. These synchronization registers in Cyclone III and Cyclone IV devices are implemented in the FPGA core fabric and are clocked directly by the PLL. In Cyclone III and Cyclone IV devices, these registers are clocked by the same PLL output clock that also clocks the DDR registers.

Generally, alignment and synchronization registers are optional and can be bypassed if not required. However, Altera external memory interface IP always implements these synchronization registers, regardless of interface speed. Hence latency through the PHY may not be optimal for lower frequency designs.

Half-Rate Data Registers

As external memory interface clock speeds increase, the core f_{MAX} can become the limiting factor in interface design. A common solution, which increases core f_{MAX} timing problems, is to implement a half-rate architecture. This solution doubles the data width on the core side interfaces compared to a full-rate SDR solution, but also halves the required operating frequency.

Arria II GZ, Stratix III, Stratix IV, and Stratix V devices include dedicated full-rate to half-rate registers within the IOE.

Arria II GX, Cyclone III, and Cyclone IV devices implement half-rate registers in the core of the device.

DQS Phase-Shift Circuitry

Devices that use DQS or CQ pins to clock the read data during read operation offer DQS phase-shift circuitry. This circuitry phase shifts the DQS and CQ_n pins during the transaction, to obtain optimal read capture margin. DQS phase-shift circuitry consists of a DLL and phase offset control block, to further fine tune the DQS phase shift.

Cyclone III and Cyclone IV devices do not have this feature, because DQS signals are not needed during read operations at lower frequencies.

DQS Postamble Circuitry

DQS postamble circuitry eliminates invalid DQ data capturing, because of the postamble glitches on the DQS signals through an override on DQS. This feature ensures the correct clock cycle timing of the postamble enable signal.

Altera devices only need DQS postamble circuitry to use the DQS scheme in read operation for clocking read data. Arria II, Stratix III, Stratix IV, and Stratix V devices have this feature.

As Cyclone III and Cyclone IV devices do not use DQS for capturing read data, they do not have this circuitry.

Differential DQS Signaling

Altera devices (except Cyclone III and Cyclone IV devices) directly support differential DQS signalling and the single-ended standard supported in previous device families. DDR SDRAM only supports single-ended DQS, DDR2 SDRAM additionally includes the option of differential DQS signaling. DDR3 SDRAM only supports differential DQS signaling.

Differential DQS signaling is recommended for DDR2 SDRAM designs operating at or above 333 MHz. Differential DQS strobe operation enables improved system timing due to reduced crosstalk and less simultaneous switching noise on the strobe output drivers. You can use single-ended DQS mode for DDR2 SDRAM interfaces, but it requires more pessimistic timing data and hence results in less system timing margin.

Cyclone III and Cyclone IV devices do not support differential signalling and thus do not support DDR3 SDRAM, which requires DQS signaling.

Read and Write Leveling

Stratix III, Stratix IV, and Stratix V I/O registers include read and write leveling circuitry to enable skew to be removed or applied to the interface on a DQS group basis. There is one leveling circuit located in each I/O subbank.

☞ ALTMEMPHY-based designs for DDR and DDR2 SDRAM (and DDR3 SDRAM without leveling) do not use leveling circuitry, as it is not needed by the memory standard. ALTMEMPHY-based designs for DDR3 SDRAM DIMMs (and components with fly-by topology like DIMMs) use leveling circuitry.

☞ UniPHY-based designs do not require read leveling circuitry during read leveling operation.

Dynamic OCT

Arria II GZ, Stratix III, Stratix IV, and Stratix V devices support dynamic calibrated OCT. This feature allows the specified series termination to be enabled during writes, and parallel termination to be enabled during reads. These I/O features allow you to greatly simplify PCB termination schemes.

Clock Divider

To ease data alignment, a single I/O clock divider may be used for an entire interface, as the half-rate resynchronization clock can be cascaded from DQ group to the adjacent DQ group. Hence, when using a common I/O clock divider, data alignment may be performed across the entire interface. Individual I/O clock dividers require the data alignment to be performed on a DQ group basis.

Arria II GZ, Stratix III, Stratix IV, and Stratix V devices include a dedicated I/O clock divider on a per DQS group basis, to simplify and reduce the number of clocks required. The output of this clock divider can then directly source the half-rate resynchronization clock from the full-rate version.

Arria II GX, Cyclone III, and Cyclone IV devices do not have the clock divider feature, and so must use separate PLL output.

ALTMEMPHY-based designs support both balanced (without leveling) and unbalanced (with leveling) CAC topologies. ALTMEMPHY-based designs with leveling designs use multiple I/O clock dividers on a DQ group basis and do not support balanced CAC topologies, as a dedicated resynchronization and half-rate resynchronization clock is required on a per DQS group basis. ALTMEMPHY-based designs without leveling designs use a single I/O clock divider for the whole interface to reduce PHY complexity and reduce latency. However, ALTMEMPHY-based without leveling interfaces cannot be interleaved, because of FPGA limitations.

In UniPHY-based designs, a clock divider is instantiated in the core of the device for each DQS groups.

Programmable Delay

I/O registers include programmable delay chains that you may use to deskew interfaces. Each pin can have different delay settings, hence read and write margins can be increased as uncertainties between signals can be minimized.

The DQ-DQS offset scheme is applicable for interfacing systems using QDR II and QDR II+ SRAM, RLDRAM II, DDR, DDR2 and DDR3 SDRAM components for frequencies of 400 MHz and below. For interfacing system using DDR3 SDRAM components with frequencies above 400 MHz, a dynamic deskew scheme improves the timing margins.

For DQ-DQS offset schemes, delay-chains in the IOE shift the offset between DQ and DQS, to meet timing. The offsets employed are FPGA family, speed grade and frequency dependent.

For systems using DDR3 SDRAM interfaces at frequencies above 400 MHz, the timing margins are too small to be fixed by the static DQ-DQS offset scheme. Hence, a dynamic scheme improves the setup and hold margin at the memory component with the DLL set to 8-tap mode. Configurable delay elements and delay-chains in the IOE observe the write window in the DDR3 SDRAM components. This information configures the delays for each individual DQ and DM pins, to meet the memory component setup and hold requirements and reduce skew between DQ and DM pins in a DQS group.

Read FIFO

Read FIFO buffer is only available for Stratix V devices. Read FIFO buffer is added to the Stratix V I/O element (IOE) to resynchronize captured data from the capture clock domain to the system clock domain. The resynchronization helps improve the performance of the Stratix V devices, and removes the need for synchronization and alignment registers.

PLL and DLL

Altera devices use PLLs to generate the memory controller clocks. The simplest slowest speed memory controllers may only require two clocks (0° system clock and –90° write clock). However, as interface speeds increase, it becomes harder to close timing and so dedicated resynchronization, postamble, and address and command clocks are typically required. Additionally, at higher frequencies the maximum frequency becomes the bottleneck and half-rate designs are the typical solution. Thus complex half high data rate designs require typically 10 clock networks. Altera devices are well equipped to address the clocking requirements of external memory interfaces.

For more information about the availability of PLL in each device family, refer to the clock network and PLL chapter in the device handbooks. For more information about the availability of DLL in each device family, refer to the *External Memory Interfaces* chapter in the device handbooks.

2. Selecting your Memory Component

This chapter details some of the high-speed memory selection criteria and describes some typical applications where these memories are used. It looks at the main types of high-speed memories available, memory selection based on strengths and weaknesses, and which Altera® FPGAs these devices can interface with. It concludes with some typical application examples.

This chapter highlights the memory component's capability. The Altera IP may or may not support all of the features supported by the memory.

For the maximum supported performance supported by Altera FPGAs, refer to the *External Memory Interface System Specifications* section in volume 1 of the *External Memory Interface Handbook*.

System architects must resolve a number of complex issues in high-performance system applications that range from architecture, algorithms, and features of the available components. Typically, one of the fundamental problems in these applications is memories, as the bottlenecks and challenges of system performance often reside in its memory architecture. As higher speeds become necessary for external memories, signal integrity gets more difficult. Newer devices have added several features to overcome this issue. Altera FPGAs also support these advancements with dedicated I/O circuitry, various I/O standard support, and specialized intellectual property (IP).

Memory Overview

The main considerations for choosing an external memory device are bandwidth, size, cost, latency, and power. Since no single memory type can excel in every area, system architects must determine the right balance for their design.

There are two common types of high-speed memories: DRAM and SRAM. DRAM devices are volatile memories offering a lower cost per bit than SRAM devices. A compact memory cell consisting of a capacitor and a single transistor makes this possible, as opposed to the six-transistor cell used in SRAM. However, as the capacitor discharges, the memory cell loses its state. This means that DRAM memory must be refreshed periodically, resulting in lower overall efficiency and more complex controllers. Generally, designers only choose DRAM where cost per bit is important.

DDR, DDR2, and DDR3 SDRAM

The desktop computing market has positioned double data rate (DDR) SDRAM as a mainstream commodity product, which means this memory is very low-cost. DDR SDRAM is also high-density and low-power. Relative to other high-speed memories, DDR SDRAM has higher latency-they have a multiplexed address bus, which reduces the pin count (minimizing cost) at the expense of a longer and more complex bus

cycle. DDR2 SDRAM includes additional features such as increased bandwidth due to higher clock speeds, improved signal integrity on DIMMs with on-die terminations, and lower supply voltages to reduce power. DDR3 SDRAM is the latest generation of SDRAM and further increases bandwidth, lowers power, and improves signal integrity with fly-by and dynamic on-die terminations.

RLDRAM and RLDRAM II

Reduced latency DRAM (RLDRAM) is optimized to reduce latency primarily for networking and cache applications. RLDRAM is partitioned into eight smaller banks. This partioning reduces the parasitic capacitance of the address and data lines, allowing faster accesses and reducing the probability of random access conflicts. Also, most DRAM memory types need both a row and column phase on a multiplexed address bus to support full random access, while RLDRAM supports a non-multiplexed address, saving bus cycles at the expense of more pins. RLDRAM utilizes higher operating frequencies and uses the 1.8V High-Speed Transceiver Logic (HSTL) standard with DDR data transfer to provide a very high throughput. RLDRAM II offers faster random access times, on-die termination, a delay-locked loop (DLL) for higher frequency operation, larger densities, wider data paths, and higher bus utilization compared with RLDRAM.

QDR, QDR II, and QDR II+ SRAM

SRAMs are fundamentally different from DRAMs in that a typical SRAM memory cell consists of six transistors, while a DRAM cell consists of a transistor and a capacitor used to store a charge. Inherently, SRAM is a low-density, high-power memory device, with very low latency compared to DRAM (as the capacitor in the DRAM is slow). In most cases, SRAM latency is one clock cycle.

Quad Data Rate (QDR) SRAM has independent read and write ports that run concurrently at double data rate. QDR SRAM is true dual-port (although the address bus is still shared), which gives this memory a significantly higher bandwidth. QDR SRAM is best suited for applications where the required read/write ratio is near one-to-one. QDR II SRAM includes additional features such as increased bandwidth due to higher clock speeds, lower voltages to reduce power, and on-die termination to improve signal integrity. QDR II+ SDRAM is the latest and fastest generation.

Memory Selection

One of the first considerations in choosing a high-speed memory is data bandwidth. Based on the system requirements, an approximate data rate to the external memory should be determined. Table 2–1 details the memory bandwidth for various technologies with the assumptions of a 32-bit data bus, operating at the maximum supported frequency in a Stratix® IV FPGA. The bandwidth column in this table includes a conservative DRAM bandwidth at 70 percent efficiency, which takes into consideration bus turnaround, refresh, burst length, and random access latency. The calculation assumes 85 % efficiency for QDR and QDR II SRAM.

Table 2–1. Memory Bandwidth for 32-bit Wide Data Bus in Stratix IV FPGA

Memory	Clock Frequency (MHz)	Bandwidth for 32 bits (Gbps)	Bandwidth at % Efficiency (Gbps) *(1)*
DDR3 SDRAM	533	34.1	23.9
DDR2 SDRAM	400	25.6	17.9
DDR SDRAM	200	12.8	9
RLDRAM II	400	25.6	17.9
QDR SRAM	200	25.6	21.8
QDR II SRAM	350	44.8	38.1
QDR II+ SRAM	350	44.8	38.1

Note to Table 2–1:

(1) 70% for DDR memories, 85% for QDR memories

You must also consider other memory attributes, including how much memory is required (density), how much latency can be tolerated, what is the power budget, and whether the system is cost sensitive. Table 2–2 is an overview of high-speed memories, and details some of the features and target markets of each technology.

Table 2–2. Memory Selection Overview

Parameter	DDR3 SDRAM	DDR2 SDRAM	DDR SDRAM	RLDRAM II	QDR II/+ SRAM
Performance	400–800 MHz	200–400 MHz	100–200 MHz	200–533 MHz	154–350 MHz
Altera-supported data rate	Up to 1066 Mbps	Up to 800 Mbps	Up to 400 Mbps	Up to 2132 Mbps	Up to 1400 Mbps
Density	512 Mbytes–8 Gbytes, 32 Mbytes – 8 Gbytes (DIMM)	256 Mbytes–1 Gbytes, 32 Mbytes – 4 Gbytes (DIMM)	128 Mbytes–1 Gbytes, 32 Mbytes – 2 Gbytes (DIMM)	288 Mbytes, 576 Mbytes	8–72 Mbytes
I/O standard	SSTL-15 Class I, II	SSTL-18 Class I, II	SSTL-2 Class I, II	HSTL-1.8V/1.5V	HSTL-1.8V/1.5V
Data width (bits)	4, 8, 16	4, 8, 16	4, 8, 16, 32	9, 18, 36	8, 9, 18, 36
Burst length	8	4, 8	2, 4, 8	2, 4, 8	2, 4
Number of banks	8	8 (>1 GB), 4	4	8	N/A
Row/column access	Row before column	Row before column	Row before column	Row and column together or multiplexed option	N/A
CAS latency (CL)	5, 6, 7, 8, 9, 10	3, 4, 5	2, 2.5, 3	4, 6, 8	N/A

Table 2–2. Memory Selection Overview

Parameter	DDR3 SDRAM	DDR2 SDRAM	DDR SDRAM	RLDRAM II	QDR II/+ SRAM
Posted CAS additive latency (AL)	0, CL-1, CL-2	0, 1, 2, 3, 4	N/A	N/A	N/A
Read latency (RL)	RL = CL + AL	RL = CL + AL	RL = CL	RL = CL/CL + 1	1.5 clock cycles
On-die termination	Yes	Yes	No	Yes	Yes
Data strobe	Differential bidirectional strobe only	Differential or single-ended bidirectional strobe	Single-ended bidirectional strobe	Free-running differential read and write clocks	Free-running read and write clocks
Refresh requirement	Yes	Yes	Yes	Yes	No
Relative cost comparison	Presently lower than DDR2	Less than DDR SDRAM with market acceptance	Low	Higher than DDR SDRAM, less than SRAM	Highest
Target market	Desktops, servers, storage, LCDs, displays, networking, and communication equipment	Desktops, servers, storage, LCDs, displays, networking, and communication equipment	Desktops, servers, storage, LCDs, displays, networking, and communication equipment	Main memory, cache memory, networking, packet processing, and traffic management	Cache memory, routers, ATM switches, packet memories, lookup, and classification memories

Altera supports these memory interfaces, provides various IP for the physical interface and the controller, and offers many reference designs (refer to Altera's Memory Solutions Center).

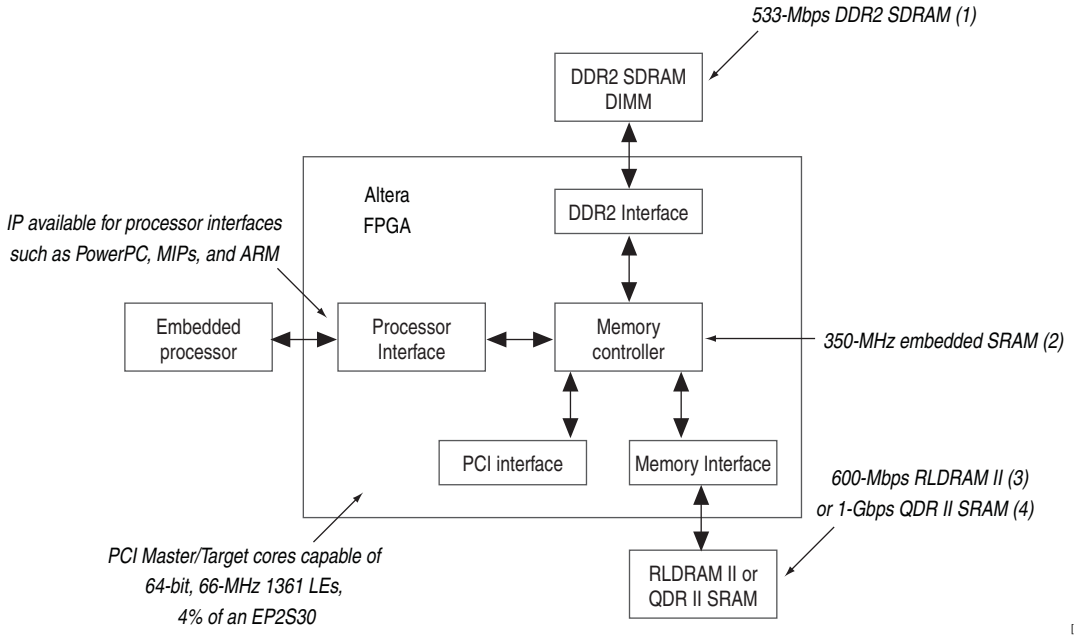
For Altera support and the maximum performance for the various high-speed memory interfaces, refer to the *External Memory Interface System Specifications* section in volume 1 of the *External Memory Interface Handbook.*

High-Speed Memory in Embedded Processor Application Example

In embedded processor applications—any system that uses processors, excluding desktop processors—DDR SDRAM is typically used for main memory due to its very low cost, high density, and low power. Next-generation processors invest a large amount of die area to on-chip cache memory to prevent the execution pipelines from sitting idle. Unfortunately, these on-chip caches are limited in size, as a balance of performance, cost, and power must be taken into consideration. In many systems, external memories are used to add another level of cache. In high-performance systems, three levels of cache memory is common: level one (8 Kbytes is common) and level two (512 Kbytes) on chip, and level three off chip (2 Mbytes).

High-end servers, routers, and even video game systems are examples of high-performance embedded products that require memory architectures that are both high speed and low latency. Advanced memory controllers are required to manage transactions between embedded processors and their memories. Altera Arria® series and Stratix series FPGAs optimally implement advanced memory controllers by utilizing their built-in DQS (strobe) phase shift circuitry. Figure 2–1 highlights some of the features available in an Altera FPGA in an embedded application, where DDR2 SDRAM is used as the main memory and QDR II SRAM or RLDRAM II is an external cache level.

Figure 2–1. Memory Controller Example Using FPGA



Notes to Figure 2–1:

(1) 533-Mbps DDR2 SDRAM operation using dedicated DQS circuitry, post-amble circuitry, automatic phase shifting, and six registers in the I/O element: 790 LEs, 3% of an EP2S30, and four clock buffers (for a 72-bit interface).

(2) High-speed memory interfaces such as QDR II SRAM require at least four clock buffers to handle all the different clock phases and data directions.

(3) 600-Mbps RLDRAM II operation: 740 logic elements (LEs), 3% of an EP2S30, and four clock buffers (for a 36-bit wide interface).

(4) Embedded SRAM with features such as true-dual port and 350-MHz operation allows complex “store and forward” memory controller architectures.

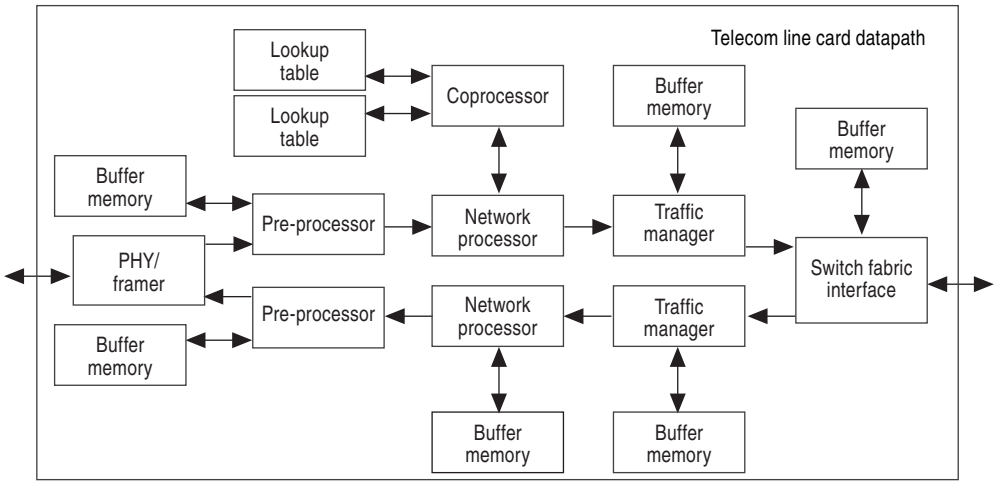
(5) The Quartus II software reports the number of adaptive look-up tables (ALUTs) that the design uses in the FPGA. The LE count is based on this number of ALUTs.

One of the target markets of RLDRAM II and QDR/QDR II SRAM is external cache memory. RLDRAM II has a read latency close to SSRAM, but with the density of SDRAM. A 16 times increase in external cache density is achievable with one RLDRAM II versus that of SSRAM. In contrast, consider QDR and QDR II SRAM for systems that require high bandwidth and minimal latency. Architecturally, the dual-port nature of QDR and QDR II SRAM allows cache controllers to handle read data and instruction fetches completely independent of writes.

High-Speed Memory in Telecom Application Example

Because telecommunication network architectures are becoming more complex, high-end network systems are running multiple 10-Gbps line cards that connect to multi-shelf switch fabrics scaling to Terabits per second. Figure 2–2 shows an example of a typical system line interface card. These line cards offer interfaces ranging from a single-port OC-192 to multi-port Gigabit Ethernet, and consist of a number of devices, including a PHY/framer, network processors, traffic managers, fabric interface devices, and high-speed memories.

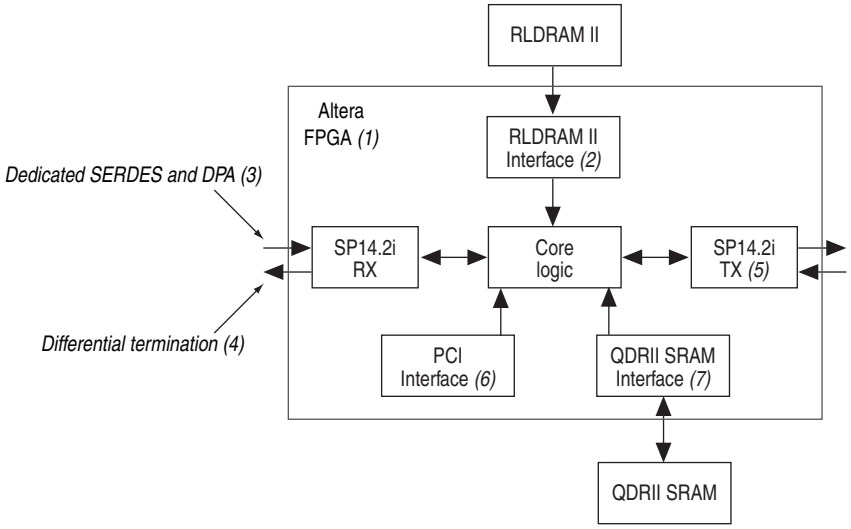
Figure 2–2. Typical Telecom System Line Interface Card



As packets traverse from the PHY/framer device to the switch fabric interface, they are buffered into memories, while the data path devices process headers (determining the destination, classifying packets, and storing statistics for billing) and control the flow of packets into the network to avoid congestion. Typically DDR/DDR2/DDR3 SDRAM and RLDRAM II are used for large buffer memories off network processors, traffic managers, and fabric interfaces, while QDR and QDR II SRAMs are used for look-up tables (LUTs) off preprocessors and coprocessors.

In many designs, FPGAs connect devices together for interoperability and coprocessing, implement features that are not supported by ASIC devices, or implement a device function entirely. Altera Stratix series FPGAs implement traffic management, packet processing, switch fabric interfaces, and coprocessor functions, using features such as 1 Gbps LVDS I/O, high-speed memory interface support, multi-gigabit transceivers, and IP cores. Figure 2–3 highlights some of these features in a packet buffering application where RLDRAM II is used for packet buffer memory and QDR II SRAM is used for control memory.

Figure 2–3. FPGA Example in Packet Buffering Application



Notes to Figure 2–3:

(1) As an example, 85% of the LEs still available in an EP2S90.

(2) 600-Mbps RLDRAM II operation: 740 LEs, 1% of an EP2S90, and four clock buffers (for a 36-bit wide interface).

(3) Dedicated hardware SERDES and DPA circuitry allows clean and reliable implementation of 1-Gbps LVDS.

(4) Differential termination is built in Stratix FPGAs, simplifying board layout and improving signal quality.

(5) SPI 4.2i core capable of 1 Gbps: 5178 LEs per Rx, 6087 LEs per Tx, 12% of an ES2S90, and four clock buffers (for both directions using individual buffer mode, 32-bit data path, and 10 logical ports).

(6) PCI cores capable of 64-bit 66-MHz 656 LEs, 1% of an EP2S90 for a 32-bit target

(7) 1-Gbps QDR II SRAM operation: 100 LEs, 0.1% of an EP2S90, and four clock buffers (for an 18-bit interface).

(8) Note that the Quartus II software reports the number of ALUTs that the design uses in Stratix II devices. The LE count is based on this number of ALUTs.

SDRAM is usually the best choice for buffering at high data rates due to the large amounts of memory required. Some system designers take a hybrid approach to the memory architecture, using SRAM to store the packet headers and DRAM to store the payload. The depth of the memories depends on the architecture and throughput of the system.

The buffer memory for the packet buffering application of an OC-192 line card (approximately 10 Gbps) must be able to sustain a minimum of one write and one read operation, which requires a memory bandwidth of 20 Gbps to operate at full line rate (more bandwidth is required if the headers are modified). The bandwidth requirement for memory is a key factor in memory selection (see Table 2–1). As an

example, a simple first-order calculation using RLDRAM II as buffer memory requires a bus width of 48 bits to sustain 20 Gbps (300 MHz × 2 DDR × 0.70 efficiency × 48 bits = 20.1 Gbps), which needs two RLDRAM II parts (one ×18 and one ×36). RLDRAM II also inherently includes the additional memory bits used for parity or error correction code (ECC).

QDR and QDR II SRAM have bandwidth and low random access latency advantages that make them useful for control memory in queue management and traffic management applications. Another typical implementation for this memory is billing and packet statistics, where each packet requires counters to be read from memory, incremented, and then rewritten to memory. The high bandwidth, low latency, and optimal one-to-one read/write ratio make QDR SRAM ideal for this feature.

3. Selecting Memory IP

This chapter gives you an overview of Altera external memory controllers and PHY IP.

Altera FPGAs achieve optimal memory interface performance with external memory IP. The IP comprises two key components:

- PHY—the physical layer that guarantees the best timing margin and latency for the interface between FPGA and memories
- Controller—the state machine that guarantees efficient data transfers between FPGA and memories.

Altera provides modular memory solutions, which allow you to customize your memory interface design. You can build a custom PHY, a custom controller, or both, as desired.

Table 3–1 shows the recommended memory types and controllers that Altera offers with the PHY IP.

Table 3–1. Altera Memory Types, PHY, and Controllers in the Quartus II Software (Part 1 of 2)

Quartus II Version	Memory	PHY IP	Controller IP
11.0	DDR/DDR2/DDR3	ALTMEMPHY (AFI)	HPC II
	DDR2/DDR3	UniPHY Nios-based Sequencer	HPC II
	QDR II/QDR II+	UniPHY Nios-based and RTL Sequencer	QDR/RLD II controller
	RLDRAM II	UniPHY Nios-based and RTL Sequencer	QDR/RLD II controller
	Other	ALTDQ_DQS *(1)*	Custom
	Other	ALTDQ_DQS2 *(2)*	Custom
10.1	DDR/DDR2/DDR3	ALTMEMPHY (AFI)	HPC HPC II
	DDR2/DDR3	UniPHY Nios-based Sequencer	HPC II
	QDR II/QDR II+	UniPHY RTL Sequencer	QDR/RLD II controller
	RLDRAM II	UniPHY RTL Sequencer	QDR/RLD II controller
	Other	ALTDQ_DQS *(1)*	Custom
	Other	ALTDQ_DQS2 *(2)*	Custom
10.0	DDR/DDR2/DDR3	ALTMEMPHY (AFI)	HPC HPC II
	DDR2/DDR3	UniPHY Nios-based Sequencer	HPC II
	QDR II/QDR II+	UniPHY RTL Sequencer	QDR/RLD II controller
	RLDRAM II	UniPHY RTL Sequencer	QDR/RLD II controller
	Other	ALTDQ_DQS *(1)*	Custom
	Other	ALTDQ_DQS2 *(2)*	Custom

Table 3–1. Altera Memory Types, PHY, and Controllers in the Quartus II Software (Part 2 of 2)

Quartus II Version	Memory	PHY IP	Controller IP
9.1	DDR/DDR2/DDR3	ALTMEMPHY (AFI)	HPC HPC II
	QDR II/QDR II+	UniPHY	QDR II controller
	RLDRAM II	UniPHY	RLDRAM II controller
	Other	ALTDQ_DQS	Custom
9.0	DDR/DDR2/DDR3	ALTMEMPHY (AFI) *(3)*	High-performance controller (HPC)
	QDR II/QDR II+	ALTMEMPHY	—
	RLDRAM II	Custom	Custom
	Other	ALTDQ_DQS	Custom

Note to Table 3–1:

(1) Applicable for Arria II, Stratix III, and Stratix IV devices.

(2) Applicable only for Stratix V devices.

(3) AFI = Altera PHY interface

For more information about the controllers with the UniPHY or the ALTMEMPHY IP, refer to *Volume 3: Implementing Altera Memory Interface IP* of the *External Memory Interface Handbook*.
For more information about the ALTDQ_DQS megafunction, refer to the *ALTDLL and ALTDQ_DQS Megafunctions User Guide*.
For more information about the ALTDQ_DQS2 megafunction, refer to the *ALTDQ_DQS2 Megafunction User Guide*.

Altera recommends that you use the HPC II architecture with the UniPHY IP for all new designs because Altera will continue optimizing the UniPHY IP and the HPC II architecture.

PHY IP

Altera offers two PHY IP options: ALTMEMPHY and UniPHY. The UniPHY IP is the latest PHY architecture that has several enhanced features to support the needs of high-performance applications.

Table 3–2 lists the benefits of using the UniPHY IP.

Table 3–2. UniPHY IP Features and Benefits (Part 1 of 2)

Feature	Benefit
Latency	■ The latency is half of the ALTMEMPHY IP. ■ The system performance for random accesses is improved more than 50%.
PLL, DLL and OCT sharing	Enables multiple memory interfaces on single chip.
Configuration support	Supports mainstream configurations for DDR2 and DDR3 SDRAM, QDR II and QDR II+ SRAM, RLDRAM II controllers with various widths, burst sizes, DIMM types, and multiple ranks through the Quartus II software.

Table 3–2. UniPHY IP Features and Benefits (Part 2 of 2)

Feature	Benefit
Calibration algorithm	Allows for higher performance through advanced calibration algorithms with improved debugging capability and easier customization.
Design flow	Has easier design flow with the following features: ■ Modular clear text code ■ Transparent and flexible timing model ■ Improved testbenches for faster development and easier debugging

While the UniPHY IP is a more enhanced technology, a limited number of the ALTMEMPHY configurations may show some advantages in resource utilization and simulation time.

☞ Altera's next generation product families will not support the ALTMEMPHY IP.

Resource Utilization

Use the appropriate PHY IPs based on the requirements of your design.

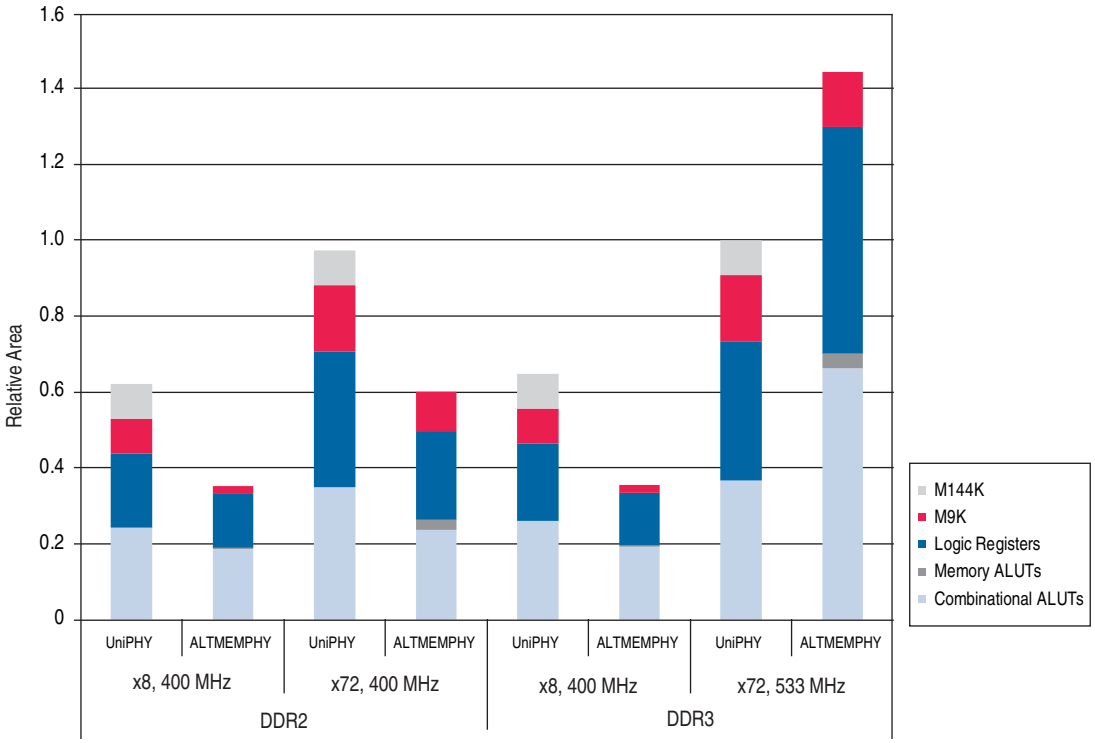
Table 3–3 lists the comparisons between the UniPHY and the ALTMEMPHY IP for resource utilization.

Table 3–3. Resource Utilization Comparisons for the UniPHY and ALTMEMPHY IP

UniPHY IP	ALTMEMPHY IP
■ The UniPHY IP is more efficient in resource utilization for wide interfaces of higher performance. ■ The UniPHY IP has advanced calibration algorithms which, while more robust, may consume more resources. ■ For example, for 533-MHz 72-bit DDR3 interface, the normalized area (LEs and internal memory), for the UniPHY IP is 35% smaller than that of the ALTMEMPHY IP.	■ The ALTMEMPHY IP consumes less resources for smaller interfaces. ■ The area for the ALTMEMPHY IP is smaller for slower and narrow DDR2 interfaces because the calibration sequencer state machines for these configurations are smaller. ■ For example, for 400-MHz 8-bit DDR2 interface, the normalized area for the ALTMEMPHY IP is 40% smaller than that of the UniPHY IP.

Figure 3–1 shows the comparisons between the UniPHY and the ALTMEMPHY IP for area utilization.

Figure 3–1. Area Utilization Comparison Chart for the UniPHY and ALTMEMPHY IP



As all new feature development focusses on the UniPHY IP only, Altera will continue to optimize area for future Quartus II releases.

For specific configurations, Altera recommends that you check the resource utilization that the Quartus II software reports. For detailed UniPHY resource utilization data, refer to the "Resource Utilization" section in the *DDR2 and DDR3 SDRAM Controller with UniPHY IP User Guide*, *RLDRAM II Controller with UniPHY IP User Guide*, and *QDR II and QDR II+ SRAM Controller with UniPHY IP User Guide* in volume 3 of the *External Memory Interface Handbook*.

Recommended IP for Your FPGA Device

Table 3–4 shows the recommended PHY options for different FPGA devices and memory types.

Table 3–4. Recommended PHY Options Available in the Quartus II Software 11.0

Family	PHY Support					
	DDR SDRAM	DDR2 SDRAM	DDR3 SDRAM	RLDRAM II	QDR II SRAM	QDR II+ SRAM
Arria II GX	ALTMEMPHY	ALTMEMPHY	ALTMEMPHY	—	UniPHY	UniPHY
Arria II GZ	—	UniPHY	UniPHY	UniPHY	UniPHY	UniPHY
Cyclone III and Cyclone IV E (1.2 V)	ALTMEMPHY	ALTMEMPHY	—	—	—	—
Cyclone IV E (1.0 V)	ALTMEMPHY	ALTMEMPHY	—	—	—	—
Cyclone IV GX	ALTMEMPHY	ALTMEMPHY	—	—	—	—
HardCopy III and HardCopy IV	ALTMEMPHY	UniPHY	UniPHY	UniPHY	UniPHY	UniPHY
Stratix III	ALTMEMPHY	UniPHY	UniPHY	UniPHY	UniPHY	UniPHY
Stratix IV E/GX/GT	ALTMEMPHY	UniPHY	UniPHY	UniPHY	UniPHY	UniPHY
Stratix V	—	UniPHY	UniPHY	UniPHY	UniPHY	UniPHY

4. Maximum Clock Rates

This chapter describes the highest achievable clock rates supported when using Altera memory controllers.

Specifications for HardCopy® IV E, and Stratix® V devices are preliminary and subject to change.

For the complete set of maximum clock rates support including all temperature and speed grades, full rate, row and wraparound I/Os and multiple chip-selects on Altera FPGA and HardCopy ASIC devices, refer to the External Memory Interface Specification Estimator tool.

For a list of supported and unsupported features for your memory interface IP, refer to the appropriate user guide in *Volume 3: Implementing Altera Memory Interface IP*.

Table 4–1 shows the maximum clock rates supported on column I/Os on Altera FPGA and HardCopy ASIC devices with fastest speed grades for single chip-select.

Table 4–1. Maximum Half-Rate Clock Rates (Part 1 of 2)

Device	Temp and Speed Grade	Maximum Half-Rate Clock Rate (MHz) *(1)*					
		DDR3 SDRAM *(2)*	DDR2 SDRAM	DDR SDRAM	RLDRAM II	QDR II SRAM *(10)*	QDR II+ SRAM *(10)*
Stratix V	C2	533 MHz	400 MHz	Not Supported	400 MHz *(5)*	350 MHz	550 MHz
Stratix IV	C2/C2x	533 MHz	400 MHz	200 MHz	533 MHz *(5) (6)*	350 MHz	550 MHz
Stratix III	C2	533 MHz	400 MHz	200 MHz	400 MHz *(5)*	350 MHz	400 MHz
Arria II GZ	C3	400 MHz	333 MHz	Not Supported	350 MHz	300 MHz	350 MHz
Arria II GX *(3)*	C4	400 MHz *(4) (5)*	333 MHz	200 MHz	Not Supported	250 MHz	250 MHz
Cyclone IV	C6	Not Supported	200 MHz	167 MHz		Not Supported	Not Supported
Cyclone III	C6		200 MHz	167 MHz			
Cyclone III LS	C7		167 MHz	150 MHz			

Table 4–1. Maximum Half-Rate Clock Rates (Part 2 of 2)

Device	Temp and Speed Grade	Maximum Half-Rate Clock Rate (MHz) *(1)*					
		DDR3 SDRAM *(2)*	DDR2 SDRAM	DDR SDRAM	RLDRAM II	QDR II SRAM *(10)*	QDR II+ SRAM *(10)*
HardCopy IV GX FF Flip Chip	C	533 MHz *(7)*	333 MHz *(8)*	200 MHz	350 MHz *(5) (9)*	300 MHz *(11)*	350 MHz *(8)*
HardCopy IV E FF Flip Chip	C	400 MHz	333 MHz *(8)*	200 MHz		300 MHz *(11)*	350 MHz *(8)*
HardCopy III FF Flip Chip	C	400 MHz	333 MHz *(8)*	200 MHz		300 MHz *(11)*	350 MHz *(8)*

Notes:

(1) The maximum clock rates listed here are guidelines based on Altera designs. The actual achievable performance of your design is based on your system's features and must be attained through the Quartus II timing analysis of the complete design.

(2) For DDR3 SDRAM Controller with UniPHY, Altera recommends that you use leveling circuitry for any DDR3 SDRAM interface.

(3) No DDR3 DIMM support for Arria II GX devices.

(4) To achieve the maximum clock rate, you require a low board skew within a DQS or DQ group.

(5) To achieve the maximum clock rate, use 533 MHz memory device speed grade.

(6) Achievable with Nios II sequencer only.

(7) For 533 MHz clock rate, contact Altera.

(8) To achieve the maximum clock rate, use 400 MHz memory device speed grade.

(9) The maximum clock rate for x36 interfaces is 170 MHz.

(10) Nonemulation clock rates.

(11) To achieve the maximum clock rate, use 333 MHz memory device speed grade.

This chapter provides additional information about the document and Altera.

Document Revision History

The following table shows the revision history for this document.

Date	Version	Changes
June 2011	3.0	■ Added *Selecting your Memory Component* chapter from Volume 1 Section II. ■ Added *Selecting Memory IP* chapter from Volume 2 Section I. ■ Added *Selecting a Device* chapter from Volume 2 Section I.
December 2010	2.1	■ Moved protocol-specific feature information to the memory interface user guides in Volume 3. ■ Updated maximum clock rate information for 10.1.
July 2010	2.0	■ Added specifications for DDR2 and DDR3 SDRAM Controllers with UniPHY. ■ Streamlined the specification tables. ■ Added reference to web-based Specification Estimator Tool.
January 2010	1.1	Updated DDR, DDR2, and DDR3 specifications.
November 2009	1.0	First published.

How to Contact Altera

To locate the most up-to-date information about Altera products, refer to the following table.

Contact *(1)*	Contact Method	Address
Technical support	Website	www.altera.com/support
Technical training	Website	www.altera.com/training
	Email	custrain@altera.com
Product literature	Website	www.altera.com/literature
Non-technical support (General)	Email	nacomp@altera.com
(Software Licensing)	Email	authorization@altera.com

Note to Table:

(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

The following table shows the typographic conventions this document uses.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Indicate command names, dialog box titles, dialog box options, and other GUI labels. For example, **Save As** dialog box. For GUI elements, capitalization matches the GUI.
bold type	Indicates directory names, project names, disk drive names, file names, file name extensions, software utility names, and GUI labels. For example, **\qdesigns** directory, **D:** drive, and **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Indicate document titles. For example, *Stratix IV Design Guidelines*.
italic type	Indicates variables. For example, *n* + 1. Variable names are enclosed in angle brackets (< >). For example, *<file name>* and *<project name>***.pof** file.
Initial Capital Letters	Indicate keyboard keys and menu names. For example, the Delete key and the Options menu.
"Subheading Title"	Quotation marks indicate references to sections within a document and titles of Quartus II Help topics. For example, "Typographic Conventions."
`Courier type`	Indicates signal, port, register, bit, block, and primitive names. For example, `data1`, `tdi`, and `input`. The suffix `n` denotes an active-low signal. For example, `resetn`. Indicates command line commands and anything that must be typed exactly as it appears. For example, `c:\qdesigns\tutorial\chiptrip.gdf`. Also indicates sections of an actual file, such as a Report File, references to parts of files (for example, the AHDL keyword `SUBDESIGN`), and logic function names (for example, `TRI`).
↵	An angled arrow instructs you to press the Enter key.
1., 2., 3., and a., b., c., and so on	Numbered steps indicate a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ■ ■	Bullets indicate a list of items when the sequence of the items is not important.
	The hand points to information that requires special attention.
	A question mark directs you to a software help system with related information.
	The feet direct you to another document or website with related information.
	A caution calls attention to a condition or possible situation that can damage or destroy the product or your work.
	A warning calls attention to a condition or possible situation that can cause you injury.
	The envelope links to the Email Subscription Management Center page of the Altera website, where you can sign up to receive update notifications for Altera documents.