11. JTAG Boundary-Scan Testing in Arria II Devices

AIIGX51011-4.1

This chapter describes the boundary-scan test (BST) features that are supported in Arria® II devices and how to use the IEEE Std. 1149.1 and Std. 1149.6 BST circuitries in Arria II devices. The features are similar to Arria GX devices, unless stated in this chapter.

This chapter includes the following sections:

Arria II GX devices support IEEE Std. 1149.1 and IEEE Std. 1149.6, while Arria II GZ devices support IEEE Std. 1149.1 only. The IEEE Std. 1149.6 is only supported on the high-speed serial interface (HSSI) transceivers in Arria II GX devices. The IEEE Std. 1149.6 enables board-level connectivity checking between transmitters and receivers that are AC coupled (connected with a capacitor in series between the source and destination).

BST Architecture for Arria II Devices

For Arria II GX devices, the TDO output pin and all JTAG input pins are powered by the V_{CCIO} power supply of I/O Bank 8C, while for Arria II GZ devices, the TDO output pin and all the JTAG input pins are powered by 2.5-V/3.0-V V_{CCPD} supply of I/O Bank 1A. All user I/O pins are tri-stated during JTAG configuration.

For more information about the IEEE Std. 1149.1 BST architecture, BST circuitry, and boundary-scan register for Arria II devices, refer to the *IEEE 1149.1 (JTAG) Boundary-Scan Testing for Arria GX Devices* chapter in volume 2 of the *Arria GX Device Handbook*.

IEEE Std. 1149.6 Boundary-Scan Register for Arria II GX Devices

The boundary-scan cell (BSC) for HSSI transmitters (GXB_TX[p,n]) and receivers/input clock buffer (GXB_RX[p,n])/(REFCLK[0..7]) in Arria II GX devices are different from the BSCs for I/O pins.

Figure 11–1 shows the Arria II GX HSSI transmitter boundary-scan cell.

Figure 11–1. HSSI Transmitter BSC with IEEE Std. 1149.6 BST Circuitry for Arria II GX Devices

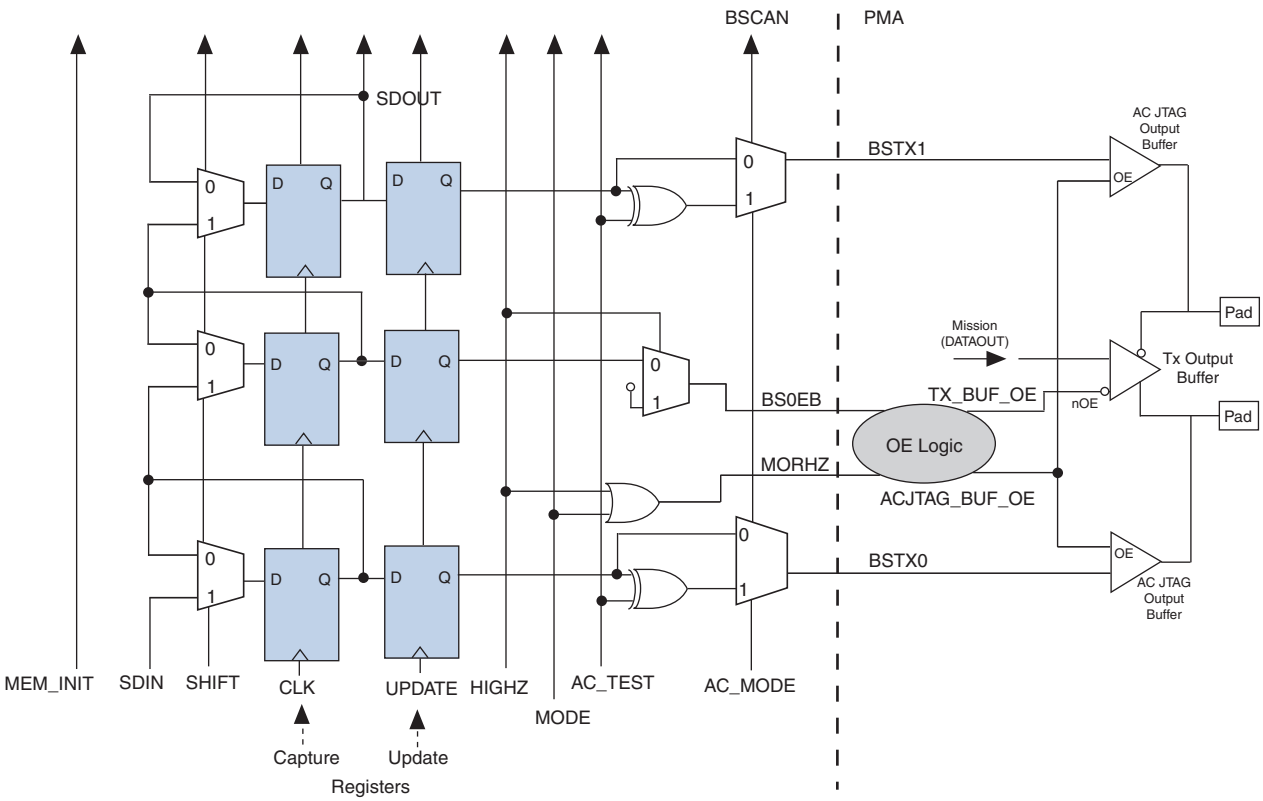
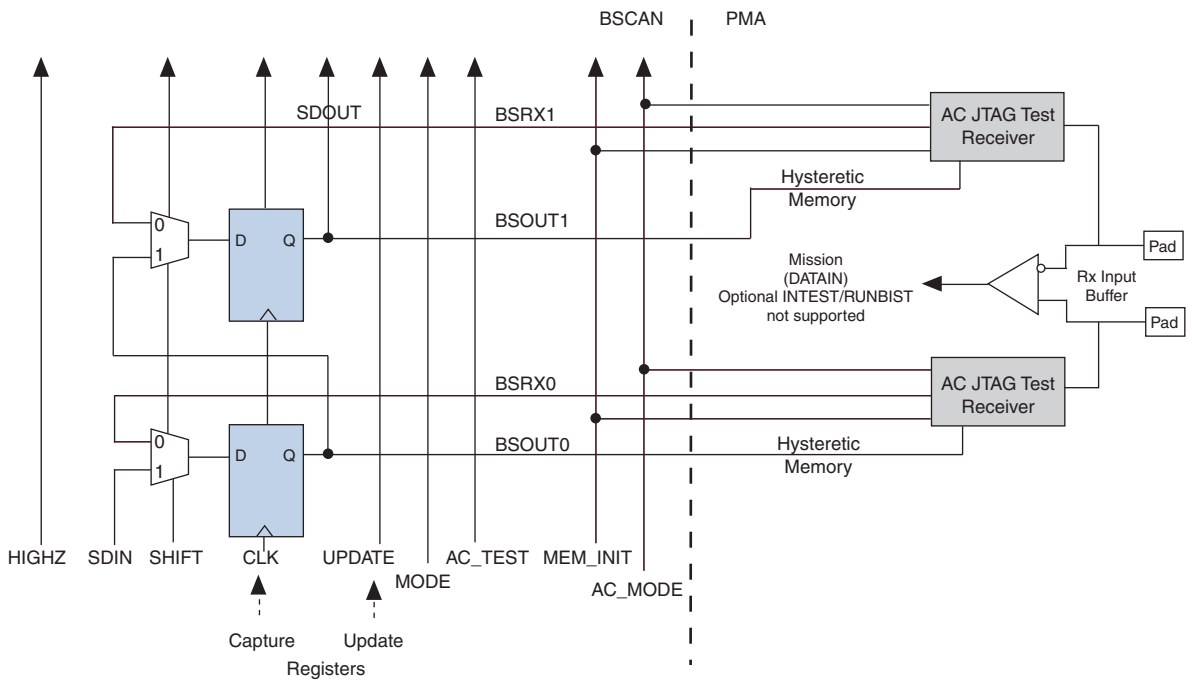


Figure 11–2 shows the Arria II GX HSSI receiver/input clock buffer BSC.

Figure 11–2. HSSI Receiver/Input Clock Buffer BSC with IEEE Std. 1149.6 BST Circuitry for Arria II GX Devices



BST Operation Control

Table 11–1 lists the boundary-scan register length for Arria II devices.

Table 11–1. Boundary-Scan Register Length for Arria II Devices

Device	Boundary-Scan Register Length
EP2AGX45	1,227
EP2AGX65	1,227
EP2AGX95	1,467
EP2AGX125	1,467
EP2AGX190	1,971
EP2AGX260	1,971
EP2AGZ225	2,274
EP2AGZ300	2,682
EP2AGZ350	2,682

Table 11–2 lists the IDCODE information for Arria II devices.

Table 11–2. 32-Bit IDCODE for Arria II Devices

Device	IDCODE (32 Bits) *(1)*			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	LSB (1 Bit) *(2)*
EP2AGX45	0000	0010 0101 0001 0010	000 0110 1110	1
EP2AGX65	0000	0010 0101 0000 0010	000 0110 1110	1
EP2AGX95	0000	0010 0101 0001 0011	000 0110 1110	1
EP2AGX125	0000	0010 0101 0000 0011	000 0110 1110	1
EP2AGX190	0000	0010 0101 0001 0100	000 0110 1110	1
EP2AGX260	0000	0010 0101 0000 0100	000 0110 1110	1
EP2AGZ225	0000	0010 0100 1000 0001	000 0110 1110	1
EP2AGZ300	0000	0010 0100 0000 1010	000 0110 1110	1
EP2AGZ350	0000	0010 0100 1000 0010	000 0110 1110	1

Notes to Table 11–2:

(1) The MSB is on the left.

(2) The IDCODE LSB is always 1.

If the device is in the RESET state, when the nCONFIG or nSTATUS signal is low, the device IDCODE might not be read correctly. To read the device IDCODE correctly, you must issue the IDCODE JTAG instruction only when the nSTATUS signal is high.

For information about JTAG instructions, TAP controller state machine, timing requirements, and how to select the instruction mode, refer to "IEEE Std. 1149.1 BST Operation Control" in the *IEEE 1149.1 (JTAG) Boundary-Scan Testing for Arria GX Devices* chapter in volume 2 of the *Arria GX Device Handbook*.

For Arria II GX devices, IEEE Std.1149.6 mandates the addition of two new instructions: EXTEST_PULSE and EXTEST_TRAIN. These two instructions enable edge-detecting behavior on the signal path containing the HSSI pins. These instructions implement new test behaviors for HSSI pins and simultaneously behave identically to the IEEE Std. 1149.1 EXTEST instruction for non-HSSI pins.

EXTEST_PULSE Instruction Mode

The instruction code for EXTEST_PULSE is 0010001111. The EXTEST_PULSE instruction generates three output transitions:

- Driver drives the data on the falling edge of TCK in UPDATE_IR/DR.
- Driver drives the inverted data on the falling edge of TCK after entering the RUN_TEST/IDLE state.
- Driver drives the data on the falling edge of TCK after leaving the RUN_TEST/IDLE state.

If you use DC-coupling on the HSSI signals, you must execute the EXTEST instruction. If you use AC-coupling on the HSSI signals, you must execute the EXTEST_PULSE instruction. AC-coupled and DC-coupled HSSI are only supported in post-configuration mode.

EXTEST_TRAIN Instruction Mode

The instruction code for EXTEST_TRAIN is 0001001111. The EXTEST_TRAIN instruction behaves like the EXTEST_PULSE instruction with one exception: the output continues to toggle on the TCK falling edge as long as the TAP controller is in the RUN_TEST/IDLE state.

These two instruction codes are only supported in post-configuration mode for Arria II GX devices.

You must not use the following private instructions as invoking such instructions potentially damage the device, rendering the device useless:

- 1100010000
- 0011100101
- 0011001001
- 1100010011
- 0011100110
- 0000101010

You must take precaution not to invoke such instructions at any instance. Altera recommends that you avoid toggling the JTAG pins when the device is not in used.

I/O Voltage Support in a JTAG Chain

The JTAG chain can support several different devices. However, use caution if the chain contains devices that have different V_{CCIO} levels. The output voltage level of the TDO pin must meet the specification of the TDI pin it drives.

Table 11–3 and Table 11–4 show board design recommendations to ensure proper JTAG chain operation.

Table 11–3. Supported TDO/TDI Voltage Combinations for Arria II GX Devices (Part 1 of 2)

Device	TDI Input Buffer Power	Arria II GX TDO V_{CCIO} Voltage Level in I/O Bank 8C				
		V_{CCIO} = 3.3 V *(1)*	V_{CCIO} = 3.0 V *(1)*	V_{CCIO} = 2.5 V *(2)*	V_{CCIO} = 1.8 V	V_{CCIO} = 1.5 V
Arria II GX	V_{CCIO} = 3.3 V	✓	✓	✓	✓ *(3)*	Level shifter required
	V_{CCIO} = 3.0 V	✓	✓	✓	✓ *(3)*	Level shifter required
	V_{CCIO} = 2.5 V	✓	✓	✓	✓ *(3)*	Level shifter required
	V_{CCIO} = 1.8 V	✓	✓	✓	✓ *(3)*	Level shifter required
	V_{CCIO} = 1.5 V	✓	✓	✓	✓ *(3)*	✓

Table 11–3. Supported TDO/TDI Voltage Combinations for Arria II GX Devices (Part 2 of 2)

Device	TDI Input Buffer Power	Arria II GX TDO V_{CCIO} Voltage Level in I/O Bank 8C				
		V_{CCIO} = 3.3 V *(1)*	V_{CCIO} = 3.0 V *(1)*	V_{CCIO} = 2.5 V *(2)*	V_{CCIO} = 1.8 V	V_{CCIO} = 1.5 V
Non-Arria II GX	V_{CC} = 3.3 V	✓	✓	✓	✓ *(3)*	Level shifter required
	V_{CC} = 2.5 V	✓ *(4)*	✓ *(4)*	✓	✓ *(3)*	Level shifter required
	V_{CC} = 1.8 V	✓ *(4)*	✓ *(4)*	✓ *(5)*	✓	Level shifter required
	V_{CC} = 1.5 V	✓ *(4)*	✓ *(4)*	✓ *(5)*	✓ *(6)*	✓

Notes to Table 11–3:

(1) The TDO output buffer meets V_{OH} (Min) = 2.4 V.
(2) The TDO output buffer meets V_{OH} (Min) = 2.0 V.
(3) An external 250-Ω pull-up resistor is not required; however, they are recommended if signal levels on the board are not optimal.
(4) The input buffer must be 3.0-V tolerant.
(5) The input buffer must be 2.5-V tolerant.
(6) The input buffer must be 1.8-V tolerant.

Table 11–4. Supported TDO/TDI Voltage Combinations for Arria II GZ Devices

Device	TDI Input Buffer Power	Arria II GZ TDO V_{CCPD} Voltage Level in I/O Bank 1A	
		V_{CCPD} = 3.0 V *(1)*	V_{CCPD} = 2.5 V *(2)*
Arria II GZ	V_{CCPD} = 3.0 V	✓	✓
	V_{CCPD} = 2.5 V	✓	✓
Non-Arria II GZ	V_{CC} = 3.3 V	✓	✓
	V_{CC} = 2.5 V	✓ *(3)*	✓
	V_{CC} = 1.8 V	✓ *(3)*	✓ *(4)*
	V_{CC} = 1.5 V	✓ *(3)*	✓ *(4)*

Notes to Table 11–4:

(1) The TDO output buffer meets V_{OH} (Min) = 2.4 V.
(2) The TDO output buffer meets V_{OH} (Min) = 2.0 V.
(3) The input buffer must be 3.0-V tolerant.
(4) The input buffer must be 2.5-V tolerant.

For more information about I/O voltage support in the JTAG chain, refer to the "I/O Voltage Support in JTAG Chain" in the *IEEE 1149.1 (JTAG) Boundary-Scan Testing for Arria GX Devices* chapter in volume 2 of the *Arria GX Device Handbook*.

Disabling IEEE Std. 1149.1 BST Circuitry

The IEEE Std. 1149.1 BST circuitry for Arria II devices is enabled after device power up. Because the IEEE Std. 1149.1 BST circuitry is used for BST or in-circuit reconfiguration, you must enable the circuitry only at specific times as mentioned in "IEEE Std. 1149.1 BST Circuitry" in the *IEEE 1149.1 (JTAG) Boundary-Scan Testing for Arria GX Devices* chapter in volume 2 of the *Arria GX Device Handbook*.

If you do not use the IEEE Std. 1149.1 circuitry in Arria II devices, permanently disable the circuitry to ensure that you do not inadvertently enable it when it is not required.

Table 11–5 lists the pin connections necessary for disabling the IEEE Std. 1149.1 circuitry in Arria II devices.

Table 11–5. Pin Connections Necessary for Disabling IEEE Std. 1149.1 Circuitry for Arria II Devices

JTAG Pins	Connection for Disabling	
	Arria II GX Devices	Arria II GZ Devices
TMS	V_{CC} supply of Bank 8C	V_{CCPD} supply of Bank 1A
TCK	GND	
TDI	V_{CC} supply of Bank 8C	V_{CCPD} supply of Bank 1A
TDO	Leave Open	
TRST	Not available	GND

Boundary-Scan Description Language Support

The boundary-scan description language (BSDL), a subset of VHDL, provides a syntax that allows you to describe the features of an IEEE Std. 1149.6 BST-capable device that can be tested. You can test software development systems, then use the BSDL files for test generation, analysis, and failure diagnostics.

For more information about BSDL files for IEEE Std. 1149.6-compliant Arria II GX devices, refer to the IEEE 1149.6 BSDL Files page on the Altera® website.

For more information about BSDL files for IEEE Std. 1149.1-compliant Arria II GZ devices, refer to the IEEE 1149.1 BSDL Files page on the Altera website.

You can also generate BSDL files (pre-configuration and post-configuration) for Arria II devices with the Quartus® II software version 9.1 and later. For the procedure to generate BSDL files using the Quartus II software, refer to Generating BSDL Files in Quartus II.

Document Revision History

Table 11–6 lists the revision history for this document.

Table 11–6. Document Revision History

Date	Version	Changes
December 2013	4.1	Updated the "EXTEST_PULSE Instruction Mode" section.
December 2010	4.0	■ Updated for the Quartus II software version 10.1 release. ■ Added Arria II GZ devices information. ■ Added "BST Architecture for Arria II Devices" and "Disabling IEEE Std. 1149.1 BST Circuitry" sections. ■ Added Table 11–3 and Table 11–5. ■ Updated Table 11–1 and Table 11–2. ■ Minor text edits.
July 2010	3.0	Updated for Arria II GX v10.0 release: ■ Updated "BST Operation Control" section. ■ Minor text edits.
November 2009	2.0	Updated for Arria II GX v9.1 release: ■ Updated Table 11–1 and Table 11–2. ■ Updated "I/O Voltage Support in a JTAG Chain" section. ■ Minor text edits.
February 2009	1.0	Initial release.