Errata Sheet for HardCopy III Devices

This errata sheet provides updated information about known Stratix® III device issues affecting HardCopy® III devices.

Table 1 lists specific Stratix III issues and which HardCopy III devices are affected by each issue.

Table 1. Stratix III Device Issues Affecting HardCopy III Devices (Part 1 of 3) ***(Note 1)***

Known Stratix III Issue	Affected Stratix III Devices	Stratix III Planned Fix	HardCopy III Affected?
"PCI 66 MHz Timing Closure" The PCI 66 MHz interface in the HardCopy device will not close timing if the column IOs (top/bottom) are used.	None	—	Yes
"PLL phasedone Signal Stuck at Low" In some cases, the HardCopy III phase-locked loop (PLL) blocks exhibit the `phasedone` signal stuck at low during the PLL dynamic phase shift.	All Stratix III (ES and production) devices	Quartus II software version 12.0 and later	Yes
"Higher Power Supply Current During Power-Up for VCCPD" Higher power-up current requirements are needed for V_{CCPD} supply.	None	—	Yes
Error Detection CRC feature, when enabled, may cause the MLAB RAM blocks to operate incorrectly.	All Stratix III Devices	■ EP3SL50 Revision G ■ EP3SL70 Revision F ■ EP3SL110 Revision I ■ EP3SL150 Revision H ■ EP3SL200 Revision G ■ EP3SL340 Revision E ■ EP3SE50 Revision D ■ EP3SE80 Revision G ■ EP3SE110 Revision F ■ EP3SE260 Revision F	No
Remote System Upgrade feature fails when loading an invalid application configuration image.	All Stratix III Devices	—	No
The CRC error injection feature may not operate correctly.	All Stratix III Devices	—	No

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Table 1. Stratix III Device Issues Affecting HardCopy III Devices (Part 2 of 3) ***(Note 1)***

Known Stratix III Issue	Affected Stratix III Devices	Stratix III Planned Fix	HardCopy III Affected?
MLAB final timing models were updated post Quartus® II Software version 8.1. Only a subset of designs using MLAB blocks is affected. See the information in the second paragraph of "Updated MLAB Final Timing Model (Affecting a Subset of MLAB Designs)"	■ EP3SL110 ■ EP3SL150 ■ EP3SL340 ■ EP3SE110 ■ EP3SE80	—	No
LVDS final timing models were updated post Quartus II Software version 8.1.	All Stratix III Devices	—	No
Dynamic phase alignment (DPA) circuitry in Stratix III devices might get stuck at the initial configured phase or move to the optimum phase after a longer than expected period of time.	All Stratix III Devices	—	No
VCCPT Power-Up Issue. Device may fail to power-up successfully.	All Stratix III Devices	—	No
CRC_ERROR may toggle unexpectedly in user mode without detecting an actual SEU.	All Stratix III Devices	—	No
M9K and M144K RAM blocks can be put into a locked, inactive state when driven by a clock with a very narrow pulse (for example, a glitch).	All Stratix III Devices	—	Yes
Stratix III devices can fail the JTAG configuration in certain positions of the JTAG chain, depending on the setup conditions.	■ 3SL150 Revision B and earlier ■ 3SE50 / L70/E110 / E260/L340 Revision A	■ 3SL150 Revision C ■ 3SE50 / L70 / E110 / E260 / L340 Revision B ■ EP3SL200 ■ EP3SL110 ■ EP3SL50 ■ EP3SE80	No
Interface timing issues with the LVDS hard macro.	All Stratix III devices	All Stratix III devices	No
The dynamic phase alignment (DPA) lock signal (rx_dpa_locked) does not assert on some channels during link initialization.	All Stratix III devices	All Stratix III devices	No
The DPA circuit in the EP3SL150 ES devices fails to lock, and data is corrupted at data rates of 150 bps to 385 Mbps and data rates above 622 Mbps.	EP3SL150 ES devices	EP3SL150 production devices	No
Analog-to-digital converter (ADC) for temperature sensing diode (TSD) no longer supported.	All Stratix III ES and production devices	—	No

Table 1. Stratix III Device Issues Affecting HardCopy III Devices (Part 3 of 3) ***(Note 1)***

Known Stratix III Issue	Affected Stratix III Devices	Stratix III Planned Fix	HardCopy III Affected?
TSD must have V_{CCPT} powered on to operate.	■ Revision A of EP3SE50, EP3SL70, EP3SE110, EP3SE260, EP3SL340 ■ Revisions A and B of EP3SL150 devices	Future revisions of the affected Stratix III devices	No
Device may enter power-on reset (POR) during reconfiguration cycle.	■ Revision A of EP3SE50, EP3SL70, EP3SE110, EP3SE260, EP3SL340 ■ Revisions A and B of EP3SL150 devices	Future revisions of the affected Stratix III devices	No
Write speed decrease for M144K blocks in certain modes.	■ Revision A of EP3SE50, EP3SL70, EP3SE110, EP3SE260, EP3SL340 ■ Revisions A and B of EP3SL150 devices	Future revisions of the affected Stratix III devices	No
MLAB RAM block size changed from 64 x 10 or 32 x 20 (640 bits) to 16 x 20 (320 bits).	All Stratix III ES and production devices	—	No
The TSD is not backwards compatible with Stratix II devices.	EP3SL150 ES devices	EP3SL150 production devices	No
Extra I_{CCL} current in user mode.	EP3SL150 ES devices	EP3SL150 production devices	No
DPA fails to lock in some cases.	EP3SL150 ES devices	EP3SL150 production devices	No

Note to Table 1:

(1) Refer to the Errata Sheet for Stratix III Devices for details and solutions of the issue where applicable.

PCI 66 MHz Timing Closure

The PCI 66 MHz interface in the HardCopy III device will not close timing if the column (top/bottom) IO pins are used. To close timing on the PCI 66 MHz interface, the PCI 66 MHz clock must drive the periphery clock (PCLK) network, which can only be driven from the row (left/right) IO pins. Ensure that you assign this PCI clock to a row IO pin that has direct access to the PCLK network.

Additionally, you must provide external off-chip clamping diodes because the row IOs do not support on-chip clamping diodes. HardCopy III customers will require FPGA/HardCopy board modifications to accommodate the external clamping diodes.

The HardCopy III device will not meet timing even if the Quartus II version 10.1 or earlier compilation may show that the PCI 66 MHz interface related paths meet the core timing.

The Quartus II software version 11.1 is the minimum software version for handoff.

The above are general guidelines and may not work under all conditions. If you plan to use the PCI 66 MHz interface in your HardCopy III design, contact Altera® Technical Support at www.altera.com/mysupport for more information.

There is no planned issue fix for HardCopy III devices.

PLL phasedone Signal Stuck at Low

In some cases, the HardCopy III PLL blocks exhibit the `phasedone` signal stuck at low during the PLL dynamic phase shift. When the PLL `phasedone` signal is stuck at low, the intended phase shift does not happen. You can recover from the PLL `phasedone` signal being stuck at low by resetting the PLL or by restarting the phase shift operation by asserting the `phasestep` signal.

To resolve the PLL `phasedone` signal stuck at low issue, the Altera PLL megafunction is enhanced to automatically restart the phase shift operation internally in the Altera PLL megafunction whenever the PLL `phasedone` signal is stuck at low. Restarting the phase shift operation compensates for the missing phase shift operation and also recovers the `phasedone` signal.

This Altera PLL megafunction solution will be implemented in the Quartus II software version 12.0 and later. Altera recommends upgrading to the latest Quartus II software, regenerating the PLL megafunction, and recompiling your design.

Additionally, software patches are available for the Quartus II software versions 9.1 SP2 and 10.1 SP1 to upgrade the PLL megafunction with the solution. To download and install the Quartus II software patch, refer to the PLL Phasedone Stuck at Low Solution.

If you need additional support, file a service request using mySupport.

Higher Power Supply Current During Power-Up for V_{CCPD}

Description

HardCopy III devices require higher power-up current levels for the V_{CCPD} power supply than previously specified. The Quartus® II software and PowerPlay Early Power Estimator (EPE) version 9.1SP2 and later versions correctly show the V_{CCPD} power-on current for production devices.

HardCopy III functionality is not affected by this issue, even if your V_{CCPD} power supply is designed with output current levels below what the Quartus II software and/or EPE specify. HardCopy III devices will power-up and operate correctly as expected, provided the supplies power up monotonically and the minimum voltage requirement is met. V_{CCPD} must meet the minimum power supply voltage requirement for the device to exit power-on reset (POR). After the device exits POR, the V_{CCPD} current requirements return to what is reported by Altera's power estimation tools. Overall thermal power and operating current levels are not affected by this issue.

Workaround

If there are other devices on the board that share the V_{CCPD} power supply, you can use the Quartus II software and/or the EPE to estimate power supply current requirements. This analysis may be needed if the other devices on the board have stringent power supply integrity requirements.

There is no planned fix for the higher power-up current requirements.

Document Revision History

Table 2 lists the revision history for this Errata Sheet.

Table 2. Document Revision History

Date	Version	Changes
February 2012	1.1	■ Added the "PCI 66 MHz Timing Closure" section. ■ Added the "PLL phasedone Signal Stuck at Low" section.
March 2011	1.0	Initial release.