SGMII Interface Implementation Using Soft CDR Mode of Altera FPGAs

2013.10.17

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The Serial Gigabit Media Independent Interface (SGMII) protocol provides connectivity between the physical layer (PHY) and the Ethernet media controller (MAC). The SGMII solution for Altera® FPGAs allows you to implement multiport Gbps Ethernet (GbE) systems with high port counts, low power, and low cost requirements.

The LVDS hard macros in the soft clock data recover (CDR) mode and Triple-Speed Ethernet MegaCore® implement the physical coding sublayer (PCS) and media access control (MAC) function for Altera FPGAs. You can use the soft CDR mode to implement SGMII systems in the following Altera FPGAs:

- Stratix® V, Stratix IV, and Stratix III
- Arria® V, and Arria II

A typical SGMII implementation uses 16 to 48 full-duplex links. With the sufficient number of transmitters and receivers in Altera FPGAs, you can implement multiple full-duplex channels. In such dense applications, the LVDS I/O standard is preferred because of its low-voltage differential signaling capability. You can implement the following SGMII connectivity with Altera FPGAs:

- Transmit side—using LVDS hard macros.
- Receive side—using LVDS hard macros configures in soft CDR mode.

Related Information

- **Serial-GMII Specification Revision 1.8**
  Cisco System's proprietary specification document for SGMII.
- **High-Speed Differential I/O Interfaces and DPA in Stratix V Devices**
- **High Speed Differential I/O Interfaces with DPA in Stratix IV Devices**
- **High-Speed Differential I/O Interfaces with DPA in Stratix III Devices**
- **High-Speed Differential I/O Interfaces and DPA in Arria V Devices**
- **High-Speed Differential I/O Interfaces and DPA in Arria II Devices**

Interfacing MAC and PHY Through SFP Transceiver

Among the wide support for interfacing with other devices on a typical line card, the Altera FPGAs provide connectivity between the following modules:

- GbE port—a small form factor pluggable optical or copper (SFP) transceiver
- Host processor
- Backplane driver

Figure 1: SGMII Connectivity Using an Altera FPGA through Optical SFP Transceiver

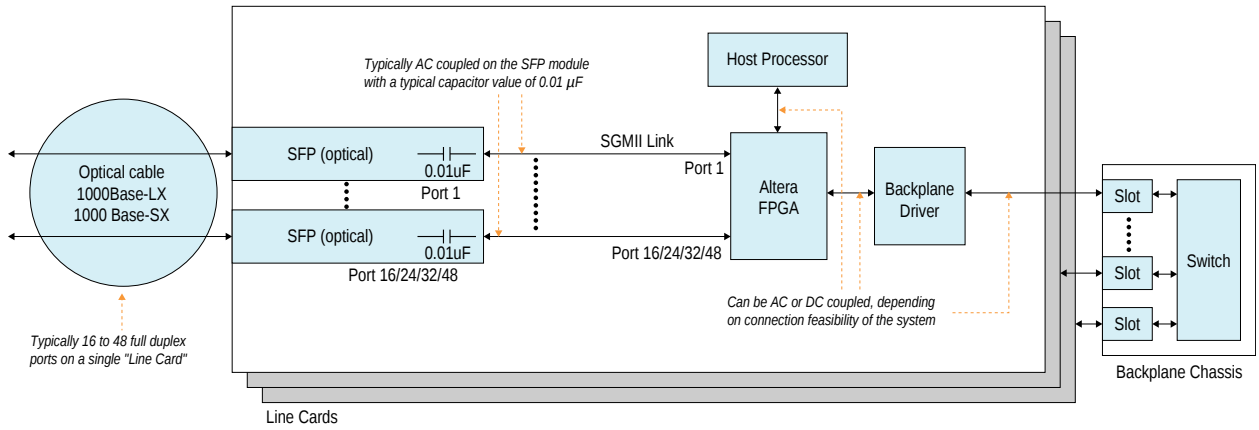
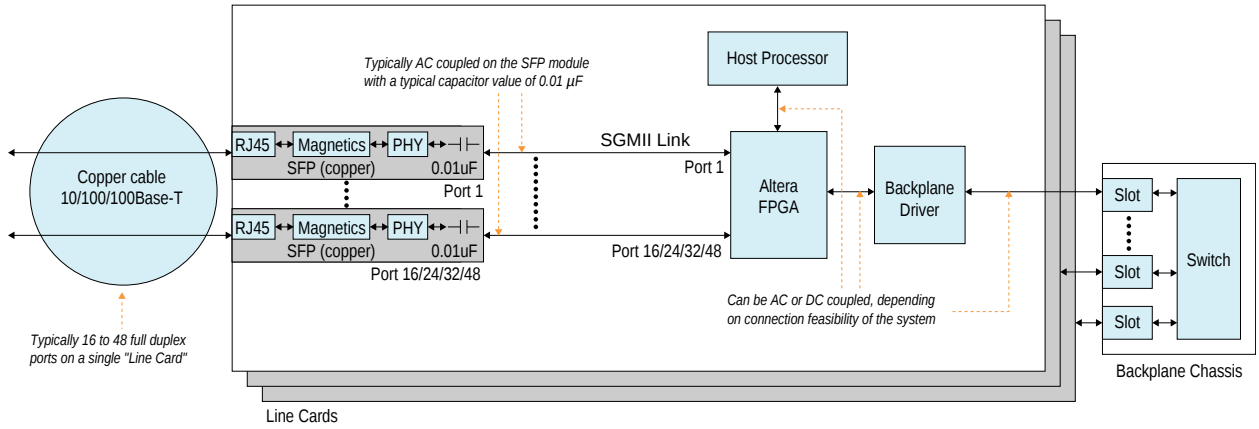


Figure 2: SGMII Connectivity Using an Altera FPGA through Copper SFP Transceiver

The PHY device is part of the copper SFP module. The copper SFP module retimes the data to enable interoperability.



Related Information

- **Small Form-factor Pluggable (SFP) Transceiver MultiSource Agreement (MSA)**
  Provides more information about the SFP transceiver specification.
- **Interfacing 3.3 V LVPECL to 2.5 V LVDS (SFP Module to Altera FPGA)** on page 3

Interfacing 3.3 V LVPECL to 2.5 V LVDS (SFP Module to Altera FPGA)

The optical or copper SFP modules are typically AC coupled on the SGMII side of the interface. This AC coupling is present within the SFP modules.

In the LVPECL-to-LVDS interface, the on-chip termination (OCT) on the FPGA LVDS receiver is disabled.

Altera recommends that you implement a resistor network that can raise the common mode voltage for the LVDS receiver. This is because the output swing of the LVPECL transmitter on the SFP and the input amplitude sustainable by the LVDS receiver on the FPGA are not compatible.

Figure 3: LVPECL-to-LVDS (3.3 V SFP to 2.5 V FPGA)

This figure shows a resistor network example to raise the common mode voltage for the LVDS receiver. The example assumes that the signal going out of SFP module is AC coupled and the trace impedance between the two devices is 50 Ω single-ended.

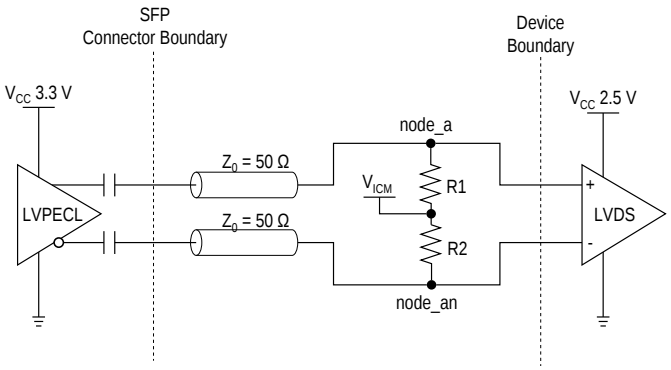
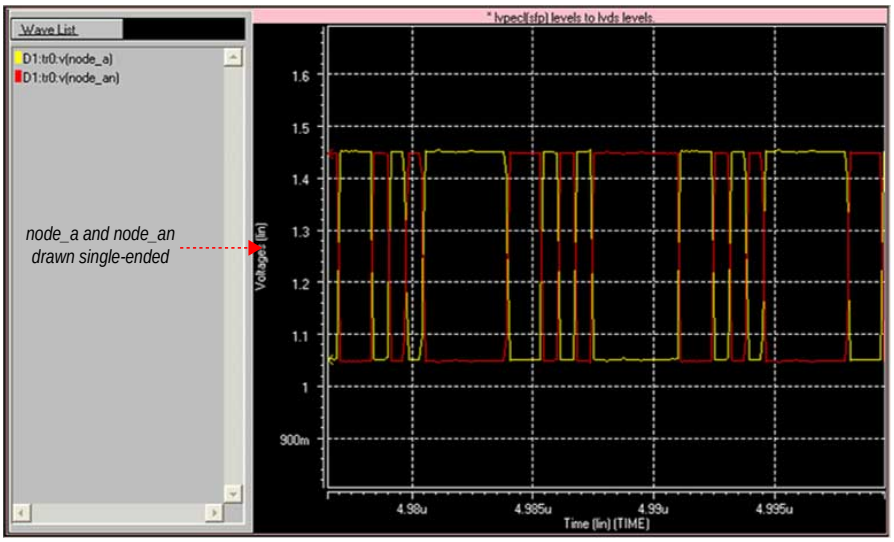


Figure 4: LVPECL-to-LVDS HSPICE Simulation Results

This figure shows the simulation results where the resistor network raises the common mode voltage of the signal incoming to the FPGA LVDS receiver to V_{ICM}. The V_{ICM} is set to 1.25 V to match the input common mode voltage range of the receiver. The value of the resistors are 50 Ω each.



Related Information

- Stratix V Device Datasheet
- DC and Switching Characteristics for Stratix IV Devices
- DC and Switching Characteristics of Stratix III Devices
- Arria V Device Datasheet
- Device Datasheet for Arria II Devices

Interfacing 2.5 V LVDS to 3.3 V LVPECL (Altera FPGA to SFP Module)

In the LVDS-to-LVPECL interface, you do not need a resistor network. This is because the SFP receiver LVPECL input voltage and input common mode voltage tolerances on the SFP receiver are greater than the maximum LVDS output amplitude and output common mode voltage on the transmitter FPGA.

The following conditions are assumed:

- The FPGA LVDS transmitter is operating at maximum output voltage settings with maximum pre-emphasis.
- The SFP module in the interface is AC coupled, as typically set for connectors in SGMII systems.

Related Information

- Stratix V Device Datasheet
- DC and Switching Characteristics for Stratix IV Devices
- DC and Switching Characteristics of Stratix III Devices

- **Arria V Device Datasheet**
- **Device Datasheet for Arria II Devices**
- **Programmable V_{OD} and Programmable Pre-Emphasis** on page 15
  Provides instructions to set the LVDS settings in Altera FPGAs.

Interfacing PCML to 2.5 V LVDS (Altera FPGA to Altera FPGA)

In the PCML-to-LVDS interface, you do not need a resistor network if DC coupling is supported between the PCML transmitter and the LVDS receiver in the FPGA. In this interface, you can enable OCT on the LVDS receiver.

Adjust the output amplitude of the PCML transmitter device so that the signal amplitude at the input of the LVDS receiver is within the input voltage specification. For the device-specific switching characteristics and supported I/O standards of the PCML transmitter and LVDS receiver refer to the relevant device datasheet.

Related Information

- **Stratix V Device Datasheet**
- **DC and Switching Characteristics for Stratix IV Devices**
- **DC and Switching Characteristics of Stratix III Devices**
- **Arria V Device Datasheet**
- **Device Datasheet for Arria II Devices**

Interfacing 2.5 V LVDS to LVDS (Altera FPGA to Altera FPGA)

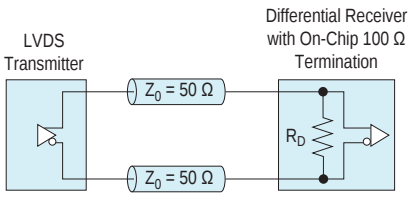
In the LVDS-to-LVDS interface, you do not need a resistor network. This is because AC or DC coupling is supported between the LVDS transmitter and LVDS receiver.

Configure the receiver FPGA for LVDS I/O standards with the proper input common mode voltage and input signal amplitude range. For the input common mode voltage and input signal amplitude requirement, refer to the relevant device datasheet.

For example, if the receiver is a Stratix II GX FPGA, configure the receiver to the LVDS I/O standard with input common mode voltage of 1.2 V. The input signal amplitude range of the Stratix II GX FPGA is 100 mV to 900 mV, single-ended.

In the LVDS-to-LVDS interface, enable OCT on the LVDS receiver FPGA. Altera FPGAs provide a 100 Ω differential OCT option on each differential receiver channel for LVDS I/O standards.

Figure 5: On-Chip Differential I/O Termination



Related Information

- Stratix V Device Datasheet
- DC and Switching Characteristics for Stratix IV Devices
- DC and Switching Characteristics of Stratix III Devices
- Arria V Device Datasheet
- Device Datasheet for Arria II Devices

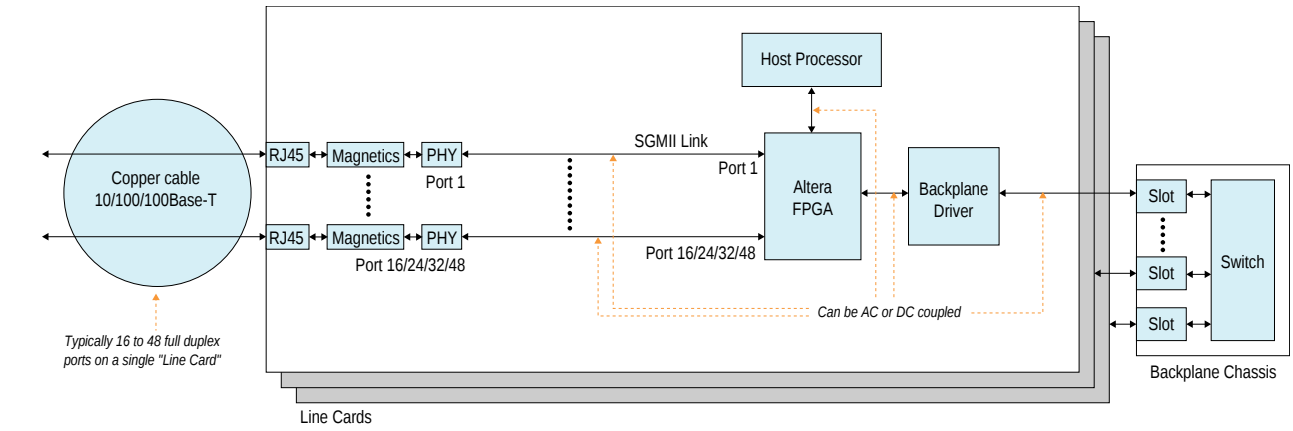
Interfacing 2.5 LVDS to LVDS (Altera FPGA to LVDS Device)

The Altera LVDS interface is compatible with the LVDS I/O standards of third-party devices. For information and specifications, refer to the documentation provided by the specific device vendor.

Interfacing MAC and PHY without SFP Transceiver

Altera FPGAs can interface with RJ45 device through a PHY device. This interface link can be AC or DC coupled, as shown in the following figure.

Figure 6: SGMII Connectivity using Altera FPGA without SFP Transceiver



Receiver Data Path Modes for SGMII in Altera FPGAs

You can configure the built-in serializer/deserializer (SERDES) circuitry in Altera FPGAs to support source-synchronous and asynchronous serial data communication for SGMII interfaces.

You can achieve data communication for SGMII interfaces using the soft CDR and DPA modes in the receiver data path.

Table 1: Typical SGMII System Scenarios

Receiver Data Path Mode	Description
Soft CDR mode in asynchronous systems	• No source-synchronous clock is sent with the data channels from the upstream transmitter. • The upstream transmitter and receiver nodes use reference clocks from two different sources. This causes a potential parts per million (ppm) difference between the upstream transmitter and receiver nodes. • The maximum ppm difference allowed between the two clock sources is ±100 ppm. • An asynchronous system is typically used for chip-to-chip or board-to-board communication with an optional backplane.
Soft CDR mode in synchronous systems	• No source-synchronous clock is sent with the data channels from the upstream transmitter. • The upstream transmitter and receiver nodes use reference clocks from the same source.
Source-synchronous mode	• A source-synchronous clock is sent with the data channels. • The receiver nodes use the source-synchronous clock to recover the received data.

Configuring ALTLVDS_TX Megafunction for the LVDS Transmitter

Use the MegaWizard Plug-in Manager in the Quartus II software to create a new custom variation of the LVDS transmitter and configure it for SGMII implementation.

Note: If you instantiate a single channel SGMII transmitter instance multiple times to create a multichannel SGMII interface, the Quartus II software automatically selects the same PLL to drive these multiple instances if the same reference clock source is shared.

Table 2: Specific ALTLVDS_TX Megafunction Settings for SGMII Implementation

This table lists the specific options and settings required for SGMII implementation on the transmitter.

Option	Instruction
Which megafunction would you like to customize?	Expand **I/O** and select **ALTLVDS_TX**.
What is the number of Channels?	Select the number of channels.
What is the deserialization factor?	Select **10**.
What is the output data rate?	Type `1250`.
Specify the input clock rate by	Select clock frequency of **125** MHz.

Option	Instruction
Use shared PLL(s) for receivers and transmitters	Turn on if you want to share the PLLs to both the transmitter and receiver instances. Sharing the PLLs is allowed for transmitters and receivers on the same side of the device.
Use 'tx_outclock' output port	Turn off if you are using a synchronous/asynchronous system (receiver in soft-CDR mode).
What is the outclock divide factor (B)?	Select the divide factor so that the output clock frequency is within the device specification. This option is applicable if you turn on **Use 'tx_outclock' output port**.

1. Open the **MegaWizard Plug-In Manager**.
2. Create a new custom variation of the ALTLVDS_TX megafunction.
3. Navigate through the **MegaWizard Plug-In Manager** and specify all necessary options and settings for your design.
   Refer to **Table 2**.

Related Information

LVDS SERDES Transmitter/Receiver (ALTLVDS_RX/TX) Megafunction User Guide
Provides more details about the ALTLVDS_TX and ALTLVDS_RX megafunctions.

Configuring ALTLVDS_RX Megafunction for the LVDS Receiver

Use the MegaWizard Plug-in Manager in the Quartus II software to create a new custom variation of the LVDS receiver and configure it for SGMII implementation.

Note: If you instantiate a single channel SGMII transmitter instance multiple times to create a multichannel SGMII interface, the Quartus II software automatically selects the same PLL to drive these multiple instances if the same reference clock source is shared.

Table 3: Specific ALTLVDS_RX Megafunction Settings for SGMII Implementation

This table lists the specific options and settings required for SGMII implementation on the receiver.

The ppm value for **What is the simulated recovered clock phase drift?** option in the ALTLVDS_RX megafunction is used only for simulation purposes and has no significance in the real hardware.

Option	Instruction
Which megafunction would you like to customize?	Expand **I/O** and select **ALTLVDS_RX**.
Enable Dynamic Phase Alignment mode	Turn on.
What is the number of Channels?	Select the number of channels.
What is the deserialization factor?	Select **10**.
What is the input data rate?	Type `1250`.

Option	Instruction
Specify the input clock rate by	Select clock frequency of **125** MHz.
Use shared PLL(s) for receivers and transmitters	Turn on if you want to share the PLLs to both the transmitter and receiver instances. Sharing the PLLs is allowed for transmitters and receivers on the same side of the device.
Use 'rx_divfwdclk' output port and bypass the DPA FIFO	Turn on to select soft CDR mode.
Use 'rx_reset' input port	Turn on. In soft CDR mode, it is not necessary to use the `rx_dpa_locked` output port.
Use a DPA initial phase selection of	Optional. Turn on if required by your design and select the degree of phase selection.
Use 'rx_channel_data_align' input port	Turn on.
After how many pulses does the data alignment circuitry restore the serial data latency back to 0?	Select **10**.
Use 'rx_cda_reset' input port	Optional. Turn on as a reset to the data realignment (bit-slip) circuitry.

1. Open the **MegaWizard Plug-In Manager**.
2. Create a new custom variation of the ALTLVDS_RX megafunction.
3. Navigate through the **MegaWizard Plug-In Manager** and specify all necessary options and settings for your design.

   Refer to **Table 3**.

Related Information

LVDS SERDES Transmitter/Receiver (ALTLVDS_RX/TX) Megafunction User Guide
Provides more details about the ALTLVDS_TX and ALTLVDS_RX megafunctions.

Soft CDR Clocking Scheme for SGMII Implementation

There are PLLs on different sides of the device. If you use only one side of the FPGA to implement all your SGMII LVDS interfaces, you need only one PLL.

Figure 7: SGMII Clocking Scheme for Soft-CDR Mode

This diagram shows an example SGMII system implemented on an Altera evaluation board with the Altera Triple-Speed Ethernet MegaCore using an LVDS hard macro configured as soft-CDR:

- The transmitter and receiver at the upstream and downstream node use a shared PLL.
- Typically, the reference clock sources for transmitter and receiver use 125 MHz/62.5 MHz with ppm tolerance of ±100 ppm.

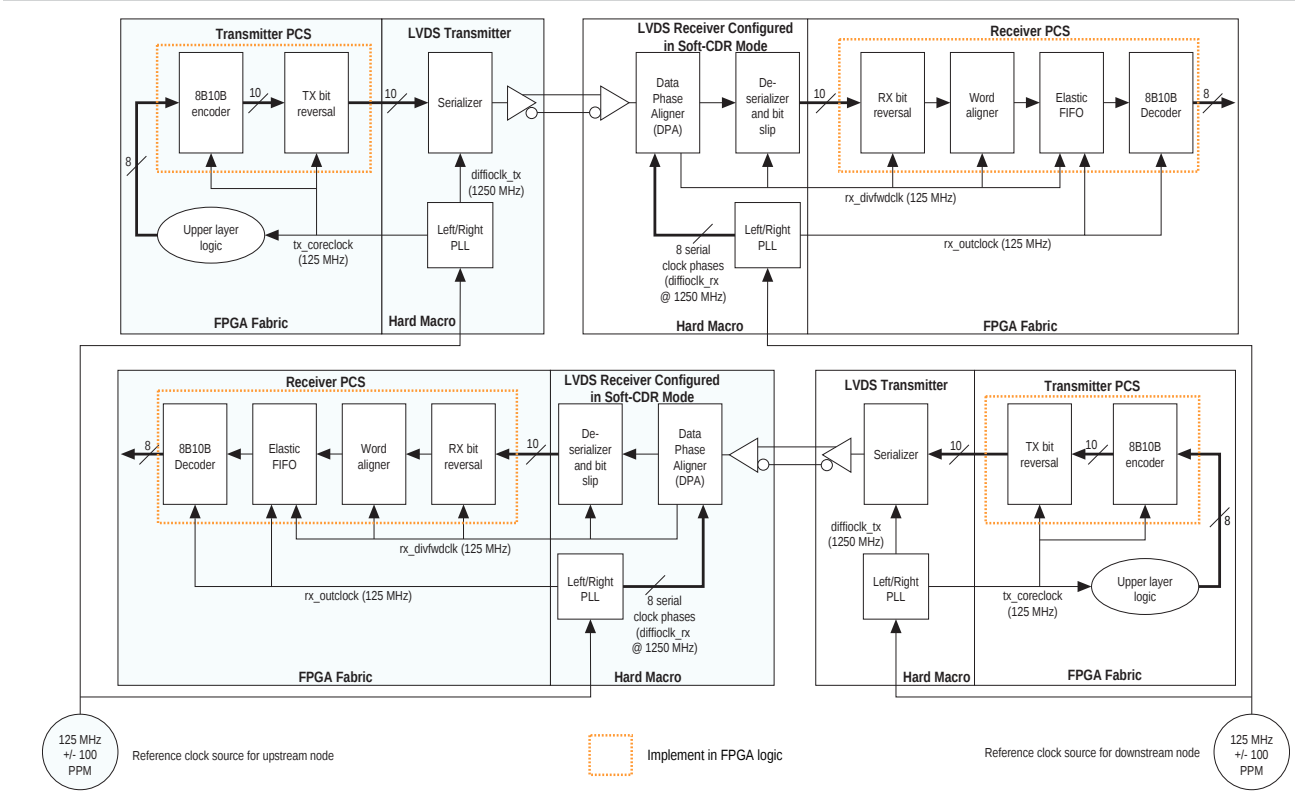


Table 4: Clocks Produced by the LVDS Transmitters

For LVDS transmitters, the PLLs typically take a 125 MHz/62.5 MHz reference clock and produces three clocks.

Clock	Description
`diffioclk_tx`	This LVDS serial clock runs at 1.25 GHz. The LVDS serial clock is internal to the hard macro and is not brought out to the output port of the ALTLVDS transmitter instantiation.
`tx_outclock`	This clock is used in source synchronous LVDS systems (DPA mode) to send the synchronous clock together with transmitted data. This clock is not used in the soft-CDR mode of the LVDS receivers.

Clock	Description
tx_coreclock	This clock runs at 125 MHz and is used for clocking these PCS functional blocks: • 8B/10B encoder • TX bit reversal block • Any other FPGA fabric logic

Table 5: Clocks Produced by the LVDS Transmitters and Receivers

For LVDS receivers, the PLL typically takes the 125 MHz/62.5 MHz reference clock and produces two clocks.

Clock	Description
diffioclk_rx	There are eight LVDS fast clocks running at 1.25 GHz with eight varying phases in the 45 degrees steps. The LVDS serial clock is internal to the hard macro and is not brought out to the output port. All eight clocks with different phases are sent to the DPA block.
rx_outclock	This is the LVDS slow clock at 125 MHz that is sent to the FPGA fabric. You can use this clock for decoupling the clock domain from the rx_divfwdclk clock in the rate matcher or elastic FIFO block.

On the LVDS receiver, the DPA block takes eight phases of serial clock from the PLL and chooses the serial clock that is best phase-aligned to the incoming serial data. The DPA block also divides this selected high speed serial clock (1.25 GHz) by the serialization factor of 10 and sends rx_divfwdclk (125 MHz) together with the parallel data to the FPGA fabric.

Implementing the Transmitter PCS Datapath

On the upstream transmitter side, upper layer logic sends 8-bit data to the 8B/10B encoder block in the PCS layer. After encoding, the 8B/10B encoder sends the 10-bit data to the transmitter reversal block. After inverting the bit order in the 10-bit word, the transmitter bit reversal block sends the data to the LVDS transmitter. In the LVDS transmitter, parallel data is serialized and sent to the transmitter buffers.

Table 6: Transmitter PCS Blocks

Implement these blocks to complete the transmitter PCS layer with an LVDS hard macro.

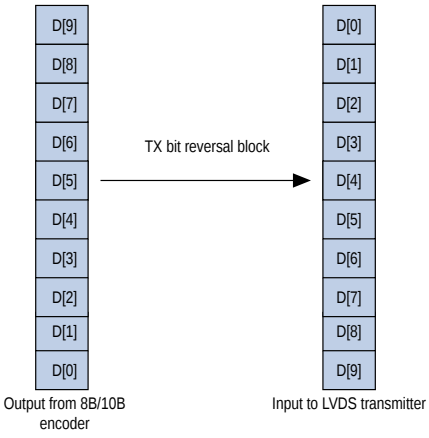
Block	Description

8B/10B encoder	• The 8B/10 encoder performs the following function:
	  • Takes in 8-bit data from the MAC layer of the GbE protocol in the FPGA fabric.
	  • Generates a 10-bit code group with proper running disparity from the 8-bit character.
	  • Feeds the 10-bit encoded data output from the 8B/10B encoder to the transmitter bit reversal block.
	• Implement the 8B/10B decoder according to the IEEE 802.3 specification.

Transmitter bit reversal	• By default, the bit order of the LVDS transmitter serializer is from most significant bit (MSB) to least significant bit (LSB). • Use the transmitter bit reversal block to reverse the bit order to LSB–to–MSB in accordance with the IEEE 802.3 standards.

Figure 8: Transmitter Bit Order Reversal

This figure shows the transmitter bit reversal block function for 10 bit wide data.



Related Information

- **High-Speed Differential I/O Interfaces and DPA in Stratix V Devices**
- **High Speed Differential I/O Interfaces with DPA in Stratix IV Devices**
- **High-Speed Differential I/O Interfaces with DPA in Stratix III Devices**
- **High-Speed Differential I/O Interfaces and DPA in Arria V Devices**
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Implementing the Receiver PCS Datapath

The PLL typically takes a 125 MHz/62.5 MHz reference clock and sends eight phases of 1.25 GHz serial clocks to the DPA block. The DPA block takes the serial data at 1.25 Gbps and selects the best phase-aligned clock using the incoming serial data. This selected DPA phase-aligned clock is used to clock the bit-slip and deserializer circuitries. The deserializer block converts the serial data stream into parallel 10-bit data and sends it to the RX bit reversal block in the FPGA fabric.

Table 7: Receiver PCS Blocks

Implement these blocks to complete the receiver PCS layer.

Block	Description
Receiver bit reversal	• By default, the LVDS receiver assumes an MSB–to–LSB bit order transmission in accordance with the IEEE 802.3 standards. • If the transmission order is LSB–to–MSB, the receiver bit reversal block reverses the data word bit order received on the FPGA fabric interface.

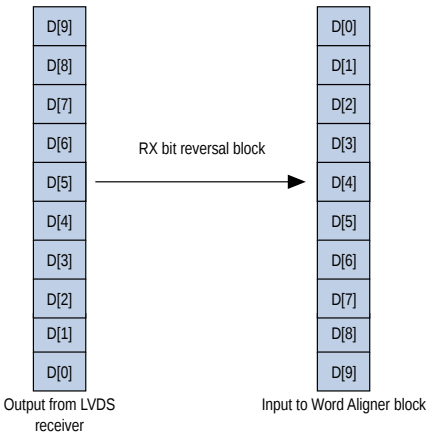
Block	Description

Word aligner	SGMII interfaces require synchronization to align the byte boundaries of the receiver and upstream transmitter. Use the word aligner block to align the byte boundary with the first /K28.5/ 10-bit comma character in the serial data stream.
	• Implement a pattern detector module in the word aligner block using data realignment (bit-slip) circuitry in the LVDS hard macro. The data realignment (bit-slip) circuit realigns the data by inserting bit latencies into the serial stream.
	• An optional `rx_channel_data_align` port controls the bit insertion of each receiver, which is independently controlled from the internal logic. The data slip one bit for every pulse on the `rx_channel_data_align` signal. Follow these requirements for the `rx_channel_data_align` signal:
	  • The minimum low time between pulses is one period of the parallel clock.
	  • The minimum pulse width is one period of the parallel clock in the logic array.
	  • This signal is an edge-triggered signal.
	  • Valid data is available two parallel clock cycles after the rising edge of the `rx_channel_data_align` signal.
	• After byte boundary alignment is fixed using the bit-slip module, your pattern detector module checks for the standard patterns and sends the data to synchronize the state machine.
	• Implement the SGMII synchronization state machine according to the IEEE 802.3 specification. Synchronization of the state machine is for hysteresis purpose.
	• For SGMII implementation, set the programmable bit rollover point at 10. The data realignment circuit can have up to 11 bit-times of insertion before a rollover occurs. An optional status port, `rx_cda_max`, is available to the FPGA fabric from each channel to indicate the time when the preset rollover point is reached.
	• Synchronization is achieved when the receiver detects three consecutive ordered sets. An ordered set defined for synchronization is a /K28.5/ comma followed by any odd number of valid /Dx.y/ code where /Dx.y/ denotes any valid data code group.

Block	Description
Elastic FIFO (rate matcher)	In GbE, the rate matcher compensates up to ±100 ppm (a total of 200 ppm) frequency difference between the upstream transmitter and receiver. • The write port of the rate matcher FIFO in each LVDS receiver channel is clocked by its forwarded clock (`rx_divfwdclk`). • The read port is clocked by the LVDS low-speed parallel clock output of the PLL. In accordance with IEEE 802.3 specification, the rate matcher logic must insert or delete /I2/ (idle ordered sets) to or from the rate matcher FIFO during the interframe or interpacket gap (IFG or IPG). If the auto-negotiation feature is implemented as part of the system, the rate matcher must insert/delete the first two bytes of the /C2/ (configuration ordered sets) in addition to the insertion/deletion of /I2/ ordered sets.
8B/10B Encoder	• In GbE, the 8B/10B decoder clocks in 10-bit data from the rate matcher and decodes it into 8-bit data. • The 8-bit decoded data is fed to upper layer logic. • Implement the 8B/10B decoder according to the IEEE 802.3 specification.

Figure 9: Receiver Bit Reversal Block

This figure shows the receiver bit reversal block functionality for 10-bit wide data.



Programmable V_{OD} and Programmable Pre-Emphasis

You can use the programmable V_{OD} and programmable pre-emphasis features in Altera FPGAs to optimize the SGMII interface. These features provide advantages in driving serial data in chip-to-chip or backplane applications.

You can assign the programmable V_{OD} and programmable pre-emphasis settings using the Quartus II Assignment Editor.

Related Information

- **High-Speed Differential I/O Interfaces and DPA in Stratix V Devices**
- **High Speed Differential I/O Interfaces with DPA in Stratix IV Devices**
- **High-Speed Differential I/O Interfaces with DPA in Stratix III Devices**
- **High-Speed Differential I/O Interfaces and DPA in Arria V Devices**
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Soft-CDR Jitter Tolerance for SGMII Interface

To meet the receiver jitter tolerance for 1000 Base LX/SX specification, implement passive equalization circuitry at the LVDS receiver input.

For GbE protocols, the total jitter specification consists of the following elements:

- Inter-symbol interference (ISI)
- Random jitter

To reduce ISI, implement passive equalization circuits.

Figure 10: Receiver Soft-CDR Passive Equalizer for GbE

This figure shows the passive equalization circuit at the LVDS receiver input pins for the GbE protocol. The circuit uses 100 Ω on-chip termination (OCT).

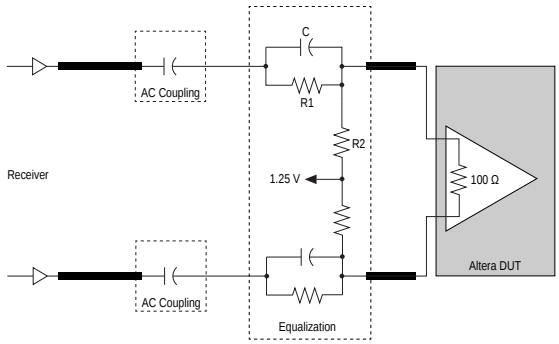


Table 8: GbE 1000BASE-CD Passive Equalizer Parameters

This table lists parameter values that Altera recommends for the GbE 1000BASE-CD passive equalizer.

Parameter	Recommended Value
R1	35 Ω
R2	15 Ω
C	30 pF

Power Consumption for SGMII Physical Layer Implementation Using Soft-CDR Mode

Altera provides the Early Power Estimator (EPE) software—a tool for power estimation in the early design phase. Perform a power assessment using the EPE software to calculate approximate power consumption values for your design.

- Power dissipation also depends on the device selected for the implementation.
- Core dynamic power consumption involves total power consumption the following modules:
- • Clock network
  - PLL
  - LVDS transmitter and receiver hard macros
  - FPGA fabric

In the following example, the PCS logic per channel in the FPGA fabric implementation is assumed to use approximately 500 ALUTs:

- Transmitter PCS—includes the 8B/10B encoder and transmitter bit-slip.
- Receiver PCS—includes the receiver bit reversal, word aligner, elastic FIFO, and 8B/10B decoder.

Table 9: Approximate Power Consumption Example for 24-Channel SGMII Physical Layer Design Implemented Using Soft-CDR Mode

The power consumption values in this table were calculated using the EPE software. Actual power consumption values will vary depending on your design.

Power Consumption Type	Consumption Value (mW)
Core static power	632
Core dynamic power	460
I/O power	940
Total power	2032

Related Information

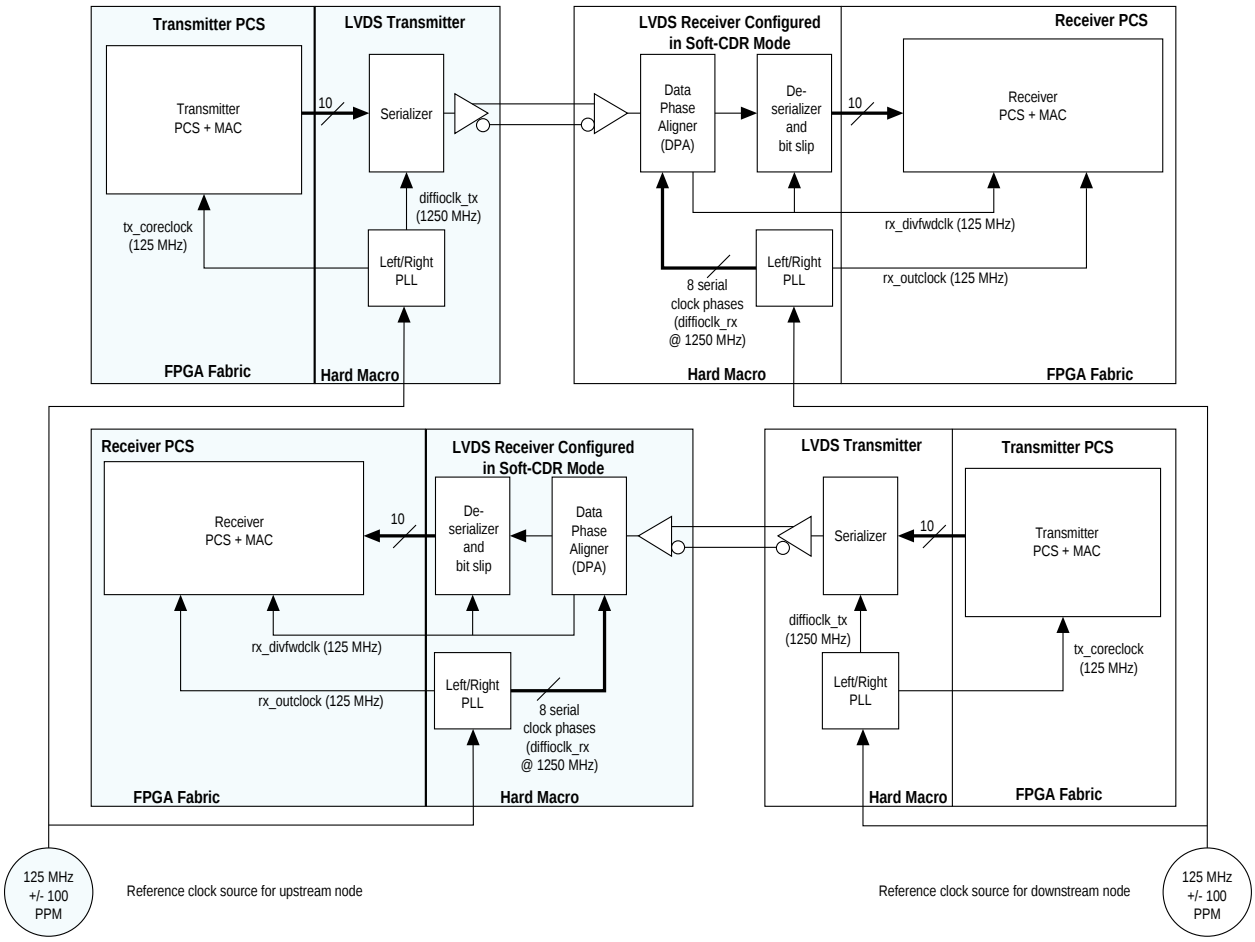
PowerPlay Early Power Estimators (EPE) and Power Analyzer

Example Implementation of SGMII Interface Using Soft-CDR

The LVDS specifications of Altera FPGA comply with the SGMII specifications. For Ethernet application, Altera implements a complete solution using the Triple-Speed Ethernet MegaCore with the PMA, PCS, and MAC.

Figure 11: Altera Triple-Speed Ethernet MegaCore Solution

This diagram shows an example SGMII system implemented on an Altera evaluation board with the Altera Triple-Speed Ethernet MegaCore. The Triple-Speed Ethernet MegaCore uses an LVDS hard macro configured as soft-CDR.



Related Information

Altera Worldwide Sales Support

For more information about the Altera Triple-Speed Ethernet MegaCore, contact the Altera sales team.

Document Revision History

Date	Version	Changes
October 2013	2013.10.17	• Rewritten and restructured document to improve clarity and speed of reference. • Added topics about implementing passive equalization circuitry to meet receiver jitter tolerance for SGMII implementation.
December 2012	2.1	Added support for Arria V devices.

Date	Version	Changes
January 2011	2.0	• Removed the "Introduction" heading and updated the section. • Added information for Stratix V, Stratix IV, and Arria II. • Added link to Cisco's SGMII specification document. • Updated the labels of the AC coupled, 1.25 Gbps links in Figure 1 and Figure 2. • Updated the "I/O Standards Interoperability" section. • Replaced previous Table 1 and Table 5 with links to relevant documents. • Added links to relevant Stratix V, Stratix IV, and Arria II documents. • Simplified the "LVDS Transmitter and Receiver (Soft-CDR)", "Configuring the ALTLVDS Transmitter and Receiver for SGMII Implementation", "Programmable VOD and Pre-Emphasis", and "Results" sections. • Removed all figures from the simplified sections except Figure 10 (previously Figure 22). • Added new Table 1 and Table 2. • Removed previous Table 2, Table 3, and Table 4. • Removed "Referenced Documents" section. • Text edits throughout the document.
March 2008	1.0	Initial release.