OpenCore Plus Evaluation of Megafunctions

November 2007, version 1.6 Application Note 320

Introduction

Altera® and Altera Megafunction Partners Program (AMPP℠) partners offer a broad portfolio of megafunctions optimized for Altera devices. The Altera MegaCore® functions and AMPP megafunctions are reusable blocks of intellectual property (IP) that you can customize and use in a design, allowing you to concentrate on adding proprietary value. Using megafunctions reduces your system implementation and verification times while maintaining high quality.

With Altera's free OpenCore Plus evaluation feature, you can perform the following actions:

- Simulate the behavior of a megafunction within your system
- Verify the functionality of your design, as well as evaluate its size and speed quickly and easily
- Generate time-limited device programming files for designs that include megafunctions
- Program a device and verify your design in hardware

OpenCore Plus hardware evaluation supports the following two modes of operation:

- *Untethered*—the design runs for a limited time
- *Tethered*—requires a connection between your board and the host computer. If tethered mode is supported by all megafunctions in a design, the device can operate for a longer time or indefinitely

All Altera MegaCore functions are included in the MegaCore IP Library. You can request AMPP megafunctions that support OpenCore Plus evaluation directly from Altera's website.

You need to purchase a license for the megafunction only when you are completely satisfied with its functionality and performance, and want to take your design to production.

This application note covers the following topics:

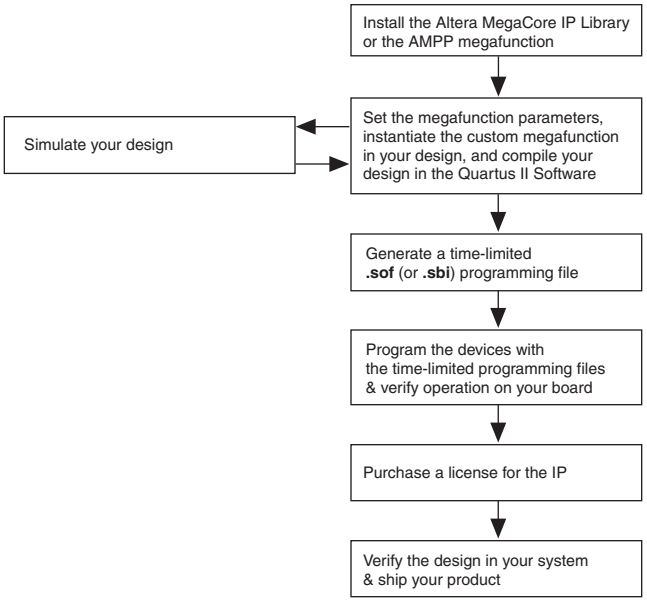
- Design flow
- Timeout indicator
- Disabling OpenCore Plus hardware evaluation

This application note covers megafunctions that are designed for the Quartus® II software version 7.2 and higher.

Design Flow

Figure 1 shows the OpenCore Plus design flow.

Figure 1. OpenCore Plus Design Flow



After you have installed the megafunctions, you are ready to begin your design. Refer to the megafunction user guide for specific instructions on how to set parameters and simulate the megafunction.

Although OpenCore Plus supported megafunctions implemented in FPGA hardware timeout, the simulation models for these megafunctions do not timeout.

If you want a positive indication that the FPGA device has timed out, you can instantiate the **ocp_timeout_indicator** IP block.

For more information on the timeout indicator, see "Timeout Indicator" on page 7.

After you have added the megafunctions to your design, on the Processing menu click **Start Compilation** to compile your design.

If all the megafunctions in your design that are not fully licensed support OpenCore Plus hardware evaluation, the Quartus II software allows you to generate a special programming file, an SRAM Object File (<*top-level project*>**_time_limited.sof**), that you can use to program a device with the Quartus II Programmer and an Altera download cable. However, you cannot use it to program memory. No **.vqm**, or atom-level **.vo**, or **.vho** files are generated. The bottom-up incremental design flow is also not supported.

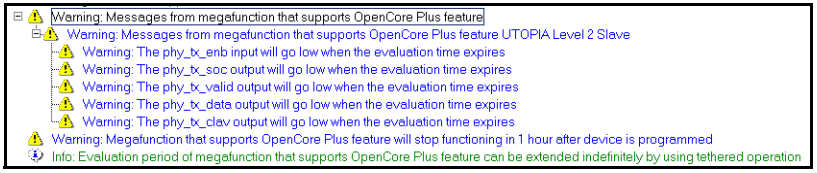
During compilation, you receive OpenCore Plus warning messages (Figure 2 on page 3). All Quartus II OpenCore Plus compilation warning messages are grouped by megafunction name. These messages inform you how each megafunction behaves when the evaluation time expires. A single summary Quartus II OpenCore Plus compilation warning reports the expiration time, which is the most restrictive (minimum) evaluation time for the entire design based upon the untethered timeout values of all the megafunctions in your design. A Quartus II OpenCore Plus compilation informational message reports the evaluation time for your design in tethered mode.

All cores must support tethered mode evaluation for this message to be displayed.

The design may run for a longer time than the evaluation time displayed in the messages. The actual time can be device and operating condition specific.

OpenCore Plus hardware evaluation is only available for devices families that have programming file support. You can still compile and simulate megafunctions for device families that do not have programming file support.

Figure 2. Time Limit Warning Message



OpenCore Plus Modes

OpenCore Plus hardware evaluation supports the following two modes of operation:

- Untethered
- Tethered

All megafunctions in a device timeout simultaneously when the most restrictive evaluation time is reached. If there is more than one megafunction in a design, a specific megafunction's timeout behavior may be masked by the timeout behavior of the other megafunctions.

Refer to the Quartus II Message Window for the device evaluation times in untethered and tethered modes and for a summary of the behavior of each megafunction when the evaluation time expires. Refer to the megafunction documentation for more details.

For Altera MegaCore functions, the untethered timeout is one hour; the tethered timeout value is indefinite.

Untethered Mode

The OpenCore Plus hardware evaluation is in untethered mode if any of the following situations exist:

- The device is not connected to the host computer running the Quartus II Programmer during hardware evaluation
- The device becomes disconnected during the evaluation
- Any of the unlicensed megafunctions in a design do not support tethered mode

Your design stops working after the hardware evaluation time expires.

Tethered Mode

Tethered mode requires an Altera serial joint test actions group (JTAG) cable connected between the JTAG port on your board and the host computer, which runs the Quartus II Programmer for the duration of the hardware evaluation period. The Quartus II Programmer only requires a minimum installation of the Quartus II software—no license is required. You can run a second Quartus II session on the host computer, to concurrently use the SignalTap® II logic analyzer.

Visit the Altera Download Center to install and run the Quartus II programmer standalone without a license.

Figure 3 shows the warning message that the host computer displays, when you add a time-limited **.sof** file to the Quartus II Programmer.

Figure 3. OpenCore Plus Warning Message

In tethered mode, the host computer controls the evaluation time by sending a periodic signal to the device via the JTAG port. If all the megafunctions in a design support tethered mode, the evaluation time runs for as long as the most restrictive megafunction. If all the megafunctions support unlimited evaluation time, the device does not time-out. If the cable is disconnected, the evaluation reverts to untethered operation, and expires when the most restrictive megafunction times out.

When the hardware evaluation time expires, you must reprogram the Altera device to continue hardware verification.

Purchase a License

After you have finished testing your design in hardware using the OpenCore Plus feature, you are ready to purchase a license for the megafunctions that you want to use.

You must license all megafunctions in the design to generate an unrestricted programming file. You can then compile your design and program the Altera devices.

Distributed Work Flow with OpenCore Plus Evaluation

The OpenCore Plus evaluation feature supports team-based (distributed) workflows. The OpenCore Plus feature allows individual designers to simulate and hardware test portions of a design containing MegaCore functions or AMPP megafunctions without requiring every member of the design team to possess a full (production) license for the IP. However, you must ultimately produce the production-ready FPGA configuration file on a machine with an available production license for all IP in the design.

The most flexible methodology for distributed workflows is for every designer to have a full license available for all IP included in their portion of the design. This methodology allows you to design and combine modules that contain IP using the Quartus II incremental compilation feature. However, OpenCore Plus allows you to avoid this licensing requirement as long as you observe the following guidelines.

- You cannot use the Quartus II incremental compilation flow to compile a portion of your design that contains unlicensed IP with the OpenCore Plus evaluation feature enabled, and then import that portion as a pre-compiled module to another machine which has an available license for the IP.
- You can use the Quartus II incremental compilation flow to avoid a full recompilation by following these steps on any machine with a Quartus II license:

1. Disable the OpenCore Plus feature on the machine without production IP licenses for all cores in the sub-design, as described in "Disabling OpenCore Plus Hardware Evaluation" on page 8.
2. Compile the sub-design.
3. On the Project menu, click **Export Design Partition**. The Quartus II software generates a Quartus II Exported Partition File (<entity name>.**qxp**) in the project directory.
4. When you are ready to generate a production, non-time-limited FPGA configuration file, use the **Import Design Partitions** command (Project menu) to import the previously exported **.qxp** files to a machine that has a full license for all of the IP cores in your design.

For more information on Quartus II incremental compilation, refer to the *Quartus II Incremental Compilation for Hierarchical and Team-Based Design* chapter in volume 1 of the *Quartus II Handbook*.

OpenCore Plus does not support the bottom-up incremental design flow.

5. Complete the remaining compilation steps to generate a production FPGA configuration file.

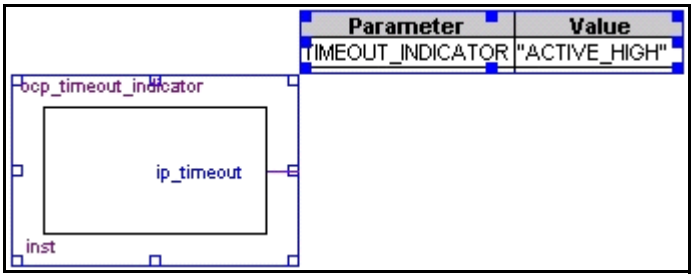
The guidelines described above apply only to hardware evaluation. For Altera MegaCore functions, it is always possible to simulate a design using IP Functional Simulation (IPFS) models generated by multiple

Quartus II sessions even if you do not have a full IP license. For AMPP megafunctions, you may need to obtain a license directly from the partner.

Timeout Indicator

If you want a positive indication that the device has timed out, you can instantiate the **ocp_timeout_indicator** IP block that is supplied with the Quartus II software (in the **quartus\libraries\others\opencore_plus** directory). The active polarity of the time-out signal, `ip_timeout`, can be specified via the `TIMEOUT_INDICATOR` parameter. The options are `ACTIVE_HIGH` (the default), or `ACTIVE_LOW`. Figure 4 shows the **ocp_timeout_indicator** symbol, VHDL, Verilog HDL prototypes and sample instantiation.

Figure 4. OCP_TIMEOUT_INDICATOR Symbol, VHDL, Verilog Prototypes & Sample Instantiation



The VHDL component declaration:

```
component ocp_timeout_indicator is
generic
    (
        TIMEOUT_INDICATOR: string := "ACTIVE_HIGH"
    );
    port
    (
        ip_timeout: out std_logic
    );
end component ocp_timeout_indicator;
```

The VHDL instantiation prototype is:

```
My_Instance : ocp_timeout_indicator
GENERIC MAP(TIMEOUT_INDICATOR => "ACTIVE_HIGH")
PORT MAP(ip_timeout => My_Output);
```

The Verilog HDL instantiation prototype is:

```
ocp_timeout_indicator my_instance
(.ip_timeout(my_output));
defparam my_instance.TIMEOUT_INDICATOR =
"ACTIVE_HIGH";
```

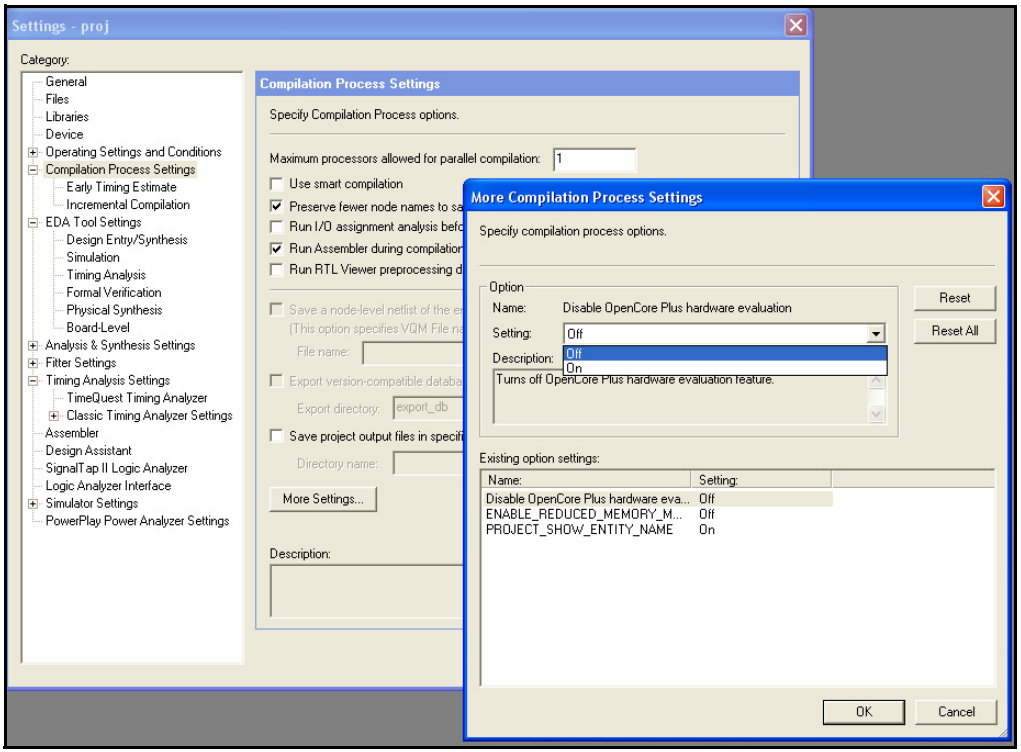
Disabling OpenCore Plus Hardware Evaluation

The OpenCore Plus hardware evaluation feature adds logic to your design. This additional logic may affect the timing and fitting of your design.

If you do not wish to perform an OpenCore Plus hardware evaluation, follow these steps:

1. In the Quartus II software, on the Assignments menu click **Settings**.
2. In the Category list, select **Compilation Process Settings**.
3. Click **More Settings**.
4. Click **Disable OpenCore Plus hardware evaluation** and select **On** (see Figure 5).

Figure 5. Disable OpenCore Plus Hardware Evaluation



The Quartus II Compiler and Design Assistant may produce warning messages that originate from the OpenCore Plus hardware evaluation circuitry. You can safely ignore these messages. These messages typically include source node(s) from the clock `altera_internal_jtag~TCKUTAP` or have name strings similar to the following example:

```
pzdyqx:nabboc|pzdyqx_impl
sld_hub:sld_hub_inst
```

OpenCore Plus Simulation-Only Evaluation

If you specify an advanced device that does not have programming file support the OpenCore Plus hardware evaluation feature reverts to OpenCore simulation-only evaluation. You can still parameterize your megafunction, instantiate it in your design, compile and simulate it, but you will not be able to generate a programming file. The Quartus II software will generate a message that says:

```
Warning: Using OpenCore simulation evaluation for all
cores in the design.

Warning: The current device family does not support the
OpenCore Plus hardware evaluation feature.
```

Document Revision History

Table 1 shows the revision history for this document.

Table 1. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
November 2007, v1.6	• Added section on Distributed workflow using OpenCore Plus.	—
September 2007, v1.5	• Removed reference to LogicLock flow. VQM is no longer recommended and it is not supported for Stratix® III/Cyclone® III.	—
May 2007, v1.4	• Updated "Disabling OpenCore Plus Hardware Evaluation" section.	—
October 2003, v1.0	Initial release	—

101 Innovation Drive
San Jose, CA 95134
(www.altera.com