WHITE PAPER

FPGA

Delivering Intelligent Bandwidth with Intel® Stratix® 10 Transceiver Tiles

Stratix 10 FPGAs and SoCs include innovative technologies that address next-generation systems' bandwidth and intelligence requirements.

Author

Minh Mac
Manager, Transceiver and Platform Product Marketing
Intel FPGA

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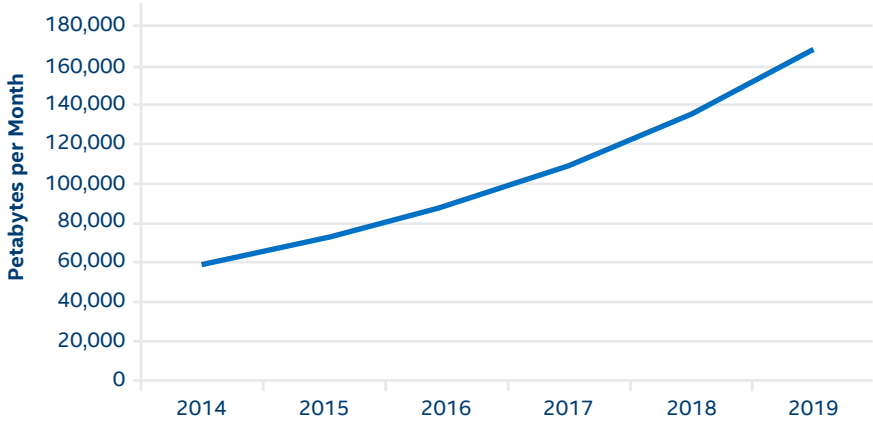
Introduction

It's clear: the need to transfer increasing volumes of data traffic as fast as possible from one point to another will remain unabated for the foreseeable future. Back in 2014, total global IT traffic was predicted to nearly triple within five years, and this traffic increase is well underway. Applications such as wired data centers and wireless next-generation cellular networks are driving this tremendous bandwidth increase. See Figure 1.

It is not economical or feasible to simply add incremental network infrastructure to keep pace with this explosive demand. The need for faster, smarter data centers and networks has become a fundamental requirement in today's and next-generation systems. To solve this problem, a system should be able to handle the increasing bandwidth and have intelligence to balance the workload of the data entering and leaving the system. Intel® Stratix® 10 FPGAs and SoCs (formerly Altera® Stratix® 10 FPGAs and SoCs) make this solution possible.

Intel Stratix 10 FPGAs and SoCs include innovative technologies that address next-generation systems' bandwidth and intelligence requirements. A data center server's workload fluctuates depending on the time of day. For example, the workload may be low in the morning, peak at mid-day, and be very low at night. Furthermore, a single server's workload type can vary from running a specific application to providing compute resources. Servicing each workload request using a standard "one size fits all" approach—without the intelligence to switch and balance workloads—is costly and ineffective. To create smarter systems such as workload balancing and virtualization, Intel Stratix 10 FPGAs utilize a high-



Source: Global IP Traffic Growth 2014-2019 Forecast, Cisco VNI

Figure 1. Global IP Traffic

performance, programmable monolithic core fabric. The programmable core allows a server to switch seamlessly between optimized applications catered to the workload type the server needs.

To satisfy bandwidth needs, Intel Stratix 10 FPGAs have fully integrated transceivers. Transceivers are the backbone that transmit and receive large amounts of data traffic in the shortest time possible either from component-to-component, across long copper PCB traces, or through copper cables. Transceivers accomplish this task by serializing parallel data before transmission and deserializing the serial data on reception. Using serialized data, transceivers can transmit and receive data in the giga-bits per second range for single or multiple channels. By combining channels, applications can achieve 40, 50, 100, 400, 800, and 1,200 Gigabit interfaces.

Despite the need for faster and larger amounts of data, not every step along a data packet's journey requires top line rates. For example, massive multiple-input and multiple-output (MIMO) to enable 5G wireless requires different bandwidth than a backhaul/access network. Additionally, the chip-to-chip communications within a system has its own bandwidth requirements.

Intel Stratix 10 FPGAs bridge bandwidth needs for today and tomorrow

Intel Stratix 10 FPGAs employ heterogeneous 3D SiP technology that integrates multiple die in a single package. Intel's Embedded Multi-die Interconnect Bridge (EMIB) is a silicon bridge that connects the multiple die together in the package. All Intel Stratix 10 family variants use a single monolithic core fabric die that is connected to transceiver tiles (up to 6 die), with EMIB bridging the die together as shown in Figure 2.

The Intel Stratix 10 monolithic core is capable of up to 1 GHz $\mathbf{f}_{MAX}$ performance and provides a programmable platform for intelligent systems. The core contains up to 5.5 million logic elements along with variable-precision DSP blocks that feature hard floating-point and fixed-point capability, as well as multiple sizes of embedded SRAM memory blocks. These features are more than sufficient to address system needs today and tomorrow.

Transceiver tiles reside on either side of the monolithic core. A transceiver tile is a group of full-duplex transceiver channels with hard IP blocks on a single silicon die. The tile also contains auxiliary functions, such as high-speed clocking, encoding, and decoding. Because system needs vary, the Intel Stratix 10 family offers three different transceiver tiles: L-tiles, H-tiles, and E-tiles. Each transceiver tile offers unique benefits for system design.

Mainstream and high-bandwidth applications

The transceiver L-tile is ideal for mainstream protocols running data rates up to 17.4 Gbps. A single L-tile contains 24 full duplex channels with advanced PCS and PMA capabilities. This versatile tile provides chip-to-chip, chip-to-module, and backplane capabilities. It also supports a hard PCIe* Gen3 x16 IP block, which provides the control plane needed for communication networks.

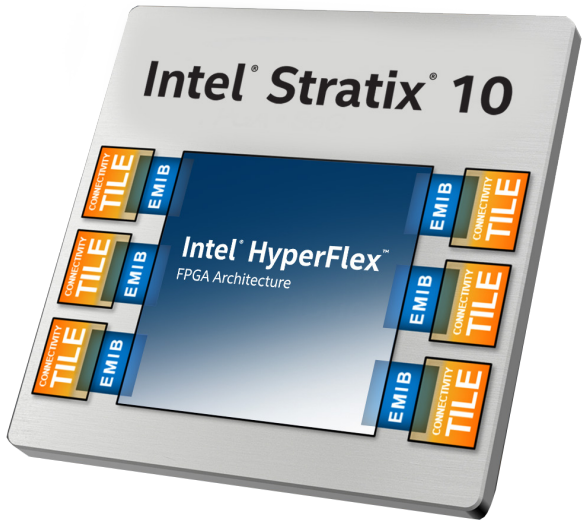


Figure 2. Intel Stratix 10 Heterogeneous 3D SiP Technology

The transceiver H-tile addresses systems requiring bandwidths beyond those offered by the L-tile. The H-tile contains transceiver channels capable of data rates up to 28.3 Gbps. Similar to the L-tile, each H-tile supports 24 full duplex channels with advanced PCS and PMA capabilities. The H-tile transceivers can be used in chip-to-chip, chip-to-module, and backplane applications. Each H-tile transceiver channel contains advanced equalization circuits. With these circuits, the tile can drive backplanes at the maximum data rate of 28.3 Gbps with up to 30 dB of insertion loss.

High-performance and next-generation applications

Transceiver E-tiles target high-performance protocols as well as new, emerging protocols. Each E-tile supports 24 full duplex channels with advanced PCS and PMA capabilities. Unlike the L- and H-tiles, E-tile transceiver channels are dual-mode. Dual-mode allows a single transceiver channel to switch the modulation format it uses when transmitting and receiving data. The E-tile supports two modulation formats:

- The traditional Non Return to Zero (NRZ) format
- The newer four-level Pulse Amplitude Modulation (PAM-4) format

In NRZ mode, the transceiver channel supports data rates up to 30 Gbps, which is ideal for chip-to-chip, chip-to-module, and backplane applications. In this mode, the transceiver supports short and long reach electrical specifications such as IEEE 802.3bj and OIF CEI 28G VSR.

In PAM-4 mode, the transceiver channel supports data rates up to 56 Gbps, and targets the short and long reach electrical specifications for new and emerging standards such as OIF CEI 56 LR, MR, and VSR. Because of their advanced equalization circuits, the transceivers support legacy backplanes and high-loss backplanes, and can achieve the bit error rates (BER) required by most high-speed protocols. To complement the high-bandwidth transceiver channels,

Features	Transceiver Tile Variations		
	PCIe Gen3x16 L-Tile 17.4G	PCIe Gen3x16 H-Tile 28.3G	4x100GE E-Tile 30G/56G
Intel Stratix 10 Device Variants	GX, SX	GX, SX, TX, MX	TX, MX
Transceivers per Tile	24	24	24
Maximum Chip-to-Chip Data Rates			
NRZ	17.4 Gbps	28.3 Gbps	30 Gbps
PAM-4	—	—	56 Gbps
Maximum Backplane Data Rates			
NRZ	12.5 Gbps	28.3 Gbps	30 Gbps
PAM-4	—	—	56 Gbps
Insertion Loss at Maximum Data Rate	Up to 18 dB	Up to 30 dB	Up to 30 dB
Hard IP	• PCIe* Gen1, 2, and 3 with x1, x4, x8, and x16 lane support • 10G Fire Code FEC Hard IP	• PCIe Gen1, 2, and 3 with x1, x4, x8, and x16 lane support • SR-IOV with4 Physical functions and 2K Virtual Functions • 10G Fire Code FEC Hard IP	• 10/25/100 GbE MAC with RS-FEC
Channel Support	GX	GX and GXT	GXE

Table 1. Intel Stratix 10 Transceiver Tile Variations

the E-tile supports hard 100 Gb Ethernet MACs. Each E-tile supports up to four 100 Gb Ethernet MAC blocks or alternatively, six 10/25 Gb Ethernet MACs.

Conclusion

With heterogeneous 3D SiP technology that pairs a high-performance monolithic core with transceiver tiles, the Intel Stratix 10 family is uniquely positioned to address the bandwidth demands of next-generation systems. Because transceiver tiles are decoupled from the monolithic core, each tile uses optimized technology to provide the best power and performance for the functions it performs. This architecture allows flexibility and fast time to market for current and future protocol needs.

References

[1] https://www.altera.com/content/dam/altera-www/global/en_US/pdfs/literature/wp/wp-01251-enabling-nextgen-with-3d-system-in-package.pdf

Where to Get More Information

For more information about Intel and Intel Stratix 10 FPGAs, visit **https://www.altera.com/products/fpga/stratix-series/stratix-10/overview.html**