

Performance Benchmarks Overview

This data sheet lists the performance and logic element (LE) usage for the Nios® II soft processor and peripherals. The Nios II soft processor is configurable and designed for implementation in Altera® FPGAs. The following Nios II processors were used for these benchmarks:

- Nios II/f—The Nios II/f “fast” processor is designed for high performance while presenting the most configuration options which are unavailable in the other Nios II processors.
- Nios II/s—The Nios II/s “standard” processor is designed for small size while maintaining moderate performance.
- Nios II/e—The Nios II/e “economy” processor is designed for the smallest possible processor size while providing adequate performance.

The default options for the Nios II processor were chosen for these benchmarks, unless specified otherwise.



Results may vary slightly depending on the version of the Quartus® II software, the version of the Nios II processor, and the target device. Also, any changes to the system logic design might change the performance and LE usage.

Table 1 and Table 2 list the f_{MAX} and millions of instructions per second (MIPS) for a system with the following components:

- Nios II processor with JTAG debug module
- JTAG UART
- 64 kilobytes (KB) on-chip memory (Cyclone® designs use one megabyte [MB] of off-chip SDR SDRAM)
- Avalon® Memory-Mapped (Avalon-MM) pipeline bridge
- Timer



The MIPS reports were obtained using the MIPS* (*Dhrystones 2.1 benchmark). You can download the Dhrystones 2.1 benchmark software from the [Nios II Embedded Processor Design Examples](#) page on the Altera website. For more information about the Dhrystones 2.1 benchmark software, refer to the **readme.txt** file which is included in the Dhrystones 2.1 benchmark design example.



The Fast design example illustrates a system that has all the components listed. You can download the Fast design example from the [Nios II Embedded Processor Design Examples](#) page on the Altera website. For more information about the Fast design example, refer to the **readme.txt** file which is included in the Fast design example.

Table 1. f_{MAX} for Nios II Processor System (MHz) (Note 1)

Device Family	Device Used	Nios II/f	Nios II/s	Nios II/e
Stratix [®] V (2)	5SGXMA3H2F35C2	250	240	320
Stratix IV	EP4SGX230HF35C2	230	240	300
Stratix III	EP3SL150F1152C2	290	230	340
Stratix II	EP2S60F1020C3	220	170	285
Stratix	EP1S80F1020C5	150	130	170
HardCopy [®] IV (2)	HC4E35FF1152	305	285	290
HardCopy III (2)	HC322FF1152	230	220	210
HardCopy II	HC230F1020C	200	200	320
HardCopy Stratix	EP1S80F1020C5_HC	150	130	175
Cyclone IV GX	EP4CGX30CF19C6	150	120	175
Cyclone III LS (3)	EP3CLS70F484C7	135	100	140
Cyclone III (3)	EP3C40F324C6	175	145	215
Cyclone II	EP2C20F484C6	140	110	195
Cyclone	EP1C20F400C6	135	120	175
Arria [®] II GX	EP2AGX95DF25C4	230	200	270
Arria GX	EP1AGX60CF484C6	140	100	150

Notes to Table 1:

- (1) These results were generated using push button Analysis, Synthesis and Fitter settings in the Quartus II software. The results for Stratix V, Stratix IV, Cyclone IV GX, Cyclone III LS, and Arria II GX are generated using Qsys-based designs while other results are generated using SOPC Builder-based designs.
- (2) Stratix V, HardCopy IV, and HardCopy III results are based on preliminary timing models.
- (3) When comparing Cyclone III LS and Cyclone III results in Table 1, note that a speed grade 6 device was used for the Cyclone III device, whereas a speed grade 7 device was used for the Cyclone III LS device.

Table 2 lists the value of MIPS for the different types of Nios II processors, while Table 3 lists the ratio of MIPS over the system clock (MIPS/MHz).

Table 2. MIPS for Nios II Processor System (Note 1) (Part 1 of 2)

Device Family	Device Used	Nios II/f	Nios II/s	Nios II/e
Stratix V (1)	5SGXMA3H2F35C2	283	154	49
Stratix IV (1)	EP4SGX230HF35C2	260	154	46
Stratix III	EP3SL150F1152C2	340	140	48
Stratix II	EP2S60F1020C3	250	110	45
Stratix	EP1S80F1020C5	170	80	27
HardCopy IV	HC4E35FF1152	345	180	45
HardCopy III (1)	HC322FF1152	260	140	30
HardCopy II	HC230F1020C	230	130	50
HardCopy Stratix	EP1S80F1020C5_HC	165	85	27

Table 2. MIPS for Nios II Processor System (Note 1) (Part 2 of 2)

Device Family	Device Used	Nios II/f	Nios II/s	Nios II/e
Cyclone IV GX	EP4CGX30CF19C6	170	77	27
Cyclone III LS	EP3CLS70F484C7	153	64	22
Cyclone III	EP3C40F324C6	195	90	30
Cyclone II	EP2C20F484C6	145	55	18
Cyclone	EP1C20F400C6	130	52	17
Arria II GX	EP2AGX95DF25C4	260	128	42
Arria GX	EP1AGX60CF484C6	150	65	25

Notes to Table 2:

- (1) These results were generated using push button Analysis, Synthesis, and Fitter settings in the Quartus II software. The results for Stratix V, Stratix IV, Cyclone IV GX, Cyclone III LS, and Arria II GX are generated using Qsys-based designs while other results are generated using SOPC Builder-based designs.
- (2) Stratix V, HardCopy IV, and HardCopy III MIPS results are based on estimations.

Table 3 lists the ratio of MIPS over system clock (MIPS/MHz).

Table 3. MIPS/MHz Ratio for Nios II Processor System on Various Device Families

Device Family	Nios II/f	Nios II/s	Nios II/e
Stratix V	1.13	0.64	0.15
Stratix IV	1.13	0.64	0.15
Stratix III	1.183	0.611	0.138
Stratix II	1.183	0.611	0.138
Cyclone IV GX	1.13	0.64	0.15
Cyclone III LS	1.13	0.64	0.15
Cyclone III	1.109	0.604	0.138
Cyclone II	1.105	0.518	0.107
HardCopy IV	1.13	0.64	0.15
Arria II GX	1.13	0.64	0.15

Table 4 lists the LE usage for the Nios II processor cores and most of the common peripherals for Stratix IV, Stratix III, Stratix II and Stratix devices.

Table 4. LE Usage for Nios II Processor Cores and Peripherals—Stratix IV, Stratix III, Stratix II, and Stratix Devices (Note 1)

Processor Core / Peripheral	Stratix V (ALUTs) (1)	Stratix IV (ALUTs) (1)	Stratix III (ALUTs)	Stratix II (ALUTs)	Stratix (LEs)
Nios II/f (3)	1,110	1,110	1,020	1,320	1,800
Nios II/s (4)	890	890	800	1,030	1,170
Nios II/e (5)	660	660	520	500	530
Nios II JTAG debug module	110	110	110	430	390
UART	90	90	40	130	150
JTAG UART	110	110	115	205	210
SDR SDRAM Controller	180	180	310	520	760

Table 4. LE Usage for Nios II Processor Cores and Peripherals—Stratix IV, Stratix III, Stratix II, and Stratix Devices (Note 1)

Processor Core / Peripheral	Stratix V (ALUTs) (1)	Stratix IV (ALUTs) (1)	Stratix III (ALUTs)	Stratix II (ALUTs)	Stratix (LEs)
Timer	100	100	120	185	160

Notes to Table 4:

- (1) The resource utilization results were generated using moderate Analysis and Synthesis settings or Fitter settings in the Quartus II software. The results for Stratix V, Stratix IV, Cyclone IV GX, Cyclone III LS, and Arria II GX are generated using Qsys-based designs while other results are generated using SOPC Builder-based designs. These results represent typical results. Your results may vary.
- (2) An adaptive look-up table (ALUT) is the cell used in the Quartus II software for logic synthesis for the Stratix II device and later device families. It is equivalent to about 1.25 LEs.
- (3) The Nios II/f processor used has 512-bytes instruction and data caches, and no hardware multiplier.
- (4) The Nios II/s processor used has 512-bytes instruction, no data caches and hardware multiplier.
- (5) The Nios II/e processor used has no instruction, data caches, and hardware multiplier.

Table 5 lists the LE usage for the Nios II processor cores and most of the common peripherals for Cyclone IV GX, Cyclone III LS, Cyclone III, Cyclone II and Cyclone devices.

Table 5. LE Usage for Nios II Processor Cores and Peripherals—Cyclone IV GX, Cyclone III LS, Cyclone III, Cyclone II, and Cyclone Devices (Note 1)

Processor Core / Peripheral	Cyclone IV GX	Cyclone III LS	Cyclone III (LEs)	Cyclone II (LEs)	Cyclone (LEs)
Nios II/f (3)	2,100	2,080	1,800	1,600	1,680
Nios II/s (4)	1,620	1,630	1,300	1,030	1,140
Nios II/e (5)	980	980	650	540	520
Nios II JTAG debug module	290	290	250	450	450
UART	130	130	75	140	155
JTAG UART	160	160	170	165	200
SDR SDRAM Controller	360	360	420	750	760
Timer	150	150	150	150	155

Notes to Table 5:

- (1) The resource utilization results were generated using moderate Analysis and Synthesis settings or Fitter settings in the Quartus II software. The results for Stratix V, Stratix IV, Cyclone IV GX, Cyclone III LS, and Arria II GX are generated using Qsys-based designs while other results are generated using SOPC Builder-based designs. These results represent typical results. Your results may vary.
- (2) HCells are logic blocks that implement both logic and DSP functions. DSP block functions are implemented using HCells instead of dedicated DSP blocks.
- (3) The Nios II/f processor used has 512-bytes instruction and data caches, and no hardware multiplier.
- (4) The Nios II/s processor used has 512-bytes instruction, no data caches and hardware multiplier.
- (5) The Nios II/e processor used has no instruction, data caches, and hardware multiplier.

Table 6 lists the LE usage for the Nios II processor cores and most of the common peripherals for HardCopy IV, HardCopy III, HardCopy II, HardCopy Stratix, Arria II GX, and Arria GX devices.

Table 6. LE Usage for Nios II Processor Cores and Peripherals—HardCopy IV, HardCopy III, HardCopy II, HardCopy Stratix, Arria II GX, and Arria GX Devices (Note 1) (Part 1 of 2)

Processor Core / Peripheral	HardCopy IV	HardCopy III (HCells) (2)	HardCopy II (HCells) (2)	HardCopy Stratix (LEs)	Arria II GX (ALUTs) (3)	Arria GX (ALUTs)
Nios II/f (4)	11,000	9,100	8,900	1,770	1,120	1,000
Nios II/s (5)	8,150	6,900	6,500	1,200	890	800

Table 6. LE Usage for Nios II Processor Cores and Peripherals—HardCopy IV, HardCopy III, HardCopy II, HardCopy Stratix, Arria II GX, and Arria GX Devices (Note 1) (Part 2 of 2)

Processor Core / Peripheral	HardCopy IV	HardCopy III (HCells) (2)	HardCopy II (HCells) (2)	HardCopy Stratix (LEs)	Arria II GX (ALUTs) (3)	Arria GX (ALUTs)
Nios II/e (6)	4,390	4,000	2,250	520	690	550
Nios II JTAG debug module	1,800	1,200	350	390	110	110
UART	1,000	700	520	150	90	100
JTAG UART	1,300	850	620	210	110	110
SDR SDRAM Controller	2,700	1,900	1,740	760	180	300
Timer	1,260	9,100	700	160	110	110

Notes to Table 6:

- (1) The resource utilization results were generated using moderate Analysis and Synthesis settings or Fitter settings in the Quartus II software. The results for Stratix V, Stratix IV, Cyclone IV GX, Cyclone III LS, and Arria II GX are generated using Qsys-based designs while other results are generated using SOPC Builder-based designs. These results represent typical results. Your results may vary.
- (2) HCells are logic blocks that implement both logic and DSP functions. DSP block functions are implemented using HCells instead of dedicated DSP blocks.
- (3) An ALUT is the cell used in the Quartus II software for logic synthesis for Stratix II and later device families. It is equivalent to about 1.25 LEs.
- (4) The Nios II/f processor used has 512-bytes instruction and data caches, and no hardware multiplier.
- (5) The Nios II/s processor used has 512-bytes instruction, no data caches and hardware multiplier.
- (6) The Nios II/e processor used has no instruction, data caches, and hardware multiplier.



Additional performance benchmarking information for the Nios II processor can be found at the following links:

- For more information about the Nios II interrupt latency performance, refer to the *Exception Handling* chapter of the *Nios II Software Developer's Handbook*.
- For more information about the Nios II floating-point custom instruction performance, refer to the *Using Nios II Floating-Point Custom Instructions Tutorial*.
- For more information about the Nios II networking applications performance, refer to *AN440: Accelerating Nios II Networking Applications*.

Document Revision History

Table 7 shows the revision history for this document.

Table 7. Document Revision History (Part 1 of 2)

Date	Version	Changes
June 2011	7.0	<ul style="list-style-type: none"> ■ Measured performance and LE usage with the Quartus II version 11.0 software and the Nios II version 11.0 processor. ■ Updated all tables with new data.
July 2010	6.0	<ul style="list-style-type: none"> ■ Measured performance and LE usage with the Quartus II version 11.0 software and the Nios II version 10.0 processor. ■ Rearranged the logic element usage for Nios II processor cores and peripherals for HardCopy IV, HardCopy III, HardCopy II, HardCopy Stratix from table 5 to table 6. ■ Added new information for Stratix V device. ■ Updated all tables with new data.

Table 7. Document Revision History (Part 2 of 2)

Date	Version	Changes
February 2010	5.0	<ul style="list-style-type: none"> ■ Measured performance and LE usage with the Quartus II version 9.1 software and the Nios II version 9.1 processor. ■ Added new information for the Cyclone III LS, Cyclone IV GX, and HardCopy IV devices. ■ Updated information for Arria II GX devices. ■ Updated Table 1, Table 2, Table 3, Table 5, and Table 6 with new data.
June 2009	4.0	<ul style="list-style-type: none"> ■ Measured performance and LE usage with the Quartus II version 9.0 SP1 software and the Nios II version 9.0 SP1 processor. ■ Added information for the HardCopy III, Arria II GX, and Arria GX devices. ■ Updated Tables 1 and 2 with new data. ■ Added Table 6.
July 2008	3.0	<ul style="list-style-type: none"> ■ Measured performance and LE usage with the Quartus II version 8.0 software and the Nios II version 8.0 processor. ■ Added information for the Stratix IV device. ■ Added links for additional information on Nios II benchmark performance. ■ Updated Tables 1, 2, 4 and 5 with new data. ■ Added Table 3.
August 2007	2.0	<ul style="list-style-type: none"> ■ Measured performance and LE usage with the Quartus II version 6.1 software and the Nios II version 6.1 processor. ■ Added information for the Stratix III, HardCopy II, and Cyclone III devices. ■ Updated Tables 1, 2, and 3 with new data.
October 2004	1.0	Initial release.