



# Intel FPGA IP

## Release Notes

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Updated for Intel® Quartus® Prime Design Suite: **17.1**

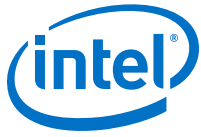


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## 1 Intel® FPGA IP Release Notes

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These release notes include links to Intel FPGA IP cores, including the Intel FPGA IP Library and other IP cores.

- [1G/10GbE and Backplane Ethernet 10GBASE-KR PHY Release Notes](#)
- [10-Gbps Ethernet \(10GbE\) MAC IP Core Release Notes](#)
- [1G/2.5G/10G Multi-rate Ethernet PHY Release Notes](#)
- [10GBASE-R PHY IP Core Release Notes](#)
- [25G Ethernet IP Core Release Notes](#)
- [40- and 100-Gbps Ethernet MAC and PHY IP Core Release Notes](#)
- [50G Ethernet IP Core Release Notes](#)
- [50G Interlaken IP Core Release Notes](#)
- [100G Interlaken IP Core Release Notes](#)
- [Arria V GZ Hard IP for PCI Express IP Core Release Notes](#)
- [Arria V Hard IP for PCI Express IP Core Release Notes](#)
- [Arria 10 1G/10GbE and 10GBASE-KR PHY IP Core Release Notes](#)
- [Arria 10 External Memory Interface IP Core Release Notes](#)
- [Arria 10 FPLL IP Core Release Notes](#)
- [Arria 10 Hard IP for PCI Express IP Core Release Notes](#)
- [Arria 10 Transceiver ATX PLL IP Core Release Notes](#)
- [Arria 10 Transceiver CMU PLL IP Core Release Notes](#)
- [Arria 10 Transceiver Native PHY IP Core Release Notes](#)
- [BCH IP Core Release Notes](#)
- [CIC IP Core Release Notes](#)
- [CPRI IP Core Release Notes](#)
- [Cyclone V Hard IP for PCI Express IP Core Release Notes](#)
- [DDR2 and DDR3 SDRAM Controller with UniPHY IP Core Release Notes](#)
- [Intel FPGA DisplayPort IP Core Release Notes](#)
- [FIR II IP Core Release Notes](#)
- [FFT IP Core Release Notes](#)
- [Intel FPGA HDMI IP Core Release Notes](#)
- [High-speed Reed-Solomon IP Core Release Notes](#)
- [Hybrid Memory Cube Controller IP Core Release Notes](#)
- [Intel® Stratix® 10 H-Tile Hard IP for Ethernet IP Core Release Notes](#)

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- [Intel Stratix 10 Hard IP for PCI Express\\* IP Core Release Notes](#)
- [Intel Stratix 10 Low Latency 40-Gbps Ethernet IP Core Release Notes](#)
- [Intel Stratix 10 Low Latency 100-Gbps Ethernet IP Core Release Notes](#)
- [Intel Stratix 10 1G/2.5G/5G/10G Multi-rate Ethernet PHY IP Core Release Notes](#)
- [Intel Stratix 10 10GBASE-KR PHY IP Core Release Notes](#)
- [Interlaken IP Core \(2nd Generation\) Release Notes](#)
- [Interlaken PHY IP Core Release Notes](#)
- [IP Compiler for PCI Express Release Notes](#)
- [JESD204B IP Core Release Notes](#)
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- [Other Transceiver IP Cores Product Release Notes](#)

#### **Related Links**

- [Introduction to Intel FPGA IP Cores](#)



- [Intel FPGA Software Installation and Licensing](#)

## **1.1 Errata**

Errata are functional defects or errors, which may cause the product to deviate from published specifications. Documentation issues include errors, unclear descriptions, or omissions from current published specifications or product documents.

For full information on errata and the versions affected by errata, refer to the Knowledge Base page of the Altera website.

### **Related Links**

[Altera Knowledge Base](#)