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Revision History

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<tr>
<th>Rev.</th>
<th>Draft/Changes</th>
<th>Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>-001</td>
<td>• Initial Release.</td>
<td>February 2004</td>
</tr>
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</table>
Preface

This public document is an update to the specifications contained in the documents listed in the following Affected Documents/Related Documents table. It is a compilation of device and document errata and specification clarifications and changes, and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this update document and are no longer published in other documents.

Affected Documents/Related Documents

<table>
<thead>
<tr>
<th>Document Title</th>
<th>Document Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel® E7210 Chipset Datasheet:</td>
<td>300798-001EN</td>
</tr>
</tbody>
</table>

Nomenclature

Errata are design defects or errors. Errata may cause the behavior of the Intel E7210 MCH to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Specification Clarifications describe a specification in greater detail or further highlight a specification’s impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.
Component Identification via Programming Interface

The E7210 MCH may be identified by the following register contents:

<table>
<thead>
<tr>
<th>Stepping</th>
<th>Vendor ID¹</th>
<th>Device ID²</th>
<th>Revision Number³</th>
</tr>
</thead>
<tbody>
<tr>
<td>A2</td>
<td>8086h</td>
<td>2578h</td>
<td>02h</td>
</tr>
</tbody>
</table>

NOTES:
1. The Vendor ID corresponds to bits 15:0 of the Vendor ID Register located at offset 00–01h in the PCI function 0 configuration space.
2. The Device ID corresponds to bits 15:0 of the Device ID Register located at offset 02–03h in the PCI function 0 configuration space.
3. The Revision Number corresponds to bits 7:0 of the Revision ID Register located at offset 08h in the PCI function 0 configuration space.

Component Marking Information

The E7210 MCH may be identified by the following component markings:

<table>
<thead>
<tr>
<th>Stepping</th>
<th>Q-Spec</th>
<th>S-Spec</th>
<th>Top Marking</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>A2</td>
<td>QE60</td>
<td>SL744W</td>
<td>RGE7210MC</td>
<td></td>
</tr>
</tbody>
</table>
Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes that apply to the listed E7210 MCH stepping. Intel may intend to fix some of the errata in a future stepping of the component and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

**Codes Used in Summary Table**

- **X:** Errata that applies to this stepping.
- **Doc:** Document change or update that will be implemented.
- **PlanFix:** This erratum may be fixed in a future stepping of the product.
- **Fixed:** This erratum has been previously fixed.
- **NoFix:** There are no plans to fix this erratum.
- (No mark) or (Blank Box): This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

**Shaded:** This item is either new or modified from the previous version of the document

<table>
<thead>
<tr>
<th>NO.</th>
<th>A2</th>
<th>PLANS</th>
<th>ERRATA</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>X</td>
<td>NoFix</td>
<td>FSB800 / DDR333 Running at 320 MHz Refresh Timing</td>
</tr>
</tbody>
</table>

**SPECIFICATION CHANGES**

There are no specification changes in this Specification Update revision.

**SPECIFICATION CLARIFICATIONS**

There are no specification clarifications in this Specification Update revision.

**DOCUMENTATION CHANGES**

There are no documentation changes in this Specification Update revision.
Errata

1. FSB800 / DDR333 Running at 320 MHz Refresh Timing Erratum

Problem: When a system is configured with an 800 MHz FSB process and DDR333 DIMM(s), the chipset's memory interface operates at 320 MHz. At this specific memory frequency, the chipset issues refresh cycles at a slower rate than the DDR333 JEDEC specification documents.

Chipset, with memory frequency at 320 MHz, issues refresh cycles every:
- 8.1 µs with 256-Mb and 512-Mb memory technology
- 16.2 µs with 64-Mb and 128-Mb memory technology

JEDEC spec for DDR333 devices is:
- 7.8 µs with 256-Mb and 512-Mb memory technology
- 15.6 µs with 64-Mb and 128-Mb memory technology

Implication: None

Workaround: None

Status: No silicon fix planned. Intel has contacted the major memory suppliers about this issue and has modified the DDR validation specification that Intel uses to test memory. Feedback from memory suppliers is that they can meet Intel's updated DDR validation specification.
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There are no Specification Changes in this Specification Update revision.
This page is intentionally left blank.
There are no Specification Clarifications in this Specification Update revision.
This page is intentionally left blank.
There are no documentation changes in this Specification Update revision.